ORDER NO. VKD84040819C8

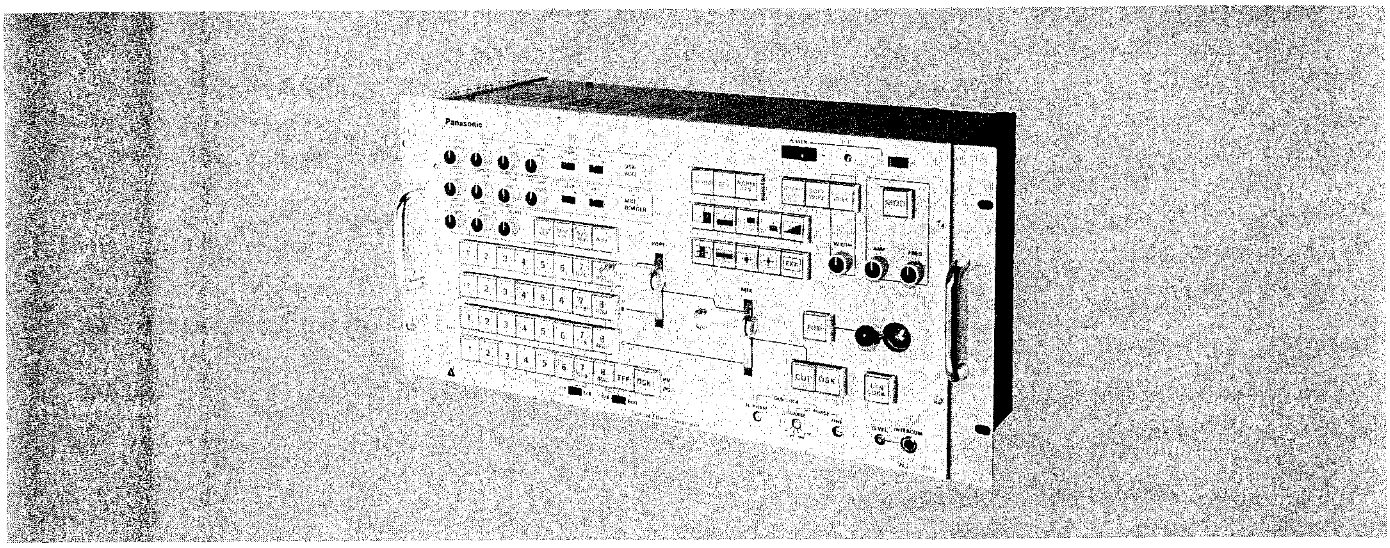
Service Manual

Vol. 1

Circuit Description

Special Effects Generator

WJ-5600



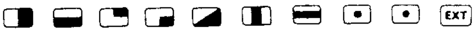
CONTENTS

Specifications 1
Outline 2
1. Output Board 6
2. DSK, BGD Board 10
3. Effect, Mix Board 16
4. Chroma Key Board 21
5. Input A, B and C Board 23
6. Input PV-PG Board 25
7. Wipe Process Board 27
8. Waveform Gen Board 31
9. Modulation Board 34
10. Lever Board 35
11. Sync. C/Bar Board 37
12. Mother Board 41
13. Connector Board/Termination Board 42

Panasonic

Matsushita Electric Trading Co., Ltd.
P.O. Box 288, Central Osaka Japan

SPECIFICATIONS

Video Input :	1.0Vp-p composite or 0.7Vp-p non-composite/75 ohms or Hi-Z looping through x 8 (BNC connectors)
R.G.B Video Input :	0.7Vp-p non-composite/75 ohms (BNC connectors)
DSK Video Input :	1.0Vp-p composite or 0.7Vp-p non-composite/75 ohms or Hi-Z looping through x 1 (BNC connector)
EXT Pattern Input :	1.0Vp-p composite or 0.7Vp-p non-composite pattern signal/75 ohms (Synchronized) (BNC connector)
Gen-lock Video Input :	1.0Vp-p VBS composite only/75 ohms or Hi-Z looping through x 1 (BNC connector)
Output (Program) :	1.0Vp-p composite/75 ohms x 2 (BNC connectors)
Preview Output :	1.0Vp-p composite/75 ohms x 2 (BNC connectors)
Sync Output :	HD, VD, BL, SYNC, BFP : 4.0Vp-p/75 ohms, SC : 2.0Vp-p/75 ohms, PAL PULSE (BNC connectors)
Black Burst Output :	0 setup Black signal (Composite Sync, Burst : 0.3Vp-p/75 ohms) x 3 (BNC connectors)
Gen-lock Range :	Sync : 15.625KHz ± 150Hz SC : 4.43361875MHz ± 50Hz
Colour Bar Signal :	Built-in EBU colour bar
Colour Generator :	2 generators with 3 controls (HUE, SAT, LUM) The one is used for Mat key and border wipe, the other is used for Background and DSK.
Switch :	All illuminated, non-locking type
Switching :	Vertical interval switching (input buses, preview/program buses and effect function buses)
Frequency Response :	10MHz ±1dB
Gain :	Unity
Signal to Noise Ratio :	More than 60dB
Differential Gain :	Less than 1.5% at 10 - 90% APL
Differential Phase :	Less than 1.5 at 10 - 90% APL
Crosstalk :	Better than 50dB at 4.43MHz (CUT Function, better than 45dB)
Functions :	
Input Bus :	Input A, B and C (camera 1 - 6, 7 or colour bar, 8 or background)
Preview/Program Bus :	Camera 1 - 6, 7 or colour bar, 8 or background, Effect, DSK
Effects :	
Mixing :	Yes
Downstream Mixing :	Yes
Fading :	Yes
Dissolves :	Yes
Superimposing :	Yes
Wipes :	Normal, normal-reverse or reverse wipe modes; sharp, soft edges or border edges; 9 wipe patterns with positioning and external pattern 
Wipe Modulation :	Yes (Horizontal only)
Wipe Key :	Yes
R.G.B Chrome Key (External key) :	Yes
Mat Key (Internal key) :	Yes (Nega-Posi switch)
Background :	Yes
Tally Light Control :	8 (camera 1 - 8)
Intercom :	9 (camera 1 - 8, self)
Power Source :	12V DC 2A or 240V AC 50Hz : WJ-5600/A, WJ-5600/B or 220V AC 50Hz : WJ-5600/C, WJ-5600/G
Power Consumption :	42W
Ambient Temperature :	0°C - 40°C (32°F - 104°F)
Ambient Humidity :	Less than 90%
Dimensions :	18-7/8 (X) x 8-11/16 (H) x 8-7/8 (D)
Weight :	20.9 lbs, 9.5kg

Circuit Description

Outline

Incoming video input signals from cameras or another systems at Video Input connectors 1 to 8 on the rear panel are sent to Input A, B, C and preview (PV)-program (PG) boards respectively and then they are selected by Input Selector switch on the each board. Selected input video signal on Input A, B, and C board is sent to the Effect, Mix board respectively. The selected input video signal on PV-PG board is sent to down stream (DSK), back ground (BGD) board.
The selected video signal on Input B board is also sent to the effect wave output circuit on the DSK, BGD board for mat key signal. The chroma key signal and wipe pattern are also supplied to effect wave output circuit, and selected effect wave selected by Wipe/Key Control switches on the Chroma Key board is sent to wipe/mat key amplifier circuit on the Effect, Mix board.

The 180° phase difference two color signals are generated at the mat, border color generator circuit on the Effect, Mix board and they are sent to border wipe amplifier circuit and CH.B-mat color switching circuit. The selected video signal from Input B board and Wipe/Key control signal of wipe, key or wipe key mode from mat key, wipe key, chroma key, wipe select circuit on the chroma key board are also supplied to CH.B-mat color switching circuit and then the selected signal is sent to wipe/mat key amplifier circuit. The selected video signal from Input A board and selected video signal from Input B board or mat color signal are supplied to wipe/mat key amplifier circuit, and these two signals are used for wiping or keying controlled by effect wave, and wiped or mat keyed signal is sent to border wipe amplifier circuit. The wipe/mat key signal from wipe/mat key amplifier circuit, border signal from mat border color generator circuit and border pulse from border pulse generator circuit on the Modulation board are supplied to the border wipe amplifier circuit, where the effect signal is produced for border wipe on wipe border when both wipe switch on the Wipe/Key Control and border wipe switch on the Wipe Mode Selector are selected.

This effect video signal and selected video signal from Input C board are supplied to mix amplifier circuit and they are mixed by mix control signal from mix lever and this signal is sent out to switching circuit on Output board as program video signal. The effect video signal is also supplied to video input 1 to 8 EFF video select circuit on the DSK, BGD board, and its circuit also receives selected video signal from Input PV- PG board. Then selected signal is sent to cut switching circuit on Output circuit as preview video signal.

The output signal from cut switching circuit on the Output board is switched by CUT ON/OFF switch and the output signal is supplied to program-DSK switching circuit and preview DSK switching circuit. For example, when CUT switch is OFF, the program video signal is supplied to program-DSK switching circuit and preview video signal is supplied to preview-DSK switching circuit, when CUT switch is ON, the program video signal is supplied to preview-DSK switching circuit and preview video signal is supplied to program-DSK switching circuit.

The DSK signal from DSK input connector on the rear panel is supplied to the DSK pulse generator circuit on the DSK, BGD board, where the DSK pulse is generated when DSK ON/OFF switch is ON. The DSK pulse is sent to DSK process circuit.

The DSK, BGD color generator circuit generates the 180° phase difference two color signals and sents to BGD-C/8 switching circuit and DSK process circuit.
The output signal of cut switching circuit which is same signal as supplied to program-DSK switching circuit is also supplied to DSK process circuit where the DSK pulse is produced which is mixed with cut switching output signal, DSK pulse and DSK color. Then DSK signal is supplied to program-DSK switching circuit and preview-DSK switching circuit.

The program-DSK switching circuit selects output signal from two input video signal by DSK control signal. The video signal selected by DSK ON/OFF switch becomes program signal when CUT ON/OFF switch is OFF.When CUT ON/OFF switch is ON, selected signal by DSK ON/OFF switch or DSK switch on the input PV-PG selector switch becomes program signal. For example when DSK switch is ON, DSK signal is sent to program out process circuit.
While cut ON/OFF switch is OFF, the output signal of cut switching circuit and the output signal of DSK process circuit are supplied to the preview-DSK switching circuit, where the cut switching signal and the DSK process signal are selected by the DSK switch on the Input PV-PG selector board, and the selected signal is

supplied to the preview out process circuit. For example, when DSK switch on the input PV-PG selector is ON, the output signal of DSK process circuit is supplied to the preview out process circuit.
However, while CUT ON/OFF switch is ON, program signal from cut switching circuit is constantly supplied to preview out process circuit through preview-DSK switching circuit.

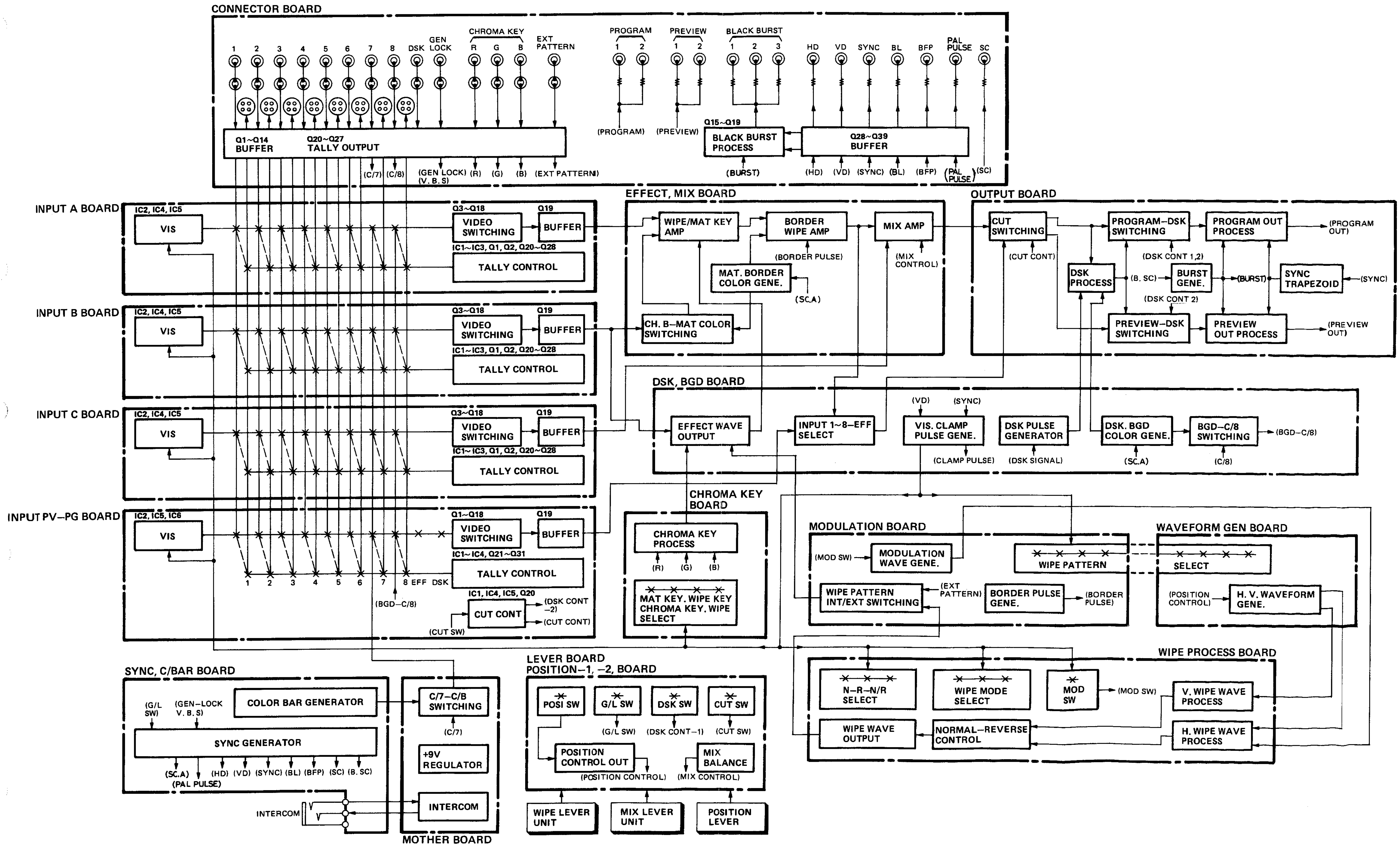
These outputs of program-DSK switching circuit and preview-DSK switching circuit are supplied to program out process circuit and preview out process circuit respectively, where the burst signal and sync signal are added and the composite video signals are sent to the program output connector and preview output connector on the rear panel respectively as output signal of Special effect generator (SEG) WJ-5600.

The burst subcarrier pulse (B.SC) from Sync, C/Bar board is supplied to burst generator circuit where the burst subcarrier pulse is converted to the burst signal and the burst signal is supplied to the program out process circuit and preview out process circuit respectively. The burst signal is also supplied to Connector board for making the black burst signal.
The border pulse which is used for border wipe is produced at border pulse generator circuit from internal wipe wave and the border pulse is supplied to Effect Mix board. In lever connection board, switching of Gen-Lock ON/OFF switch, DSK ON/OFF switch and Cut ON/OFF switch is made at vertical blanking periods and the control signal is supplied to other circuits. Otherhand, the control signal from lever unit is fed through this circuit to each circuit.
The control signal from mix lever unit is controlled by position-1 and position-2 boards and fed through lever connection board to each circuit.

The mother board is connected each circuit boards. The AC power which is supplied from rear panel is supplied to AC-DC select switch through Power ON/OFF switch, power transformer and rectifier.
The +12V DC power which is supplied to EXT DC input connector is also supplied to AC-DC select switch and the one of DC power is supplied to +9V DC regulator circuit for producing the necessary +9V DC power of SEG WJ-5600. And the +12V DC power is also supplied to each circuit for power source of switch pilot lamp.
The intercom unit, connected to Tally Intercom connector on the rear panel is received DC power from intercom circuit on SEG WJ-5600 and talk voice from headset connected on the front panel. The headset can be received the talk voice of intercom unit through audio amplifier circuit inside SEG WJ-5600.

The video signal which supplied to Video Input connector 7 and color bar signal which produced at Sync C/Bar board are supplied to C/7-C/B switching circuit, where the one of both signal is selected by C/7, Color Bar selector switch and the selected signal is sent to input A, B, C and PV-PG boards. The sync generator circuit on the Sync C/Bar board is produced horizontal drive (HD) pulse, vertical drive (VD) pulse, sync pulse, blanking (BL) pulse, subcarrier (SC) pulse and burst subcarrier (BSC) pulse, and the produced pulses are sent to each output connector on the rear panel as SEG output pulses through connector board.
The other hand, external sync signal (Gen-Lock signal) is supplied to the G/L input connector on the rear panel, and while Gen-Lock ON/OFF switch on the front panel is ON, the SEG output pulses are synchronized to the external sync signal.
The internal color bar signal is produced at color bar generator circuit and the color bar signal is sent to the C/7-C/B switching circuit.

OUTLINE BLOCK DIAGRAM


CONNECTOR BOARD
1 2 3 4 5 6 7 8 DSK
GEN LOCK
CHROMA KEY R G B
EXT PATTERN
PROGRAM 1 2
PREVIEW 1 2
BLACK BURST 1 2 3
HD VD SYNC BL BFP PAL PULSE SC
Q1~Q14 BUFFER
Q20~Q27 TALLY OUTPUT
(C/7) (C/8) (GEN LOCK) (V. B. S) (R) (G) (B) (EXT PATTERN)
(PROGRAM) (PREVIEW)
Q15~Q19 BLACK BURST PROCESS
(BURST)
Q28~Q39 BUFFER
(HD) (VD) (SYNC) (BL) (BFP) (PAL PULSE) (SC)
INPUT A BOARD
IC2, IC4, IC5
VIS
Q3~Q18 VIDEO SWITCHING
Q19 BUFFER
IC1~IC3, Q1, Q2, Q20~Q28
TALLY CONTROL
INPUT B BOARD
IC2, IC4, IC5
VIS
Q3~Q18 VIDEO SWITCHING
Q19 BUFFER
IC1~IC3, Q1, Q2, Q20~Q28
TALLY CONTROL
INPUT C BOARD
IC2, IC4, IC5
VIS
Q3~Q18 VIDEO SWITCHING
Q19 BUFFER
IC1~IC3, Q1, Q2, Q20~Q28
TALLY CONTROL
INPUT PV–PG BOARD
IC2, IC5, IC6
VIS
Q1~Q18 VIDEO SWITCHING
Q19 BUFFER
IC1~IC4, Q21~Q31
TALLY CONTROL
1 2 3 4 5 6 7 8 EFF DSK
(BGD–C/8)
IC1, IC4, IC5, Q20
CUT CONT
(DSK CONT –2)
(CUT CONT)
(CUT SW)
EFFECT, MIX BOARD
WIPE/MAT KEY AMP
BORDER WIPE AMP
MIX AMP
(BORDER PULSE)
(MIX CONTROL)
MAT. BORDER COLOR GENE.
(SC.A)
CH. B–MAT COLOR SWITCHING
OUTPUT BOARD
CUT SWITCHING
(CUT CONT)
PROGRAM–DSK SWITCHING
PROGRAM OUT PROCESS
(PROGRAM OUT)
(DSK CONT 1,2)
DSK PROCESS
(B. SC)
BURST GENE.
(BURST)
SYNC TRAPEZOID
(SYNC)
(DSK CONT 2)
PREVIEW–DSK SWITCHING
PREVIEW OUT PROCESS
(PREVIEW OUT)
DSK, BGD BOARD
EFFECT WAVE OUTPUT
INPUT 1~8–EFF SELECT
(VD) (SYNC)
VIS. CLAMP PULSE GENE.
(CLAMP PULSE)
DSK PULSE GENERATOR
(DSK SIGNAL)
DSK. BGD COLOR GENE.
(SC.A)
BGD–C/8 SWITCHING
(C/8)
(BGD–C/8)
CHROMA KEY BOARD
CHROMA KEY PROCESS
(R) (G) (B)
MAT KEY. WIPE KEY CHROMA KEY. WIPE SELECT
MODULATION BOARD
(MOD SW)
MODULATION WAVE GENE.
WIPE PATTERN
WIPE PATTERN INT/EXT SWITCHING
(EXT PATTERN)
BORDER PULSE GENE.
(BORDER PULSE)
WAVEFORM GEN BOARD
SELECT
(POSITION CONTROL)
H. V. WAVEFORM GENE.
WIPE PROCESS BOARD
N–R–N/R SELECT
WIPE MODE SELECT
MOD SW
(MOD SW)
V. WIPE WAVE PROCESS
WIPE WAVE OUTPUT
NORMAL–REVERSE CONTROL
H. WIPE WAVE PROCESS
SYNC, C/BAR BOARD
(G/L SW)
(GEN–LOCK V. B. S)
COLOR BAR GENERATOR
SYNC GENERATOR
(SC.A) (HD) (VD) (SYNC) (BL) (BFP) (SC) (B. SC)
(PAL PULSE)
INTERCOM
C/7–C/B SWITCHING
(C/7)
+9V REGULATOR
INTERCOM
MOTHER BOARD
LEVER BOARD
POSITION–1, –2, BOARD
POSI SW
G/L SW
DSK SW
CUT SW
(G/L SW) (DSK CONT–1) (CUT SW)
POSITION CONTROL OUT
MIX BALANCE
(POSITION CONTROL) (MIX CONTROL)
WIPE LEVER UNIT
MIX LEVER UNIT
POSITION LEVER

1 OUTPUT BOARD

The output board contains following circuits.

1-1 Program Out Processing Circuit 6
1-2 DSK Processing Circuit 7
1-3 Burst Generator Circuit 8
1-4 Sync Trapezoid Circuit 8
1-5 Cut Switching Circuit 9
1-6 Preview Out Processing Circuit 9

1-1 Program Out Processing Circuit

Outline

This circuit consists of a phase shifter circuit, clamp circuit, blanking killer circuit, white clip circuit, burst and sync addition circuit and output circuit.

This circuit process the incoming video signal to specified 1.0Vp-p composite video signal as program output signal.

Details

- Phase shifter circuit

The video signal from pins 9(a) and 13(a) of CN15 selected by cut switching circuit is supplied to phase shifter circuit consists of Q2 and Q3, where the chroma phase of the video signal matches to chroma phase of downstream key signal (DSK), controlled by VR1 (PROGRAM CHROMA PHASE). The video signal is then sent to program/DSK switching circuit through buffer Q4.

- Program/DSK switching circuit

This circuit consists of Q5 and Q6.

When DSK ON/OFF switch is turned ON, high potential is supplied to bases of Q5 and Q6, then Q5 turns ON, and DSK/program signal produced at DSK processing circuit is sent to the program output circuit. However, DSK switch is in OFF, then Q6 turns ON, so, phase shifted video signal is sent to program output circuit.

- Clamp circuit

The video signal at collector of Q5 or Q6 is sent to clamp circuit consist of Q7 and Q8, where the blanking level of the video signal is clamped by the clamp pulse fed to the gate of Q7 and the blanking level is set to the DC voltage at the drain of Q7.

VR2 (PROGRAM SETUP) sets the pedestal level of the video signal by changing the clamp potential. L1 and C8 are added as filter to prevent the influence of burst signal when setting the pedestal clamp, because, pedestal clamp is set at back porch of sync signal and burst signal also exist at the same place. The video signal whose blanking potential is set is sent to the blanking killer amplifier IC1.

- Blanking killer amplifier circuit

The clamped video signal Ⓐ is supplied to pin 9 of IC1 through buffer Q8 and Q9. The video signal at pin 9 of IC1 is fed to differential amplifier inside IC1 where the sync and burst signal at blanking periods of video signal are clipped by negative blanking (BL) signal Ⓑ at pin 6 of IC1. The voltage divided by R19, R20 and VR3 (BL KILLER DC BIAS) is supplied to pins 5 and 6 of IC1 through buffer Q10 and R29 and R22 respectively as base bias for TR2 and TR3, and TR1 and TR4 inside IC1 respectively.

While pin 6 of IC1 is in high potential, therefore TR2, TR3, TR5 and TR6 are turned ON, thus video signal at pin 9 of IC1 is obtained at pin 8 of IC1 through TR5 and TR2.

However, when negative blanking signal is supplied at pin 6 of IC1, TR1 and TR4 are turned ON and TR2 and TR3 are turned OFF, therefore blanking periods of video signal Ⓒ obtained at pin 8 of IC1 is clipped at emitter potential (a) of TR6.

C10 and VR5 (BL SPIKE COMP-1) are added for eliminate the BL spike noise by changing the collector impedance of TR1 and TR3.

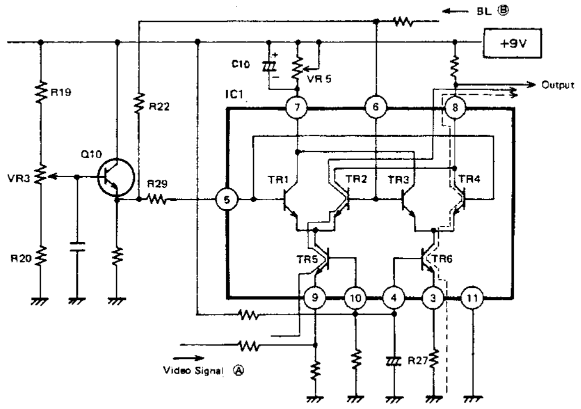


Fig. 1-1-1 Blanking killer amplifier

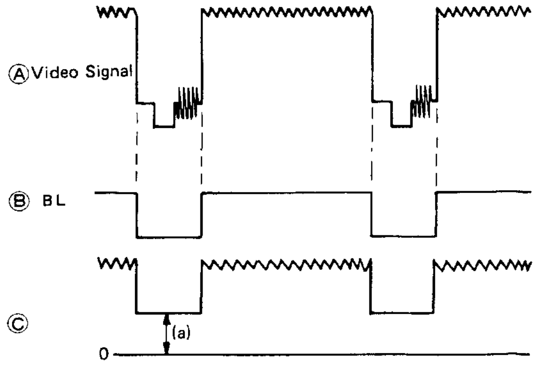


Fig. 1-1-2 Blanking killer

- White clip circuit

Video signal whose blanking periods are clipped to pin 8 of IC1 is sent to the white clip circuit consisting of Q13 and Q14 through program DG-DP Q11 and buffer Q12. VR7 (PROGRAM DG,DP) sets the differential gain (DG) and differential phase (DP) of video signal by controlling the base bias of Q11.

Usually video signal Ⓐ at emitter of Q12 is fed to Q13 and obtained at emitter of Q13.

However, excessively bright signal is supplied to base of Q13, base potential of Q13 increased and turns Q13 OFF, and emitter potential of Q14 increased and Q14 turns ON, thus the bright portion of video signal is suppressed Ⓑ.

VR8 (WHITE CLIP-1) sets the clip level of video signal for 0.9V from blanking level.

The white clipped video signal is then supplied to sync and burst addition circuit consisting of Q16 through buffer Q15 and gain control VR9 (PROGRAM GAIN-1).

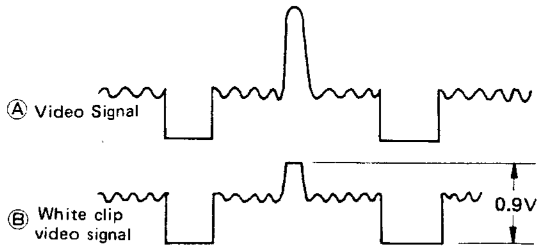


Fig. 1-1-3 White clip

- Burst and sync addition circuit

The bust signal Ⓐ from emitter of Q35 and sync signal Ⓑ from emitter of Q66 are supplied to Q16 base and video signal is supplied to its emitter, therefore, burst signal and sync signal are placed at blanking periods of video signal, thus, composite video signal Ⓒ appears at collector of Q16. VR10 (BURST GAIN-1) sets the gain of burst signal for 0.3Vp-p.

VR11 (SYNC GAIN-1) sets the gain of sync signal for 0.3V from pedestal level. CT1, (FREQUENCY RESPONSE-1) is a control for setting the phase of burst signal to matching the chroma phase of input signal.

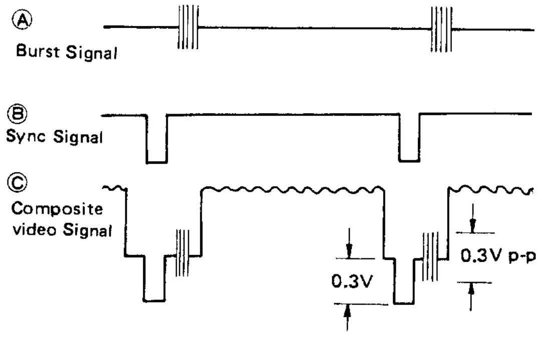


Fig. 1-1-4 Burst and -sync addition

- Program output circuit

The composite video signal is sent to the program output connector on the rear panel through buffer Q17, single end push-pull amplifier program output circuit consists of Q18, Q19 and D1, and pin 5(b) of CN15.

1-2 DSK Processing Circuit

Outline

This circuit produces downstream key (DSK) signal from video signal modulated by DSK pulse and DSK color signal and the DSK signal is supplied to program out processing circuit and preview out processing circuit.

Details

This circuit consists of a video signal clamp circuit, DSK mix amplifier circuit, DSK color clamp circuit, and edge mix amplifier circuit.

The incoming video signal selected by switching circuit consists of Q39-Q42 is supplied to program out processing circuit and also sent to DSK processing circuit consists of Q20-Q31 and IC2.

The video signal Ⓐ through C23 is sent to clamp circuit where blanking level of the video signal is clamped by the clamp pulse fed to the gate of Q20 and the blanking level is set to the DC voltage at the drain of Q20.

VR12 (PROGRAM SETUP-2) sets the pedestal level of the video signal to same level as DSK color signal by changing the clamped potential, due to DSK pulse is mixed with DSK color signal.

The clamped DSK pulse is supplied to pin 9 of DSK mix amplifier IC2 through buffers Q21 and Q22. The DSK pulse Ⓑ from pin 18 (b) of CN15 is supplied to pin 5 of IC2 through buffer Q33. The DC voltage divided by R66, R67 and VR14 (DSK DC BIAS) is sent to pins 5 and 6 of IC2 through buffer Q23 as base bias of TR1 and TR4, and TR2 and TR3 of inside IC2 respectively.

The DSK color signal Ⓒ from pin 2 (b) of CN15 is sent to pin 3 of IC2 through clamp circuit consisting of Q26, buffer Q24 and VR13 (DSK GAIN).

While pin 5 of IC2 is Low level, TR2, TR3, TR5 and TR6 are turned ON, therefore video signal at pin 9 of IC2 is fed to TR5 and TR2 and obtained at pin 8 of IC1.

However, when DSK pulse is supplied at pin 5 of IC2 TR1, TR4, TR5 and TR6 are turned ON, therefore video signal is not obtained at pin 8 of IC2 and the video level at DSK pulse periods are set to the emitter potential of Q6 and DSK color signal is obtain at pin 8 of IC2 through TR6 and TR4 inside IC2, thus DSK/program signal Ⓓ is produced.

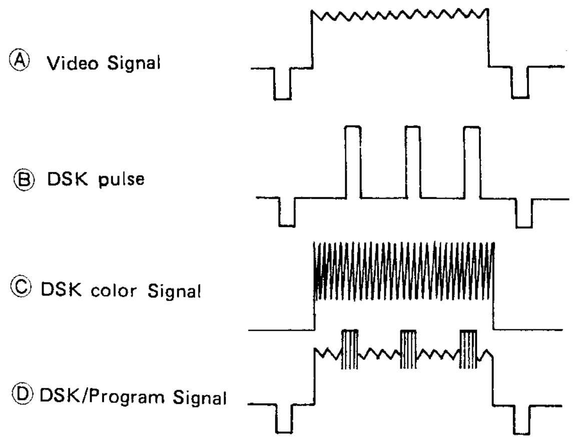

Ⓐ Video Signal
Ⓑ DSK pulse
Ⓒ DSK color Signal
Ⓓ DSK/Program Signal

Fig. 1-2-1 DSK/program signal-1

VR15 (DSK SPIKE COMP) minimize the spike noise at the edge of DSK pulse and video signal by changing the collector bias of TR1 and TR3 inside IC2. DSK/program signal at pin 8 of IC2 is then sent to edge mix amplifier Q29 through program/DSK DG.DP Q27 and buffer Q28. VR16 (DSK/PROGRAM GAIN) sets the DSK/program signal gain for 1.0 V p-p.

VR17 (DSK/PROGRAM DG.DP) controls the DG.DP of DSK/program signal.

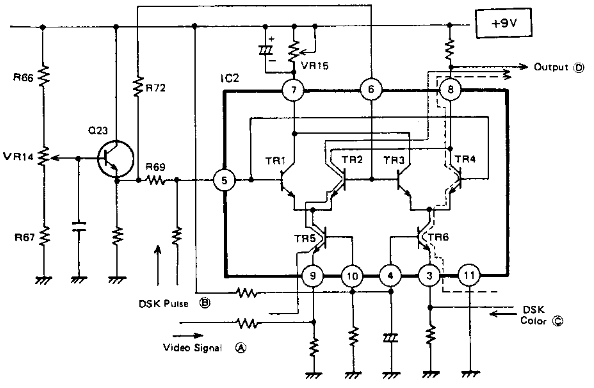

+9V
R66
R72
IC2
VR15
Output Ⓓ
Q23
VR14
R69
TR1
TR2
TR3
TR4
TR5
TR6
R67
7
6
8
5
9
10
4
3
11
DSK Pulse Ⓑ
Video Signal Ⓐ
DSK Color Ⓒ

Fig. 1-2-2 DSK /processing circuit

The DSK edge signal Ⓐ is sent to the edge mix amplifier Q30 through buffer Q31 and edge ON/OFF switching Q32. When EDGE switch at the DSK/BGD control on the front panel is turned ON, high level is obtained at base of Q32 and turns Q32 and Q31 ON, thus edge signal is mixed with DSK/program signal Ⓑ, and edge mixed DSK/program signal Ⓒ is produced.

When EDGE switch of DSK/BGD control is turned OFF, Q32 and Q31 OFF, thus edge signal is not supplied to edge mix circuit.

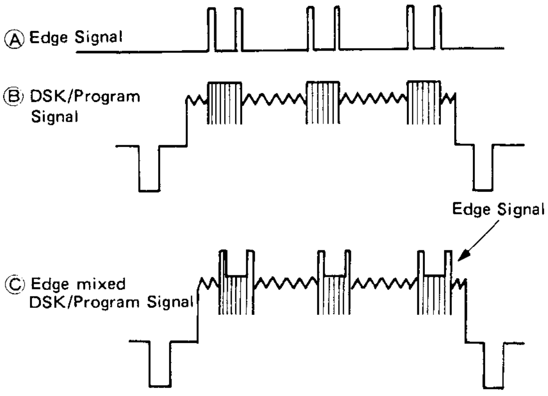

Ⓐ Edge Signal
Ⓑ DSK/Program Signal
Edge Signal
Ⓒ Edge mixed DSK/Program Signal

Fig. 1-2-3 DSK/program signal-2

1-3 Burst Generator Circuit

Outline

This circuit separates burst signal from bursted subcarrier signal.

Details

The burst subcarrier signal Ⓐ from pin 17 (a) of CN15 is sent to band pass filter (B.P.F) F1 through subcarrier phase shifter Q38 and buffer Q36, where the only 4.43 MHz burst signal Ⓑ is passed, and burst signal is supplied to program out processing circuit, preview out processing circuit and pin 16 (a) of CN 15 through buffer Q35.

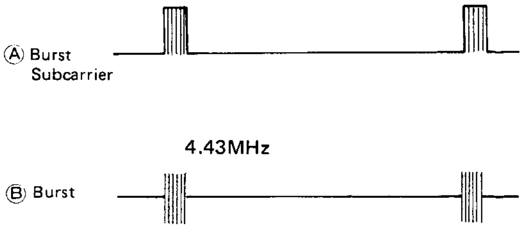

Ⓐ Burst Subcarrier
4.43MHz
Ⓑ Burst

Fig. 1-3-1 Burst signal

1-4 Sync Trapezoid Circuit

Outline

This circuit produces trapezoid sync signal.

Details

The positive sync pulse Ⓐ from pin 14 (b) of CN 15 is sent to delay circuit consists of R188, R189, R190, C67 and Q65 through buffer Q64, where the sync pulse is trapezoid Ⓑ and its supplied to program out processing circuit and preview out processing circuit through buffer Q66.

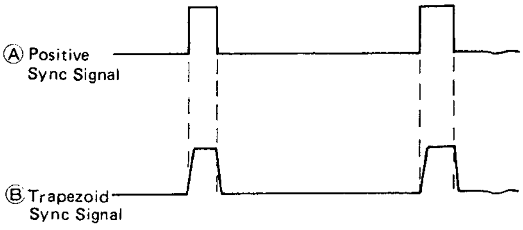

Ⓐ Positive Sync Signal
Ⓑ Trapezoid Sync Signal

Fig. 1-4-1 Sync signal

1-5 Cut Switching Circuit

Outline

This circuit selects the input signals which are the CH.PV-PG or Effect signal and Mix video signal by switching Q43. The selected signal is supplied to the program out processing circuit/DSK processing circuit and preview out processing circuit respectively.

Details

The mix video signal at pin 13 (a) of CN15 is supplied to emitters of Q41, and Q42. The CH. PV-PG or Effect video signal at pin 9 (a) of CN15 is supplied to emitters of Q39 and Q40. Q43 is a switching transistor and controlled by cut ON/OFF switch on the front panel. While, cut ON/OFF switch is OFF, high potential is obtained at bases of Q40, Q42 and Q43, therefore Q40 and Q41 are turned ON, thus mix video signal is supplied to program out processing circuit and DSK processing circuit through Q41, and CH.PV-PG or Effect signal is supplied to preview out processing circuit through Q40. When, cut ON/OFF switch is ON, low potential is obtained at bases of Q40, Q42 and Q43 therefore Q39, Q42 and Q43 are turned ON, thus mix video signal is supplied to preview out processing circuit through Q42 and CH.PV-PG or Effect signal is sent to program out processing circuit and DSK processing circuit through Q39.

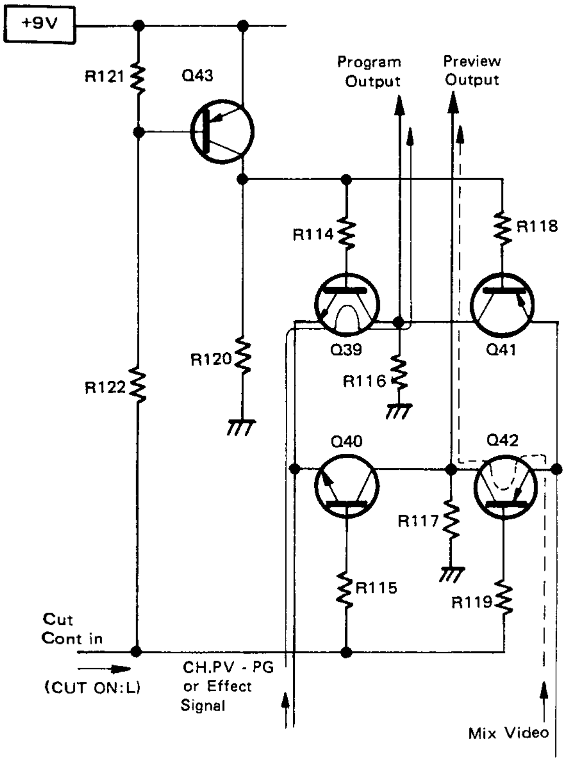


Fig. 1-5-1 Cut switching circuit

1-6 Preview Out Processing Circuit

Outline

This circuit uses same design as the program out processing circuit.

The circuit process the incoming video signal to specified 1.0 Vp-p composite video signal as preview output signal.

Details

- Phase shifter circuit

The video signal from pin 9 (a) of CN15 or pin 13 (a) of CN15 selected by cut switch is supplied to phase shifter circuit consists of Q44 and Q45, where the chroma phase of the video signal matches to chroma phase of DSK signal, control by VR20 (PREVIEW CHROMA PHASE). The video signal is then supplied to preview/DSK switching circuit through buffer Q46.

- Preview/DSK switching circuit

This circuit consists of Q47 and Q48. When DSK switch on the preview/program selector is turned ON, high potential is obtained to bases of Q47 and Q48, thus Q47 turns ON, so, DSK/program signal produced at DSK processing circuit is sent to the preview output circuit. However, DSK switch is in OFF, Q48 turns ON, so, phase shifted video signal is sent to preview output circuit.

- Clamp circuit

The video signal at collector Q47 or Q48 is sent to clamp circuit consisting of Q49, where the blanking level of the video signal is clamped by the clamp pulse fed to the gate of Q49 and the blanking level is set to the DC voltage at the drain of Q49.

VR21 (PREVIEW SETUP) sets the pedestal level of the video signal by changing the clamped potential. L4 and C49 are added as filter to prevent the influence of burst signal when setting the pedestal clamp, because, pedestal clamp is set at back porch of sync signal and burst signal also exist at the same place.

The video signal whose blanking potential is set is supplied to the blanking killer amplifier IC3.

- Blanking killer amplifier circuit

The clamped video signal is sent to pin 9 of IC3 through buffers Q50 and Q51. The video signal at pin 9 of IC3 is fed to differential amplifier inside IC3 where the sync and burst signal at blanking periods of video signal are clipped by negative blanking signal at pin 6 of IC3. The voltage divided by R138, R139 and VR23 (BLANKING DC BIAS-2) is sent to pins 5 and 6 of IC3 through buffer Q52 and R148 and R141 respectively as base bias for TR1 and TR4, and TR2 and TR3 respectively.

While pin 6 of IC1 is in high potential, TR2, TR3, TR5 and TR6 are turned ON, therefore video signal at pin 9 of IC3 is obtained at pin 8 of IC3 through TR5 and TR2 inside IC3.

However, when negative blanking signal appear at pin 6 of IC1, TR2, TR3 are turned OFF and TR1, TR4, TR5 and TR6 are turned ON, therefore blanking periods of video signal is clipped at emitter potential of TR6. C52 and VR24 (BL SPIKE COMP-2) are added for eliminate the BL spike noise by changing the collector impedance of TR1 and TR3.

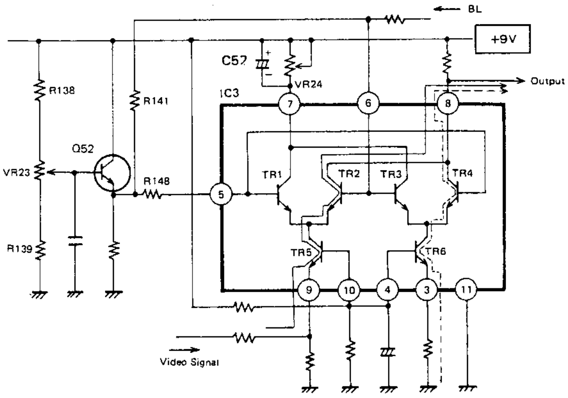


Fig. 1-6-1 Blanking killer amplifier circuit

- White clip circuit

The video signal whose blanking periods are clipped and obtained at pin 8 of IC3 is sent to the white clip circuit consists Q55 and Q56 through preview DG.DP Q53 and buffer Q54.

VR26 (PREVIEW DG.DP) sets the DG.DP of video signal by controlling the base bias of Q53.

Usually video signal at emitter of Q54 is fed to Q55 and obtained at emitter of Q55. However, excessively bright signal is applied to base of Q55, base potential of Q55 increased and turns Q55 OFF, and emitter potential of Q56 increased and Q56 turns ON, thus the excessively bright portion of video signal is suppressed.

VR27 (WHITE CLIP-2) sets the clip level of video signal for 0.9V from blinking level.

The white clipped video signal is then sent to sync and burst addition circuit consisting of Q60 through buffer Q59 and gain control VR29 (PREVIEW GAIN-3).

- Burst and sync addition circuit

The bust signal from emitter of Q35 and sync signal from emitter of Q66 are supplied to Q60 base and video signal is supplied to its emitter, therefore, burst signal and sync signal are placed at blanking periods of video signal, thus, composite video signal is obtained at collector of Q60.

VR30 (BURST GAIN-2) sets the gain of burst signal for 0.3 Vp-p.

VR31 (SYNC GAIN-2) sets the gain of sync signal for 0.3 Vp-p from pedestal level.

CT2 (FREQUENCY RESPONSE-2) is a control for setting the phase of burst signal to matching the chroma phase of input signal.

- Program output circuit

The composite video signal is sent to the preview output connector on the rear panel through buffer Q61, single end push-pull amplifier preview output circuit consisting of Q62, Q63 and D2, and pin 19 (b) of CN15.

2 DSK, BGD Board

The downstream key (DSK), back ground (BGD) board contain following circuits.

2-1. BGD, DSK Color Generator Circuit. 10
2-2. DSK Pulse Generator Circuit 13
2-3. DSK Edge Generator Circuit 13
2-4. CH, PV-PG 1-8/Effect Selector Circuit 13
2-5. C/8-BGD Selector Circuit · · · · · · · · · · · · · · 14
2-6. VIS, Clamp Pulse Generator Circuit 14
2-7. Wipe Key, Mat Key Signal Process Circuit . . . 15
2-8. Effect Wave Output Select Circuit 15

2-1 BGD, DSK Color Generator Circuit

Outline

This circuit consists a subcarrier (SC) generator circuit, blanking killer amplifier circuit and DSK chroma phase shifter circuit.

This circuit produces BGD, DSK color signal from SCA signal.

Details

The 2.215MHz SC A pulse Ⓐ from pin 21 (a) of CN16 is supplied to B inputs of monostable multivibrator

(M.M) at pin 2 of IC4 (a) and pin 10 of IC4 (b) respectively, then the rise timing of SC A pulse, negative pulse Ⓑ is obtained at $\overline{Q}_B$ and $\overline{Q}_A$ outputs of M.M at pin 4 of IC4 (a) and pin 10 of IC4 (b) respectively. Refer to trath table 2-1-1.

The width of output pulses at pin 4 of IC4 (a) and pin 12 of IC4 (b) is controlled by VR2 (HUE), and the VR2 is connected in series between pin 15 of IC9 (a) and pin 7 of IC9 (b), and +5V DC is supplied to center tap of VR2, therefore the width variation of individual outputs at pin 4 of IC4 (a) and pin 12 of IC4 (b) are inversed, because of the chroma phase of PAL color signal is 90° difference by each 1H line.

CT1 (HUE PRESET-1) and CT2 (HUE PRESET-2) set the chroma phase of Border and Mat color signal can be changed 380° by VR2 (HUE).

The negative pulses obtained at pin 4 of IC4 (a) and pin 12 of IC4 (b) are supplied to A and B input of analog switch at pin 2 and pin 3 of IC5 (a) respectively.

While strobe (G) input at pin 15 of IC5 (a) is low level by the color ON/OFF switch SW1 on the Mat/Border control is ON, depending on the high level or low level of select (S) input at pin 1 of IC5 (a) by PAL pulse Ⓒ, B or A input pulses are selected and the selected pulse appeared Y output at pin 4 of IC5 (a). Refer to truth table 2-1-2.

When Color ON/OFF switch SW1 is OFF, high level is supplied to G input at pin 15 of IC4 (a) through R21, therefore no output signal appeared Q and $\overline{Q}$ outputs at pin 13 and pin 4 of IC6 (a).

While S input is high level, B input pulse is obtained at Y output and S input is low level, A input pulse is obtained at Y output Ⓓ.

The Y output pulse is supplied to B input of M.M at pin 2 of IC6 (a) then the rise timing of B input pulse, positive pulse and negative pulse appeared Q and $\overline{Q}$ output at pin 13 and pin 4 of IC6 (a) respectively Ⓔ.

VR6 (SC DUTY) is a control for adjusting the wave width of Q and $\overline{Q}$ output signals at pin 13 and pin 4 of IC6 (a) for fifty-fifty respectively.

The positive pulse and negative pulse obtained at pin 13 and pin 4 of IC6 (a) are supplied to A and B input at pin 2 and pin 3 of IC7 (a) respectively.

The positive pulse is also supplied to analog switch delay circuit consisting of IC7 (b), (c), (d) and IC5 (b), (c), (d) where the positive pulse is delayed approximately 90° Ⓕ, and the delayed pulse is supplied to S input at pin 1 of IC7 (a) as select signal.

While pin 1 of IC7 (a) is high level, input B pulse is obtained at Y output and when pin 1 of IC7 (a) is low level, input A pulse is obtained at Y output, as a result 2.215MHz input pulse is converted to 4.43MHz pulse Ⓗ and this pulse is supplied to B input at pin 10 of analog switch IC6 (b).

The rise time of 4.43MHz pulse, negative 4.43MHz pulse is obtained $\overline{Q}$ output at pin 12 of IC6 (b).

This 4.43MHz pulse is supplied to buffer Q1 through differential circuit consisting of C9 and R7.

The output signal of buffer Q1 is then supplied to phase shifter circuit consisting of Q2, C12 and VR6 (SUB CARRIER PHASE) through 4.43MHz band pass filter (B.P.F) F1, where the phase of SC signal is adjusted to specified SC signal Ⓘ by VR6.

The specified SC signal is supplied to pin 3 of differential amplifier IC1 through buffer Q9 and VR3 (SATURATION).

Truth table of M.M

Input			Output	
Clear (CL)	A	B	Q	$\overline{Q}$
H	L	↑	⎍	⊔

↑ : **Rise timing**
⎍ : **One positive pulse**
⊔ : **One hegative pulse**

Table 2-1-1

Truth table of analog switch

Color ON/OFF Switch (SW1)	Input				Outpu
	Strobe (G)	Selet (S)	A	B	Y
OFF	H	X	X	X	L
ON	L	L	L	X	L
			H	X	H
		H	X	L	L
			X	H	H

X: H or L,Do not care

Table 2-1-2

- Blanking killer amplifier

The DC voltage divided by R28 and R29 is supplied to pin 4 of IC1 as base bias of constant current transistor TR5 inside IC1.

The DC voltage divided by VR4 (LUMINANCE), R26, VR5 (LUMINANCE SETUP) and R27 is supplied to pin 10 of IC1 as base bias of constant current transistor TR6 inside IC1.

The DC voltage divided by R47, VR9 (BL KILLER DC BIAS) is supplied to pin 5 and pin 6 of IC1 as base bias of TR1 and TR4, and TR2 and TR3 inside IC1 respectively through buffer Q13.

The negative blanking (BL) signal obtained at pin 13 (b) of CN17 is supplied to pin 6 of IC1 through buffer Q10. Unless, C.P.BL signal is supplied at pin 6 of IC1, TR2, TR3, TR5 and TR6 turns ON, therefore SC signal at pin 6 is obtained at pin 7 of IC1 through TR5 and TR2. However, when C.P.BL Ⓙ is supplied to pin 6 of IC1, TR1, TR4, TR5 and TR6 are turned ON, therefore SC signal is not obtained at pin 7 of IC1 and blanking level of SC signal is set with emitter potential of TR6, thus blanking periods of SC singal is eliminated, and blanked SC signal Ⓚ is produced.

This signal is supplied to the DSK chroma phase shifter circuit and C/8-BGD selector circuit through DSK.BGD DG.DP Q11 and buffer Q12.

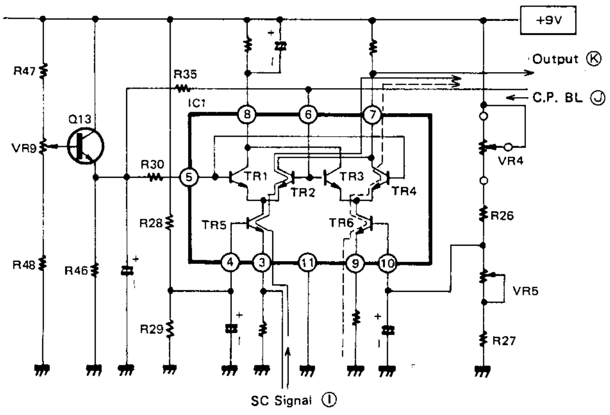

+9V
R47
R35
IC1
Output Ⓚ
C.P. BL Ⓙ
Q13
VR9
R30
8
6
7
5
TR1
TR2
TR3
TR4
VR4
R28
TR5
TR6
R26
R48
R46
4
3
11
9
10
VR5
R29
R27
SC Signal Ⓘ

Fig. 2-1-1 Blanking killer amplifier circuit

- DSK chroma phase shifter circuit

This circuit consists Q14-Q17, where the phase of blanked SC signal is controlled by VR10 (DSK CHROMA PHASE) and supply to pin 2 (a) of CN16 as a DSK color out signal.

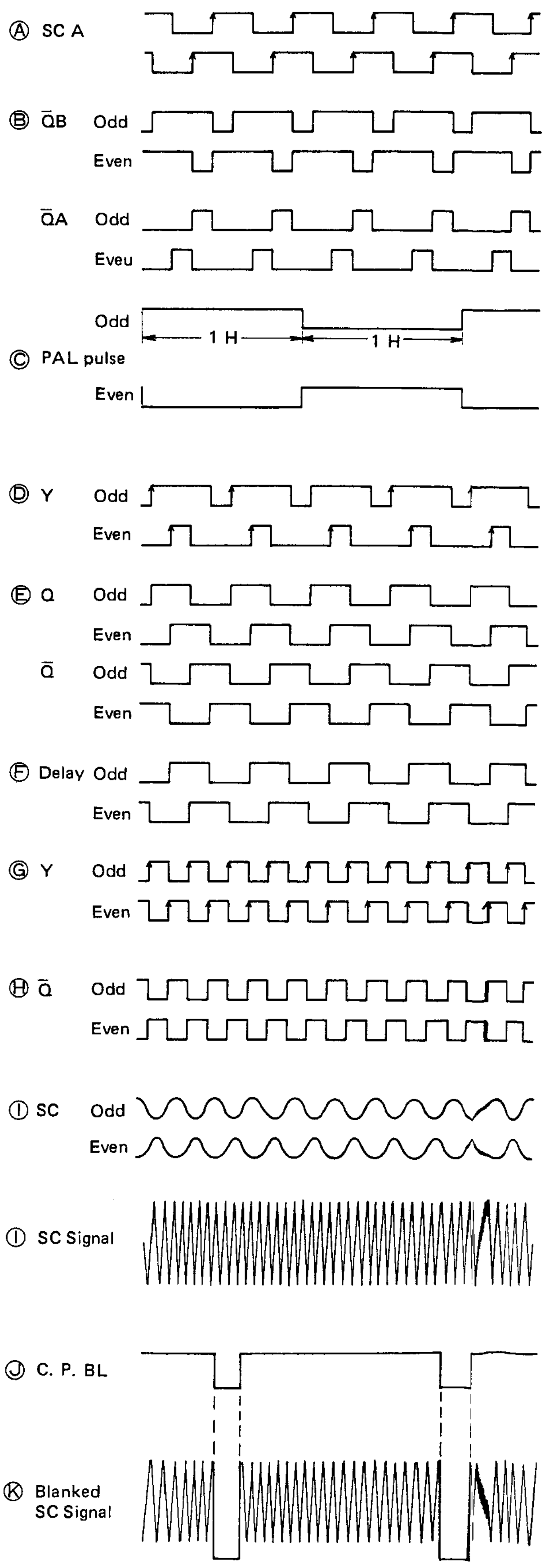

Ⓐ SC A
Ⓑ Q̄B
Odd
Even
Q̄A
Odd
Eveu
Odd
1 H
1 H
Ⓒ PAL pulse
Even
Ⓓ Y
Odd
Even
Ⓔ Q
Odd
Even
Q̄
Odd
Even
Ⓕ Delay
Odd
Even
Ⓖ Y
Odd
Even
Ⓗ Q̄
Odd
Even
Ⓘ SC
Odd
Even
Ⓘ SC Signal
Ⓙ C. P. BL
Ⓚ Blanked SC Signal

Fig. 2-1-2 SC signal

2-2. DSK Pulse Generator

Outline

This circuit produces DSK pulse consists of Q18-Q25.

Details

DSK video signal at pin 20 (b) of CN16 is supplied to clamp circuit Q18, where the blanking level of the DSK video signal is clamped by the clamp pulse fed to the gate of Q18 and the blanking level is set to the DC voltage at the drain of Q18.

The clamped DSK video signal Ⓐ is supplied to DSK amplifier consisting of Q20 and Q21, through buffer Q19, where the DSK signal is converted to DSK pulse Ⓑ.

Transistor Q72 is a DSK ON/OFF switching Transistor and the DSK ON/OFF control signal obtained at pin 10 (a) of CN16 is supplied to its base, therefore while DSK ON/OFF switch on the front panel is ON and high level is supplied to base of Q72, Q72 is OFF thus the DSK signal is supplied to Q21, however, when DSK ON/OFF switch is OFF and low level is supplied to base of Q72, Q72 is ON, thus the DSK signal is grounded and no signal is supplied to Q21.

VR1 (DSK LEVEL) sets the clamp level of DSK video signal by control the source voltage of Q18 and also sets the clip level of DSK pulse by control the cut off potential of Q21 through diode D1.

In order to prevent sync and burst signal of DSK signal form convert to DSK pulse, the DSK level is limited by D1.

The DSK pulse at emitter of Q22 is supplied to the pin 20 (a) of CN16 as DSK signal through phase shifter Q23, buffers Q24 and Q25, and gain control VR12 (DSK PULSE GAIN).

D2 is a level mutching diode between DSK pulse and input video signal.

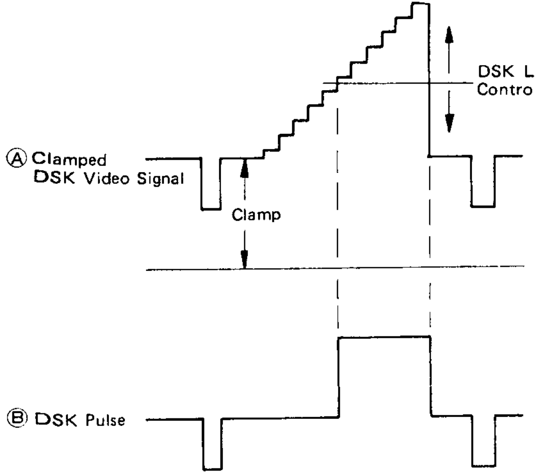


Fig. 2-2-1 DSK pulse

2-3. DSK Edge Generator Circuit

Outline

This circuit produces DSK edge signal form DSK pulse.

Details

The DSK pulse Ⓐ at emitter of Q22 and phase shifted DSK pulse Ⓑ at emitter of Q24 are sent to pin 5 and pin 6 of DSK edge generator circuit IC3 through buffer Q28 and inverter Q29, and buffer Q26 and inverter Q27 respectively.

IC3 is a exclusive OR gate, therefore, while input levels of pin 6 and pin 5 of IC3 become opposite polarity, high level appears at pin 4 of IC3. That is, while, phase of input DSK signal at pin 5 and pin 6 are shifted, corresponded pulse Ⓒ appears at pin 4 as edge signal and the edge signal is supplied to pin 19 (b) of CN16 through edge ON/OFF control transistor Q73.

While Edge ON/OFF switch SW2 on the DSK/BGD control is ON, edge ON/OFF control signal at pin 4 (a) of CN16 is supplied to base of Q73 and Q73 is ON. However, Edge ON/OFF switch is OFF, edge ON/OFF control signal is grounded and Q73 is OFF therefore edge signal is not supplied to pin 19 (b) of CN16. VR11 (DSK EDGE WIDTH) sets the DSK edge width by controlling the phase of DSK signal which is supplied to pin 6 of IC3.

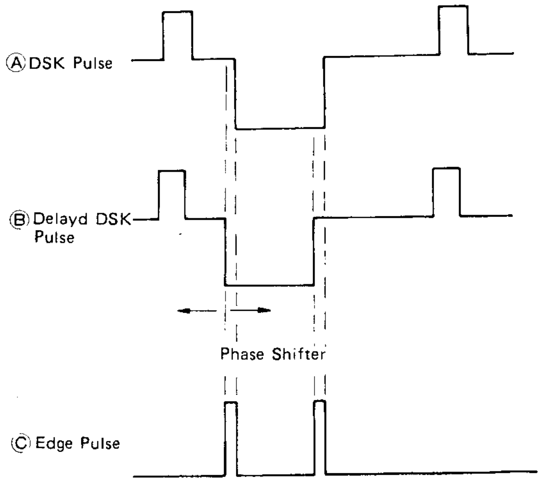


Fig. 2-3-1 Edge pulse

2-4. CH.PV-PG1-8/Effect Selector Circuit

Outline

This circuit selects the video signal from effect signal and PV-PG signal and the selected video signal is sent to the cut switching circuit on the output board.

Details

The effect signal at pin 8 (b) of CN16 is supplied to CH.PV-PG Effect chroma phase shifter circuit consisting of Q30, C40 and VR13 (EFFECT CHROMA PHASE), where the chroma phase of effect signal is matched to phase of internal color bar signal.

This signal is sent to switching transistor Q33 through buffer Q32.

Other hand, CH, PV-PG signal at pin 19 (a) of CN16 is supplied to CH, PV-PG 1-8 chroma phase shifter circuit consists of Q40, Q41, C45, C46, R100 and VR14 (PV-PG CHROMA PHASE), where the chroma phase of CH, PV-PG signal is matched to chroma phase of internal color bar signal.

This signal is supplied to switching transistor Q35 through buffer Q36.

While effect switch on the preview/program is OFF, pin 6 (a) of CN16 becomes low, therefore Q35 is ON and CH.PV-PG 1-8 video signal is obtained at pin 10 (b) of CN16 through buffer Q34.

When effect switch on the preview/program is ON, pin 6 (a) of CN16 becomes high, therefore Q33 is ON and effect video signal is obtained at pin 10 (b) of CN16 through buffer Q34.

2-5. C/8 - BGD Selector Circuit

Outline

This circuit selects the C/8 - BGD input signal for input selector boards by C/8, BGD selector.

Details

While C/8, BGD selector is set to C/8 position, high voltage (approx. 6V DC) is obtained at pin 5 (b) of CN16, so Q43 turns ON, thus video signal at pin 4 (b) of CN16 which is supplied from input connector 8 is sent to input selector.

When C/8, BGD selector is set to BGD position, pin 5 (b) of CN16 becomes low voltage, so Q43 is turned ON, thus vertical blanked SC signal which is produced in BGD, DSK color generator at emitter of Q12 is supplied to the input selector through buffer Q80.

2-6. VIS, Clamp Pulse Generator Circuit

Outline

This circuit contains vertical interval switching (VIS) pulse generator circuit consists of Q44-Q46 and clamp pulse (CP) generator circuit consists of Q47-Q49.

Details

- VIS pulse generator circuit

The negative vertical drive (VD) pulse Ⓐ is obtained at pin 18 (b) of CN16 is supplied to differential circuit consisting of C51 and R111 where the VD pulse is differentiated Ⓑ.

The differentiated signal is supplied to switching transistor Q44 and while differentiated signal becomes higher than threshold voltage of Q44 then ON, thus positive pulse Ⓒ is obtained at its emitter. This positive pulse is supplied to next differential circuit consists of C52 and R112, where the positive pulse is differentiated Ⓓ.

This differentiated signal is converted to negative VIS pulse Ⓔ by switching transistor Q45 and it is supplied to pin 18 (a) of CN16 through inverter Q46 as VIS pulse.

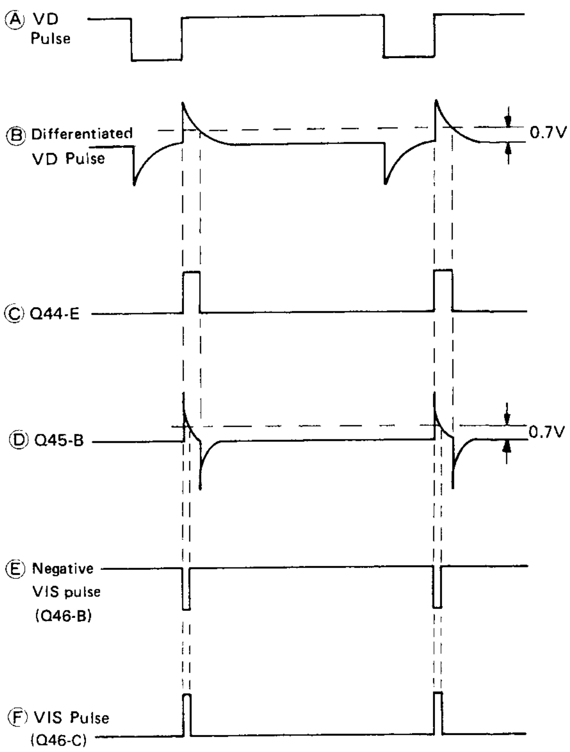


Fig. 2-6-1 V.I.S. pulse

- Clamp Pulse Generator Circuit

The negative composite sync signal Ⓐ obtained at pin 15 (b) of CN16 is fed through invertor Q47 to pin 15 (a) of CN16 as sync signal Ⓑ.

The sync signal at collector Q47 is also sent to differential circuit consists of R118 and C55, where the sync signal is differentiated Ⓒ.

The differentiated sync signal is converted to clamp pulse Ⓓ by Q48 and this clamp pulse is supplied to clamp circuit through buffer Q49.

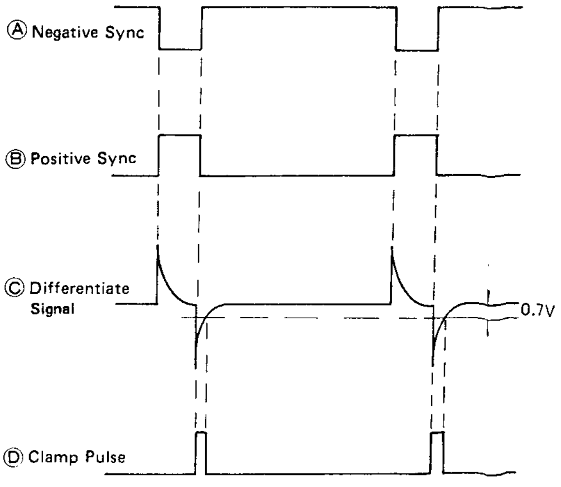


Fig. 2-6-2 Clamp pulse

2-7. Wipe Key Mat Key Signal Process Circuit

Outline

This circuit produces key signal for mat key and wipe key from input B video signal.

Details

The input video signal Ⓐ at pin 12 (b) of CN16 which is selected by input B selector is supplied to clamp circuit Q53 through buffer Q52, where the blanking level of the video signal is clamped by the clamp pulse fed to the gate of Q53 and the blanking level is set to the DC voltage at the drain of Q53.

C63 and L3 are added as filter to prevent the influence of burst signal when setting the pedestal clamp. The clamped video signal Ⓑ which chroma signal is reducted by chroma trap consists of C65 and L4 is supplied to key signal converter Q55 through buffer Q54,where the video signal is converted to key signal Ⓒ.

VR1 (DSK LEVEL) on the effect, mix board sets the pedestal level of the video signal by changing the source voltage of Q53, and also sets the clip level of key signal by changing the cut off potential of Q55 through D3.

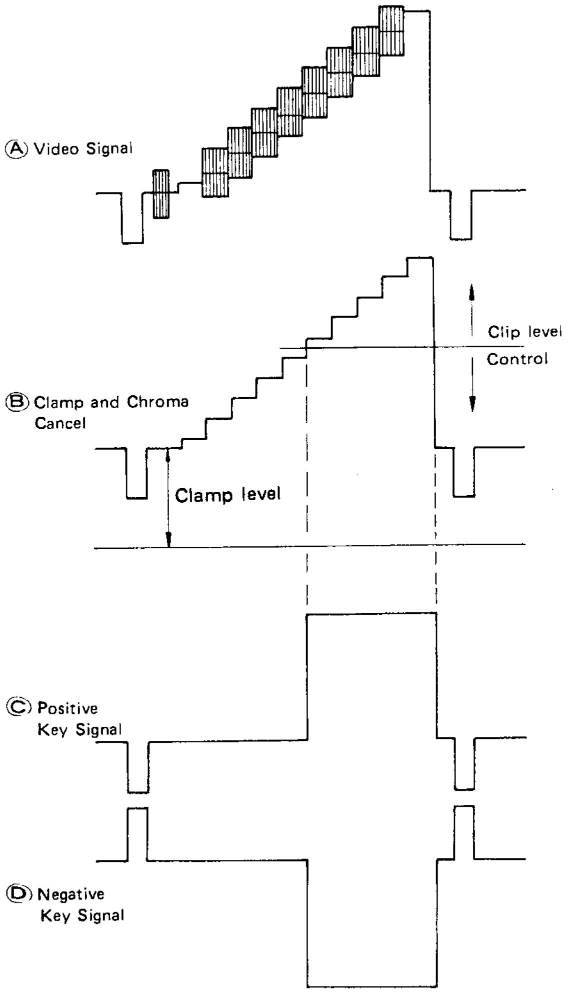


Fig. 2-7-1 Key signal

In order to prevent sync signal of video signal from convert to wipe signal, the key level is limited by D3. The key signal is supplied to differential amplifier consisting of Q57, Q58 and Q59 through buffer Q56 and D4.

The positive and negative key signal which obtained at collectors of Q57 and Q59 respectively are supplied to effect wave output circuit through NEG/POS switching circuit consisting of Q62 and Q63, buffer Q64 and level matching diode D5 and D6.

While key switch on the mat/border control is in POS position, low voltage appears at pin 9 (a) of CN16, so Q62 is turned ON, thus positive key signal is supplied to effect wave output select circuit.

Otherhand key switch is set to NEG postion, Q63 is turned ON and negative key signal Ⓓ is supplied to effect wave output select circuit.

2-8. Effect Wave Output Select Circuit

Outline

This circuit contains a mat key/chroma key switching circuit, a wipe/key switching circuit, a wipe key mixing circuit and a blanking mixing circuit.

This circuit selects the key signal or the wipe wave by the wipe/key control switches and the selected signal is supplied to wipe/mat key amplifier circuit on the effect mix board.

Details

- Mat Key/Chroma Key Switching Circuit

This circuit selects the key signal from mat key signal and chroma key signal, and is sent to next wipe key switching circuit.

- Wipe/Key Switching Circuit

This circuit selects key signal and wipe wave by switching the Q67.

- Non Amplitude Mixer (NAM) Circuit

This circuit consists of Q68-Q70, where the wipe wave and composite blanking signal are mixed with key signal. The effect wave output select circuit are functioned as followings.

1. Chroma Key Mode

   When chroma key button on the wipe/key control is depressed, MAT/CHROMA KEY CONT IN at pin 8 (a) and KEY/WIPE CONT IN at pin 14 (b) of CN16 becomes low and high level respectively therefore Q66 and Q67 are turned ON, thus chroma key signal at pin 6 (b) of CN16 is supplied to EFFECT WAVE OUT at pin 7 (b) of CN16 through NAM circuit.

2. Mat Key Mode
   When mat key button on the wipe/key control is depressed, pin 8 (a) and pin 14 (b) becomes high level, therefore, Q65 and Q67 are turned ON, thus mat key signal whose produced at wipe key, mat key signal process circuit is supplied to pin 7 (b) of CN16.
3. Wipe Key Mode
   When wipe key button on the wipe/key control is depressed, pin 8 (a) and pin 14 (b) of CN16 becomes high level, therefore Q65 and Q67 are turned ON, thus mat key signal appeard at NAM circuit.
   At this time WIPE WAVE appeard at pin 7 (a) of CN16, therefore, mat key signal and wipe wave are mixed at base of Q71 and is supplied to pin 7 (b) of CN16 as wipe key signal.
4. Wipe Mode
   When wipe button on the wipe/key control is depressed, pin 14 (b) becomes low level therefore Q67 is turned OFF, thus key signal is not appeard at NAM circuit.
   However, at this time only the wipe wave appeard at pin 7 (a) of CN16 and the wipe wave is supplied to pin 7 (b) of CN16through buffers Q69 and Q71.

3. Effect, Mix Board

The effect mix board contains following circuits.

3-1 Border, Mat Color Generator Circuit 16
3-2 CH.B/Mat Color Switching Circuit 17
3-3 Wipe/Mat Key Amplifier Circuit 17
3-4 Border Wipe Amplifier Circuit 19
3-5 Mix amplifier Circuit 20

3-1 Border, DSK Color Generator Circuit

Outline

This circuit consists a subcarrier (SC) generator circuit, blanking killer amplifier circuit and mat chroma phase shifter circuit.

This circuit produces border, mat color signal from SC A signal. Refer to 2-1 DSK, BGD color generator circuit on page 10.

Details

The 2.215MHz SC A pulse from pin 21 (a) of CN17 is supplied to B inputs of monostable multivibrator (M.M) at pin 2 of IC9 (a) and pin 10 of IC9 (b) respectively, then the rise timing of SC A pulse, negative pulse is obtained at QB and QA outputs of M.M at pin 4 of IC9 (a) and pin 10 of IC9 (b) respectively.

The width of output pulses at pin 4 of IC9 (a) and pin 12 of IC9 (b) is controlled by VR2 (HUE), and the VR2 is connected in series between pin 15 of IC9 (a) and pin 7 of IC9 (b) and +5V DC is supplied to center tap of VR2, therefore the width variation of individual outputs at pin 4 of IC9 (a) and pin 12 of IC9 (b) are inversed, because of the chroma phase of PAL color signal is 90 difference by each 1H line.

CT1 (HUE PRESET-1) and CT2 (HUE PRESET-2) set the chroma phase of Border and Mat color signal can be changed 380 by VR2 (HUE).

The negative pulses obtained at pin 4 of IC9 (a) and pin 12 of IC9 (b) are supplied to A and B input of analog switch at pin 2 and pin 3 of IC10 (a) respectively.

While G input at pin 15 of IC10 (a) is low level by the color ON/OFF switch SW1 on the Mat/Border control is ON, depending on the high level or low level of S input at pin 1 of IC10 (a) by PAL pulse, B or A input pulses are selected and the selected pulse appeared Y output at pin 4 of IC10 (a).

When Color ON/OFF switch SW1 is OFF, high level is supplied to G input at pin 15 of IC10 (a) through R21, therefore no output signal appeared Q and Q outputs at pin 13 and pin 4 of IC6 (a).

While S input is high level, B input pulse is obtained at Y output and S input is low level, A input pulse is obtained at Y output.

The Y output pulse is supplied to B input of M.M at pin 2 of IC7 (a) then the rise timing of B input pulse, positive pulse and negative pulse appeared Q and $\overline{Q}$ output at pin 13 and pin 4 of IC8 (a) respectively. VR6 (SC DUTY) is a control for adjusting the wave width of Q and $\overline{Q}$ output signals at pin 13 and pin 4 of IC8 (a) for fifty-fifty respectively.

The positive pulse and negative pulse obtained at pin 13 and pin 4 of IC8 (a) are supplied to A and B input at pin 2 and pin 3 of IC7 (a) respectively.

The positive pulse is also supplied to analog switch delay circuit consisting of IC7 (b), (c), (d) and IC10 (b), (c), (d) where the positive pulse is delayed approximately 90°, and the delayed pulse is supplied to S input at pin 1 of IC7 (a) as select signal.

While pin 1 of IC7 (a) is high level, input B pulse is obtained at Y output and when pin 1 of IC7 (a) is low level, input A pulse is obtained at Y output, as a result 2.215MHz input pulse is converted to 4.43MHz pulse and this pulse is supplied to B input at pin 10 of analog switch IC8 (b).

The rise time of 4.43MHz pulse, negative 4.43MHz pulse is obtained $\overline{Q}$ output at pin 12 of IC8 (b).

This 4.43MHz pulse is supplied to buffer Q1 through differential circuit consisting of C9 and R7.

The output signal of buffer Q1 is then supplied to phase shifter circuit consisting of Q2, C12 and VR6 (SUB CARRIER PHASE) through 4.43MHz band pass filter (B.P.F) F1, where the phase of SC signal is adjusted to specified SC signal by VR6.

The specified SC signal is supplied to pin 3 of differential amplifier IC1 through buffer Q9 and VR3 (SATURATION).

- Blanking killer amplifier

The DC voltage divided by R28 and R29 is supplied to pin 4 of IC1 as base bias of constant current transistor TR5 inside IC1.

The DC voltage divided by VR4 (LUMINANCE), R26, VR5 (LUMINANCE SETUP) and R27 is supplied to pin 10 of IC1 as base bias of constant current transistor TR6 inside IC1.

The DC voltage divided by R47, VR9 (BL KILLER DC BIAS) is supplied to pin 5 and pin 6 of IC1 as base bias of TR1 and TR4, and TR2 and TR3 inside IC1 respectively through buffer Q13.

The negative blanking (BL) signal obtained at pin 13 (b) of CN17 is supplied to pin 6 of IC1 through buffer Q10. Unless C.P. BL signal is supplied at pin 6 of IC1, TR2, TR3, TR5 and TR6 turns ON, therefore SC signal at pin 3 is obtained at pin 7 of IC1 through TR5 and TR2. However, when C.P.BL is supplied to pin 6 of IC1, TR1, TR4, TR5 and TR6 are turned ON, therefore SC signal is not obtained at pin 7 of IC1 and the blank level of SC signal is set with emitter potential of TR6, thus blanking periods of SC signal is eliminated, and blanked SC signal is produced.

This signal is supplied to mat chroma phase shifter circuit and border wipe amplifier circuit through mat/border DG, DP Q11 and buffer Q12.

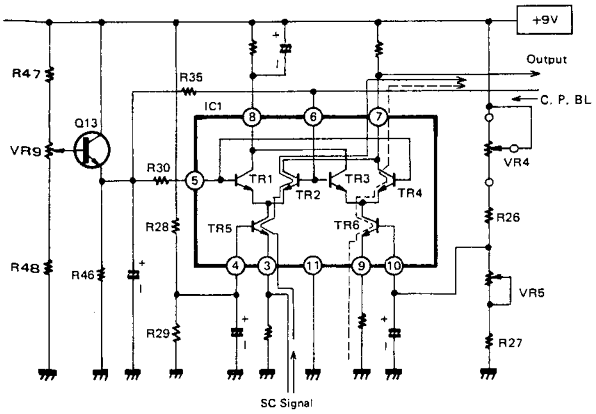


Fig. 3-1-1 Blanking killer amplifier circuit

- Mat chroma phase shifter circuit

This circuit consists of Q14-Q17, where the phase of blanked SC signal is controlled by VR10(MAT CHROMA PHASE) and it is supplied to CH.B/mat color switching circuit.

3-2 CH.B/Mat Color Switching Circuit

Outline

The mat chroma signal and CH.B video signal are selected by this circuit and selected signal is supplied to Wipe/mat key amplifier.

Details

When mat key button or wipe key button on the wipe/key control is depressed, MAT ON-OFF CONT IN at pin 10 (a) of CN17 becomes low level, therefore, Q54 is turned ON, thus met chroma signal from border mat color generator circuit is supplied to clamp circuit Q52 through buffer Q55.

However, when, chroma key button or wipe button is depressed, pin 10 (a) of CN 17 becomes high level, therefore Q53 is turned ON, thus CH.B video signal at pin 11 (b) of CN 17 which is selected by input B selector is supplied to clamp circuit Q52.

3-3 Wipe/Mat Key Amplifier Circuit

Outline

This circuit produces wipe/mat signal from CH.A video signal, convert with CH.B video signal or mat chroma signal, controlling by effect wave.

Details

The CH.A video signal at pin 5 (a) of CN 17 which is selected by input A selector is supplied to CH.A chroma phase shifter circuit consisting of Q43, where the chroma phase of CH.A video signal is matched to the chroma phase of CH.B video signal, controlled by VR29. The phase shifted CH.A video signal is supplied to the clamp circuit consists of Q44,where the blanking level of the CH.A video signal is clamped by the clamp pulse fed to the gate of Q44 and the blanking level is set to the DC voltage at the drain of Q44.

The clamped CH.A video signal Ⓐ is then supplied to pin 3 of wipe/mat key amplifier IC6 through buffers Q45 and Q46.

The CH.B video signal Ⓑ or the mat chroma signal Ⓒ selected in CH.B/mat color switching circuit is supplied to clamp circuit consists of Q52, where the blanking level of the CH.B video signal or the mat chroma signal is clamped by the clamp pulse fed to the gate of Q52 and the blanking level is set to the DC voltage at the drain of Q52.

The clamped signal is supplied to pin 9 of IC6 through buffer Q50 and Q51, and VR27 (CH.BGAIN).

VR28 (CH.B SETUP) sets the clamp level of the CH.B video signal or mat chroma signal to matching the pedestal level of CH.A video signal by changing the clamped potential.

The DC voltage divided by R145, R146 and VR25 (WIPE DC BIAS) is supplied to pins 5 and 6 of IC6 as base bias of TR1 and TR4, and TR2 and TR3 inside IC6 respectively through buffer Q49.

The effect wave such as wipe wave Ⓓ, wipe key signal Ⓔ, mat key signal Ⓕ and chroma key signal Ⓖ which is selected in the effect wave output selector circuit on the DSK, BGD board is supplied to pin 5 of IC6.

When depressed wipe button or chroma key button on the wipe/key control, wipe wave and chroma key signal appear at pin 5 of IC6 and CH.B signal appeard at pin 9 of IC6. When depressed the wipe key button or the mat key button, mat signal with wipe wave and mat signal appeard at pin 5 of IC6 and mat chroma appeard at pin 9 of IC6. While DC voltage of pin 6 higher than DC voltage of pin 5, TR2, TR3, TR5, and TR6 inside IC6 are turned ON, therefore signal at pin 9 is appeard at pin 8 fed to TR6 and TR3 inside IC6, however DC voltage of pin 5 becomes higher than DC voltage of pin 6 by effect wave signal, TR1, TR4, TR5 and TR6 are turned ON, therefore CH.A signal at pin 3 is appeard at pin 8 fed to TR5 and TR1 inside IC6, thus wipe/mat signal is produced.

The wipe/mat signal is then supplied to border wipe amplifier circuit through wipe/mat DG-DP Q48 and buffer Q47.

The switching noise is minimized by VR26 (WIPE EDGE SPIKE COMP) by controlling the collector bias of TR2 and TR4 inside IC6.

VR23 (EFFECT DG, DP-1) sets the DG, DP of wipe mat signal.

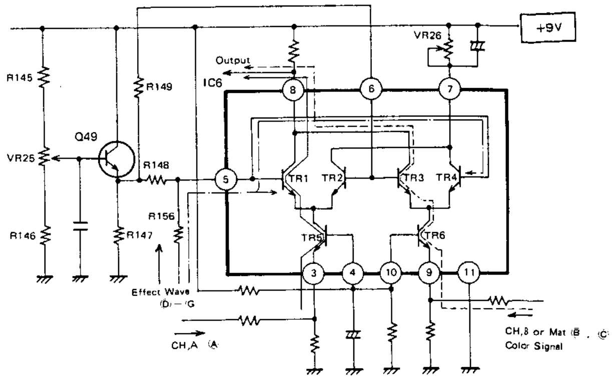

+9V
VR26
Output
IC6
R145
R149
Q49
VR25
R148
R156
R146
R147
TR1
TR2
TR3
TR4
TR5
TR6
8
6
7
5
3
4
10
9
11
Effect Wave
Ⓓ – Ⓖ
CH.A Ⓐ
CH.B or Mat Ⓑ, Ⓒ
Color Signal

Fig. 3-3-1 Wipe/Mat Key Amplifier

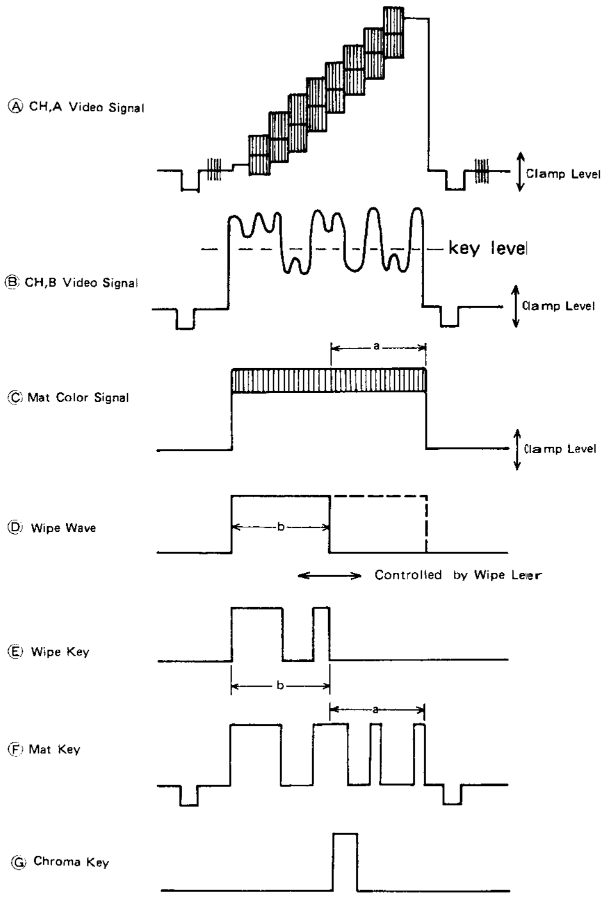

Ⓐ CH.A Video Signal
Clamp Level
Ⓑ CH.B Video Signal
key level
Clamp Level
Ⓒ Mat Color Signal
a
Clamp Level
Ⓓ Wipe Wave
b
Controlled by Wipe Lever
Ⓔ Wipe Key
b
Ⓕ Mat Key
a
Ⓖ Chroma Key

Fig. 3-3-2 Wipe/Mat signal

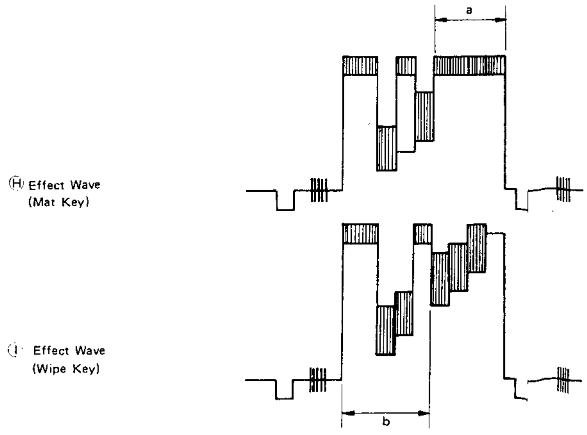

a
Ⓗ Effect Wave
(Mat Key)
Ⓘ Effect Wave
(Wipe Key)
b

Fig. 3-3-3 Effect wave

3-4 Border Wipe Amplifier Circuit

Outline

The border pulse is added on the switching edge of wipe/mat signal, and also border color is placed on the border pulse.

Details

The wipe/mat signal is supplied to clamp circuit consists of Q23 where the blanking level of wipe/mat signal is clamped by the clamp pulse fed to the gate of Q23 and the blanking level is set to the DC voltage at the drain of Q23.

The clamped wipe/mat signal Ⓐ is supplied to pin 3 of border wipe amplifier IC4 through buffers Q24 and Q25. The border color signal Ⓑ whose produced in border, mat color generator circuit is obtained at clamp circuit consists of Q32, where the blanking level of border color signal is clamped by the clamp pulse fed to the gate of Q32 and the blanking level is set to the DC voltage at the drain of Q32. VR20 (BORDER SETUP) sets the pedestal level of border color signal to same level as pedestal level of border pulse. The clamped border color signal is supplied to pin 9 of IC4 through buffers Q30 and Q31.

The DC voltage divided by R86, VR17 (BOPDER WIPE DC BIAS) and R87 is supplied to pins 5 and 6 of IC4 for base bias of TR1 and TR4, and TR2 and TR3 inside IC4 respectively through buffer Q29. The composite blanking pulse Ⓒ obtained at pin 13 (a) of CN 18 and border pulse Ⓓ obtained at pin 6 (a) of CN18 are mixed at BL/boarder mix circuit consisting of Q3 and Q4, and the mixed pulse Ⓔ is supplied to pin 5 of IC4.

While DC voltage at pin 5 is higher than DC voltage at pin 6, TR1, TR4, TR5 and TR6 are turned ON, therefore wipe/mat signal at pin 3 of IC4 is obtained at pin 8 of IC4 fed to TR5 and TR1 inside IC4, however, when DC voltage at pin 5 becomes lower than DC voltage at pin 6 by mixed pulse, TR2, TR3, TR5 and TR6 are turned ON therefore border color signal at pin 9 of IC4 is obtained at pin 8 of IC4 fed to TR6 and TR3 insde IC4, thus effect video signal Ⓕ is produced.

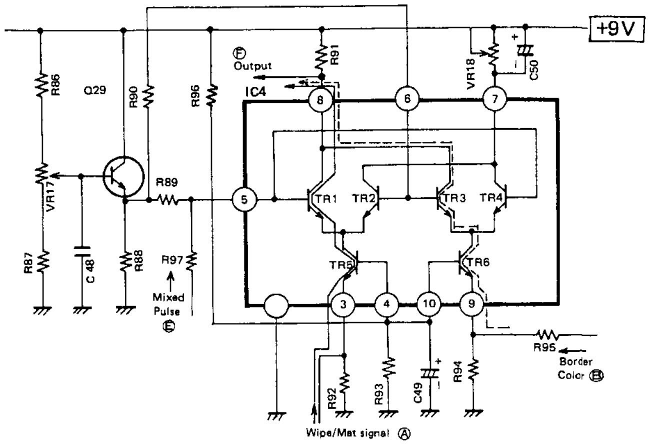

+9V
Ⓕ Output
IC4
R86
Q29
R90
R96
R91
VR18
C50
VR17
R89
TR1
TR2
TR3
TR4
TR5
TR6
R87
C48
R88
R97
Mixed Pulse Ⓔ
8
6
7
5
3
4
10
9
R95
Border Color Ⓑ
R92
R93
C49
R94
Wipe/Mat signal Ⓐ

Fig. 3-4-1 Border Wipe Amplifier

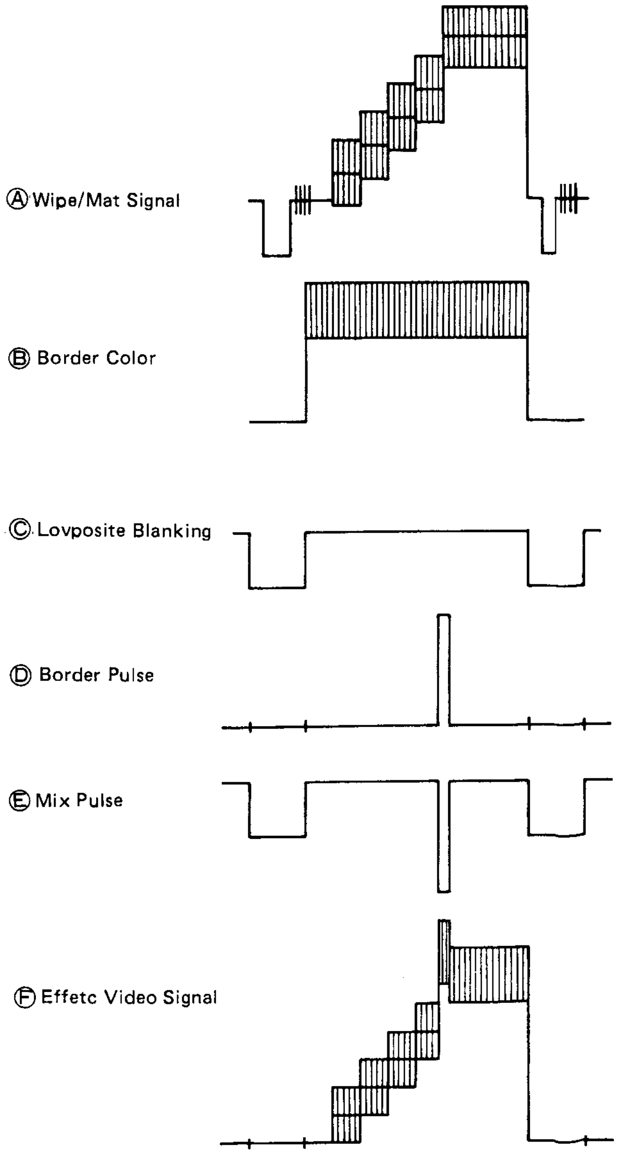

Ⓐ Wipe/Mat Signal
Ⓑ Border Color
Ⓒ Lovposite Blanking
Ⓓ Border Pulse
Ⓔ Mix Pulse
Ⓕ Effetc Video Signal

Fig. 3-4-2 Border Wipe Signal

The effect video signal obtained at pin 8 of IC4 is supplied to mix amplifier circuit and pin 8 of CN 17 through effect video DG, DP Q28 and buffer Q26. The switching noise is minimized with VR18 (BORDER EDGE SPIKE COMP) by controlling the collector bias of TR2 and TR4 inside IC4. VR15 (EFFECT DG. DP-2) sets the DG, DP of effect video signal. VR16 (EFFECT GAIN-2) sets the effect video gain for 1Vp-p.

3-5 Mix Amplifier Circuit

Outline

The CH.C video signal at pin 14 (a) of CN 17 whose selected by input C selector and effect video signal whose produced at border wipe amplifier circuit are mixed in mix amplifier circuit. The mix video signal is supplied to cut switching circuit on the output board.

Details

The effect video signal is obtained at clamp circuit Q22, where the blanking level of effect video signal is clamped by clamp pulse fed to the gate of Q22 and the blanking level is set to the DC voltage at the drain of Q22.

VR 14 (EFFECT SETUP) sets the clamp level of effect video signal for same level as clamp level of CH.C video signal.

The clamped effect video signal is supplied to pin 9 of effect fader amplifier IC3 through buffers Q20 and Q21, and VR13 (EFFECT GAIN-3).

The DC voltage divided by R58, R59, VR12 and VR11 (MIX DC BIAS-1) is supplied to pin 5 and pin 6 of IC3 as base bias of TR1 and TR4, and TR2 and TR3 inside IC3 respectively. The DC voltage controlled by EFFECT MIX LEVER is supplied to pin 5 of IC3 from pin 19 (a) of CN 17.

The DC voltage divided by R58, R59, VR11 and VR12 (MIX DC BIAS-2) is supplied to pins 4 and 10 of IC3 for base bias of constant current transistor TR5 and TR6 inside IC3 through buffer Q18.

The DC voltage at pin 5 of IC5 can be controlled by mix lever effect VR, and depending on the DC voltage at pin 5, mix wipe video signal whose obtained at pin 7 is changed.

While DC voltage at pin 5 is higher than DC voltage at pin 6, more current is fed to TR1 and TR4 inside IC3, therefore, much more effect video signal at pin 9 is obtained at pin 7, however, when DC voltage at pin 5 becomes lower than DC voltage at pin 6, more current is fed to TR2 and TR3 inside IC3, therefore effect video signal is not obtained at pin 7Ⓐ. This action can be variously effected as fade in/out function.

The other hand, CH.C video signal whose selected by input C selector is obtained at pin 14 (a) of CN 17 is supplied to CH.C chroma phase shifter circuit consists of Q39, Q40 and Q41, where the chroma phase of CH. C video signal is identical to chroma phase of effect video signal by controlling the VR22 (CH.C CHROMA PHASE).

The CH.C video signal is supplied to clamp circuit consists of Q37 through buffer Q38, where the blanking level of CH.C video signal is clamped by clamp pulse fed to gate of Q37 and blanking level is set to the DC voltage at the drain of Q37. The clamped CH.C video signal is supplied to pin 9 of IC5 through buffers Q36 and Q35, and VR30 (CH.C GAIN). The DC voltage divided by R58, R59, R11 and R12 which is supplied to pin 4 and pin 10 of IC3 is also supplied to pin 4 and pin 10 of IC5 for base bias of constant current transistors TR5 and TR6 inside IC5 through buffer Q18. The DC voltage divided by R58, R59, VR11 and VR12, which is supplied to pin 5 and pin 6 of IC3 is also supplied to pin 5 and pin 6 of IC5.

The DC voltage at pin 6 of IC5 can be controlled by mix lever CH.C VR and depending on the DC voltage at pin 6 of IC5, CH.C video signal whose obtained at pin 7 of IC5 is changed.

While DC voltage at pin 6 is higher than DC voltage at pin 5, more current is fed to TR2 and TR3 inside IC5, therefore CH.C video signal is not obtained at pin 7 of IC5, however when DC voltage at pin 6 becomes lower than DC voltage at pin 5, more current fed to TR1 and TR4 inside IC5, therefore much more CH.C video signal is obtained at pin 7 of IC5Ⓑ.

This action can be variously effected as fade out/in function.

When mix lever CH.C VR and mix lever effect VR are moved to simultaneously in same direction, fade in and fade out function of effect fader amplifier IC3 and CH.C fader amplifier IC5 are taken reverce order, therefore both effect video signal and CH.C video signal are mixed at emitter of Q34, corresponding to the position of mix leverⒸ.

The mixed video signal is supplied to cut switching circuit on the output board through mix DG, DP Q34, buffer Q33 and pin 17 (a) of CN 17.

VR21 (MIX DG DP) sets the DG, DP of mix signal.

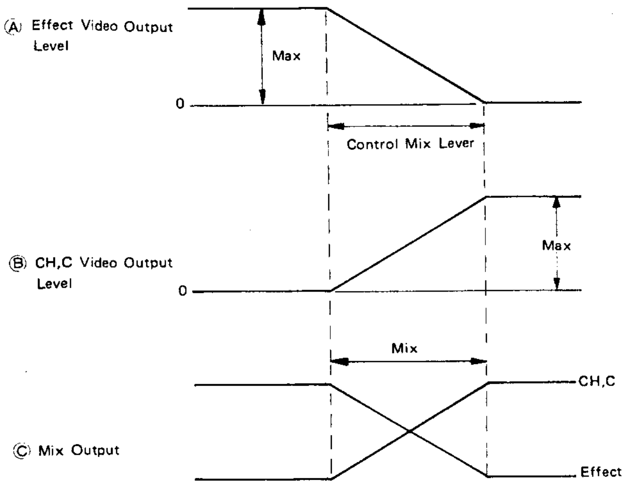


Fig. 3-5-1 Mixed signal

4. Chroma Key Board

The chroma key board contains following circuits.

4-1. Wipe, Key Control Circuit 21
4-2. Chroma Key Generator Circuit 21

4-1 Wipe, Key Control Circuit

Outline

The control signal such as key control signal, key/wipe control signal, wipe ON-OFF control signal, key pulse control signal or chroma key control signal is produced at the wipe, key control circuit by the corresponding to the selected wipe/key control button and the control signal is supplied to the each of input A and B select board, DSK, BGD board, wipe process board and effect mix board.

Details

When power switch of WJ-5600 is turned ON and +9V DC is obtained wipe, key control circuit, momentally C3 is turned ON, therefore the reset terminals of each D flip-flop inside IC2 become low level and each Q and $\bar{Q}$ outputs are set to low level and high level respectively. The V IS pulse is supplied at pin 2 of AND gate IC1 (a) because since this pulse is obtained at AND gate and one of wipe/key control button is depressed, the switching is made in vertical interval (during vertical blanking) and the switching noise is invisible. When wipe button is depressed, high level is obtained at data (D) input pin 4 and clock (C) input pin 9 of D flip-flop IC2 (a).
As a result, Q and $\bar{Q}$ output become high level and low level respectively.
The high level at Q output is supplied to base of Q1 and turns Q1 ON, thus wipe indicator lamp is illuminated.
This condition is kept until next clock pulse is enterd to clock terminal of IC1 (a) by depressing other button.
The +9V DC is supplied seriesly through switches, therefore, left side (wipe) have priolity when depress more two button simultaneously.
$\bar{Q}$ outputs of D flip-flop of IC2 (b), IC2 (c) and IC2 (d) are supplied to AND gates IC1 (c) and IC1 (b) respectively, and when power switch of WJ-5600 is turned ON or wipe button is depressed, $\bar{Q}$ outputs are high level therefore output of AND gates at pin 11 and pin 10 are high level however, when one of wipe key, mat key or chroma key button is depressed, $\bar{Q}$ output becomes low level, thus output of AND gates becomes low level.
The each control signal corresponding to the wipe/key control button shows table 4-1-1.

	ON				OFF
	WIPE	WIPE KEY	MAT KEY	CFROMA KEY	
KEY CONT OUT (4a,b)	H	L	L	L	L
KEY/WIPE CONT OUT (7a,b)	L	H	H	H	H
WIPE ON-OFF CONT OUT (8a,b)	H	H	L	L	H
MAT ON-OFF CONT OUT (9a,b)	H	L	L	H	H
MAT CHROMA KEY CONT OUT (10a,b)	H	H	H	L	H

Table 4-1-1 Control signal

4-2 Chroma Key Generator Circuit

Outline

This circuit contains buffer circuits, a mix circuit, a hue (color phase) selector circuit, clamp circuits, a differential amplifier circuit, a clip circuit, a delay circuit and output circuit. This circuit produces chroma key signal from R.G.B. input signal and the chroma signal is supplied to mat key/chorma key switching circuit on the DSK, BGD board.

Details

- Buffer circuit

The Blue (B)Ⓐ, Red (R)Ⓑand Green (G)Ⓒsignals at pin 22, pin 20 and pin 18 are supplied to buffer Q17 Q16 and Q15 respectively.
Then they are supplied to mixing circuit and hue selector circuit individually.

- Mixing circuit

The output of buffer transistors Q17, Q16 and Q15 are mixed at base of Q14 through matrix resistor R37, R36 and R35 respectivelyⒹ.

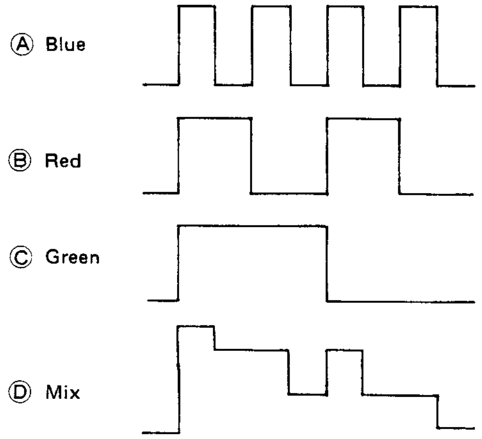


Fig. 4-2-1 R. G. B Mix signal

- Hue selector circuit

The R.G. and B signals from buffer Q17, Q16 and Q15 are also supplied to the corresponded terminal of hue selector VR3 (HUE) respectively, and a desired hue signal is taken out at pin 1 of CN2.

- Clamp circuit

The chroma key circuit has three clamp circuits as each consisting of Q13, Q7 and Q18.

The blanking level of mixed signal or hue signal is clamped by the clamp pulse fed to the gates of FET Q13 and Q7 and the blanking level is set to the DC voltage at the drain of Q13 and Q7 respectively.

The source of FET Q13 and Q7 are commonly connected to ground through R31, therefore, each of feeding mixed signal and selected hue signal are clamped with same level respectively for specified operation level of differential amplifier circuit for next stage.

The other clamp circuit consisting of Q18 clamps the blanking level of differentiate key signal by the clamp pulse fed to the gate of Q18 and the blanking level is set to the zenner voltage of D6 (+4V DC).

- Differential amplifier circuit

The clamped mix signal and clamped hue signal are supplied to the differential amplifier circuit consists of Q9-Q11 through buffers Q12 and Q8 respectively. The emitters of Q11 and Q9 are connected with collector of Q10 through R27 and R26, and base of Q10 is connected to constant current diode D5, collector current of Q10 is constant, thus the output of collector Q11 becomes the differentiated signal of mix signal and hue signal Ⓔ-Ⓙ.

Due to the above operation, brightness and constant components of image are neglected from the key signal, therefore no effects occurred when black and white picture is obtained.

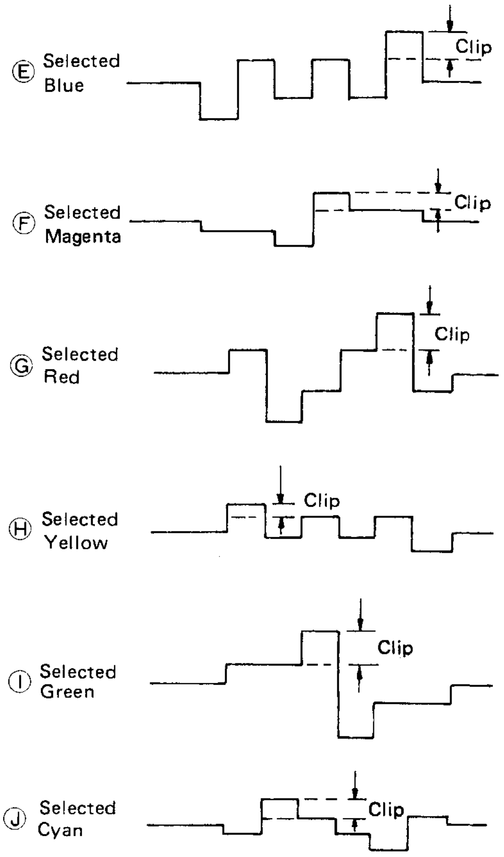


Fig. 4-2-2 Selected signal

- Clip circuit

The clamped differentiate signal at drain of Q18 is supplied to base of Q20 through buffer Q19. The DC voltage divided by R16, R17 and VR2 (LEVEL) is supplied to base of Q21. The emitters of Q20 and Q21 are connected via R51, therefore emitter potential of Q20 is controlled by controlling the emitter potential of Q21. Thus, when the emitter potential of Q20 is lower than the threshold voltage of Q20, turn Q20 ON, the clipped output signal is fed out from emitter follower Q22 through Q21.

- Delay circuit

The clipped key signal is supplied to delay circuit consisting of DL1, Q23, Q24 and VR1 (DELAY), where the phase of key signal is matched to the mat chroma signal by controlling VR1, due to chroma key signal and mat chroma signal is mixed on the effect, mix board. The key signal is fed to delay line L1 for 350 nsec delay and it is supplied to the phase shifter circuit thus the key signal is delayed totally about 500 nsec.

- Output circuit

The output signal of delay circuit is supplied to pin 12 of CN 18 through buffer Q25, output amplifier Q26 and buffer Q27.

5. Input A, B and C Board

The Input A, B and C board contains following circuits.

5-1. Vertical Interval Switching (V.I.S.) Circuit . . . 23
5-2. Tally and Pilot Lamp Control Circuit 23
5-3. Video Switching Circuit 24

5-1. Vertical Interval Switching Circuit

Outline

Input A, B and C board switch the video input A, video input B and video input C in the vertical interval switching (V.I.S.) duration.

The switching is made in vertical interval and switching noise is invisible.

Details

When the power switch of WJ-5600 is turned ON, +9V DC is supplied, and C1 is turned ON, then the reset terminals of each D flip-flop inside IC4 and IC5 become low level and each Q and $\bar{Q}$ output terminals are set to low level and high level respectively.

The V.I.S.pulse Ⓐ is supplied to pin 6 of AND gate IC2 (a) from pin 6 (b) of CN19. The output of an OR gate from D10 to D17 signal selected by input selector switches of 1 to 8 is obtained at pin 5 of IC2 (a). When switch 1 is depressed, high potential of anode of D10 is applied to pin 5 of IC2 (a) and at the same time pin 4 of IC4 (a) becomes high level Ⓑ. Within this period of time, the V.I.S. pulse goes to pin 9 of IC4 through pin 4 of IC2 (a) as the clock pulse Ⓒ. Since all D inputs are low level except pin 4 of IC4 (a), the output of flipflop at pin 2 of IC4 (a) becomes high level Ⓓ and all other outputs remain low level.

This condition is kept until next clock pulse is applied to clock terminal of IC4 or IC5 by depressing other input selector switch.

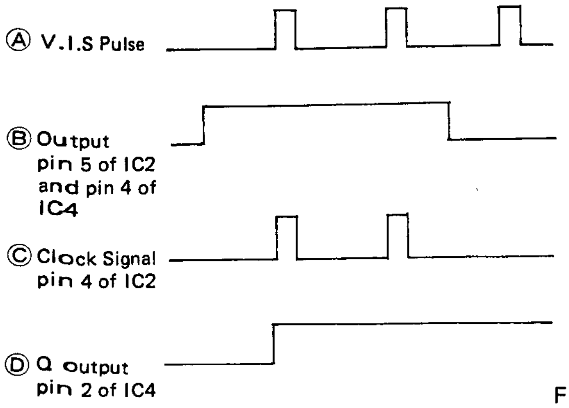

Ⓐ V.I.S Pulse
Ⓑ Output pin 5 of IC2 and pin 4 of IC4
Ⓒ Clock Signal pin 4 of IC2
Ⓓ Q output pin 2 of IC4

Fig. 5-1 Flip-flop

5-2. Pilot and Tally Lamp Control Circuit

Outline

This circuit controls the input selector pilot lamp as when the selected input video is sent to PROGRAM OUT, the pilot lamp for selected input selector bright fully. When input video is not sent to PROGRAM OUT, the pilot lamp for selected input selector turns gloomy. Also the tally lamp control signal is supplied to the selected input camera for camera tally lamp.

Details

When the input selector switch 1 is depressed, Q output pin 2 of IC4 (a) becomes high level, thus Q20 is switched ON to light up the number 1 input selector pilot lamp. The emitters of the pilot lamp ON/OFF control Q20 to Q27 are grounded through R48.

The control signal for Q28 is supplied from the micro switch of WIPE and MIX lever through Q2, Q1 and pin 5, pin 4 of IC3 (b). Pin 3 of AND gate IC3 (b) is high level except when cut switch or effect switch is selected on the PREVIEW/PROGRAM input selector. The level at pin 6 of AND gate IC3 (b) becomes high level only when input pin 3, pin 4 and pin 5 of AND gate IC3 (b) levels are high, and then this high level turns Q28 ON to bright the pilot lamp fully.

When one of the input signal level at pins 3, 4 and 5 of AND gate IC3 (b) is low level, Q28 is switched OFF to turn the pilot lamp gloomy by means of the resister R48.

The high level signal at pin 2 of IC4 (Q output) is also supplied to pin 5 of IC1 (AND-gate). At this time, if pin 6 of IC3 output is high level, output at pin4 of IC1 (AND gate) becomes high level. This signal is supplied to the tally/intercom connector on rear panel through diode D1 and Connector board for tally lamp control of selected camera.

TRUTH TABLE OF D FLIP-FLOP

CLOCK^t	DATA	RESET	Q
↑	L	H	L
↑	H	H	H
↓	X	H	Q
X	X	L	L

X—means either L or H, "Don't care" condition.
t —means level change

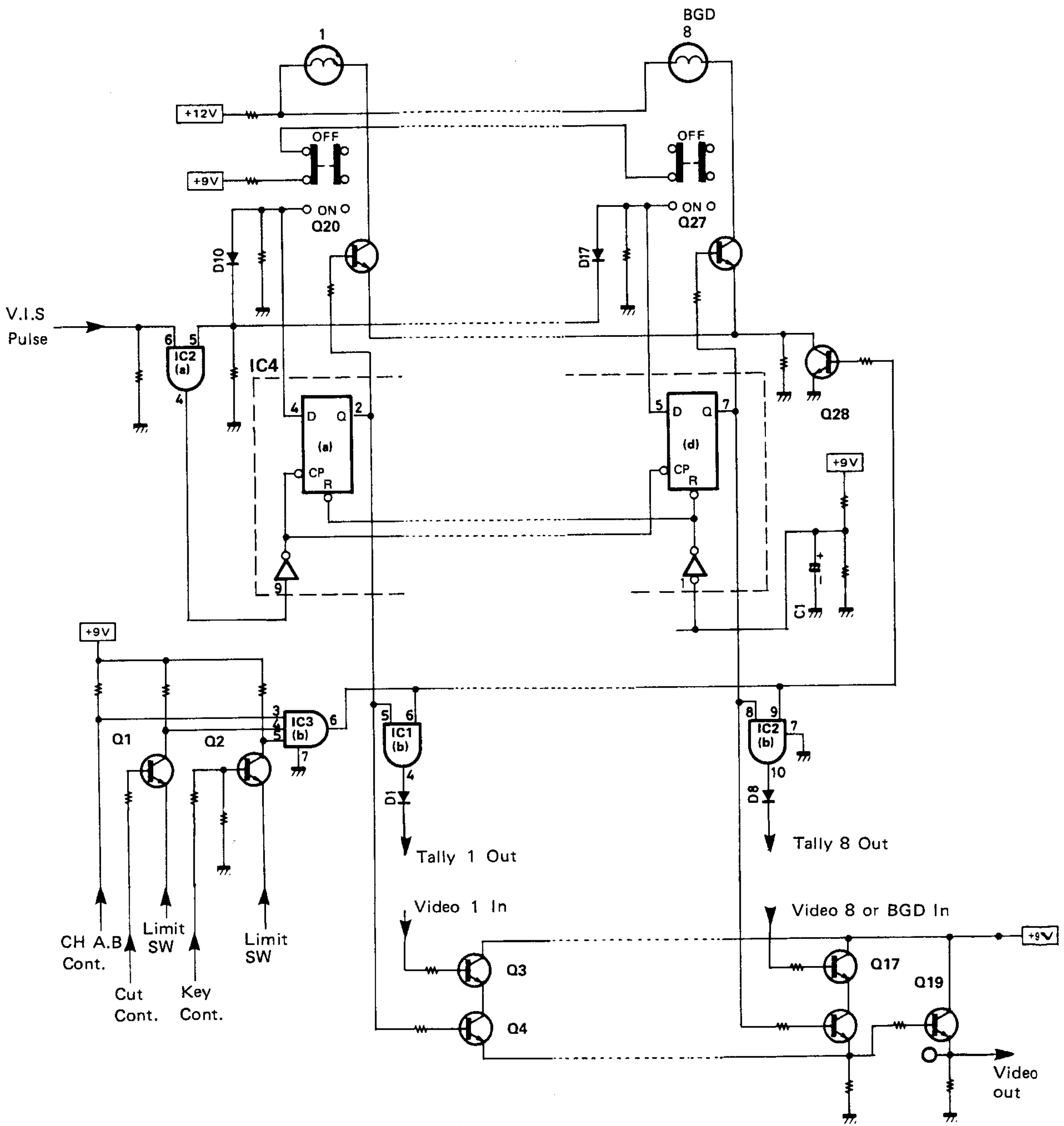

1
BGD
8
+12V
OFF
+9V
ON
Q20
Q27
D10
D17
V.I.S
Pulse
IC2 (a)
IC4
D Q
(a)
CP
R
(d)
Q28
+9V
C1
+9V
IC3 (b)
IC1 (b)
IC2 (b)
Q1
Q2
D1
D8
Tally 1 Out
Tally 8 Out
Video 1 In
Video 8 or BGD In
CH A.B Cont.
Limit SW
Cut Cont.
Key Cont.
Limit SW
Q3
Q4
Q17
Q19
+9V
Video out

Fig. 5-2 Video input circuit

5-3. Video Switching Circuit

Outline

This circuit receives the 8 input video signals from video input connector on rear panel through connector board. Then input video signals are selected in the video switching circuit and one of selected video signal is sent to the Effect, Mix board.

Details

The video input signal of video 1 to video 8 is supplied to the base of switching transister Q3, Q5, Q7, Q9 Q11, Q13, Q15 and Q17 from video input connectors respectively. When input selector switch 1 is depressed, the potential at base of Q4 becomes high level and Q4 is turned ON. As a result, video input signal video 1 is supplied to the Effect, Mix board through switching Q3 and Q4 and buffer Q19. The all others operation of input video switching circuit are same.

6. Input PV-PG Board

The Input PV-PG board contains following circuits.

6-1. Vertical Interval Switching (V.I.S.) Circuit. . . . 25
6-2. Tally and Pilot Lamp Control Circuit 25
6-3. Video Switching Circuit 25
6-4. Cut Control Circuit 26
6-5. Effect, DSK Control Circuit 26

6-1. Vertical Interval Switching (V.I.S.) Circuit

Outline

Input PV-PG board switches the video input signal in the vertical interval switching (V.I.S.) duration. This switching is made in vertical interval and switching noise is invisible.

Details

When the power switch of WJ-5600 is turned ON, +9V DC is supplied, and C2 is turned ON, then the reset terminals of each D flip-flop inside IC5 and IC6 become low level and each Q and $\bar{Q}$ output terminals are set to low level and high level respectively.

The V.I.S. pulse is supplied to pin 13 of AND gate IC2 (d) from pin 21 (b) of CN22. The output of an OR gate from D9 to D18, signal selected by input selector switches of 1 to 8, EFF and DSK is obtained at pin 12 of IC2 (d). When switch 1 is depressed, high potential at anode of D9 is applied to pin 12 of IC2 (d) and at the same time pin 3 of IC5 (a) becomes high level. Within this period of time, the V.I.S. pulse is supplied to pin 9 of IC5 through pin 11 of IC2 (d) as the clock pulse. Since all D inputs are low level except pin 3 of IC5 (a), the output of flip-flop at pin 2 of IC5 (a) becomes high level and all other outputs remain low level.

This condition is kept until next clock pulse is applied to clock terminal of IC5 or IC6 by depressing other input selector switch.

6-2. Pilot and Tally Lamp Control Circuit

Outline

This circuit controls the input selector pilot lamp as when the selected input video is sent to PREVIEW OUT, the pilot lamp for selected input selector turns gloomy. When selected input video is sent to PROGRAM OUT, the pilot lamp for selected input selector bright fully. Also the tally lamp control signal is supplied to the selected input camera for camera tally lamp.

Details

When the input selector switch 1 is depressed, Q output pin 2 of IC5 (a) becomes high level, thus Q21 is switched ON to light up the number 1 input selector pilot lamp. The emitters of the pilot lamp ON/OFF control Q21 to Q30 are grounded through R53.

The control signal for Q31 is supplied from cut switch through IC7 and IC4 (c). When the cut switch is OFF, the potential at pin 10 of inverter IC4 becomes low level. This low level turns OFF Q31 to dim the brightness of the pilot lamp. However when the cut switch is ON, the potential at pin 10 of IC4 becomes high level and Q31 is switched ON to bright the brightness of the pilot lamp.

The high potential at pin 2 of IC5 (a) is also supplied to pin 2 of AND gate IC1 (a). At this time, if the cut switch is ON and the potential at pin 2 of IC7 is high level, the output at pin 3 of AND gate IC1 (a) becomes high level. This signal is supplied to the tally/intercom connector on rear panel through D1 for tally lamp control of selected camera.

6-3. Video Switching Circuit

Outline

This circuit receives the 8 input video signals from video input connector on rear panel through connector board. The input video signals from 1 to 8 are selected in the video switching circuit and selected video signal is sent to the DSK, BGD board. However no video signal is sent when EFF or DSK switch is selected.

Details

The video input signal of video 1 to video 8 is supplied to the base of video switching transister Q2, Q4, Q6, Q8, Q10, Q12, Q14 and Q16 from video input connectors respectively.

When input selector switch 1 is depressed, the potential at base of Q1 becomes high level and Q1 is turned ON. As a result, video input signal of video 1 is supplied to the DSK, BGD board through switching Q2 and Q1 and buffer Q19. However, when EFF or DSK input selector switch is depressed, the potential at base of Q17 becomes high level and switching transistor Q17 is turned ON. Therefore DC voltage divided by R17 and R19 is supplied to the DSK, BGD board through Q17, Q18 and Q19 for prevention of crosstalk.

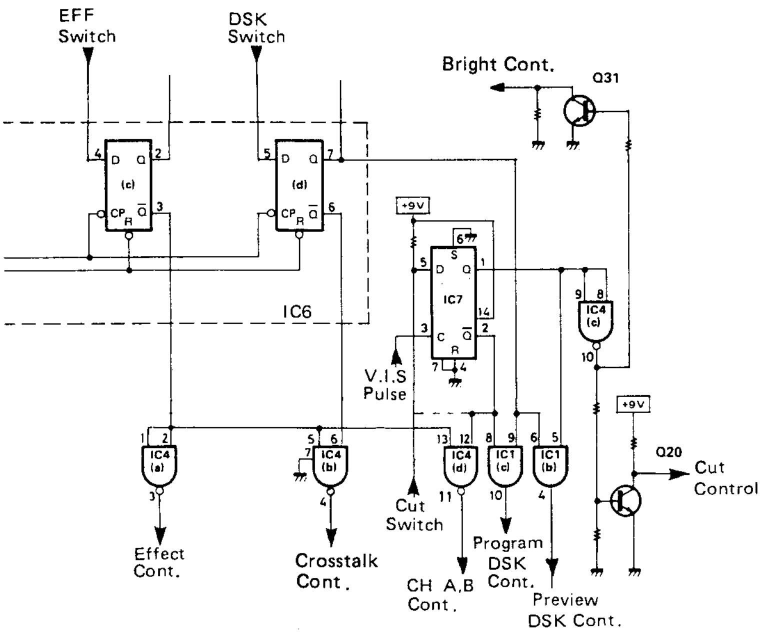


Fig. 6-1 Control circuit

6-4. Cut Control Circuit

Outline

This circuit receives control information from cut switch and sends the control signal to the base of Q31, the pilot and tally lamp control circuit on the Input A, B and C boards, and the program and preview/DSK switching circuit on the Output board through connector CN22.

Details

The potential at pin 5 of IC7 is controlled by CUT ON/OFF switch. While Cut switch is OFF, the potential at D input pin 5 of IC7 is high level. So that the Q output at pin 1 of IC7 becomes high level and high level is supplied into NAND gate pin 8 and pin 9 of IC4 and also to AND gate pin 5 of IC1 .

Low level of a NAND gate output at pin 10 of IC4 is supplied to base of Q31 and turned it OFF (refer to 5-2 on page 23). Also this NAND gate output is supplied to base of cut control output Q20 and turned it OFF, therefore cut control output potential at collector of Q20 becomes high level.

When Cut switch is ON, the potential at D input pin 5 of IC7 is low level. Therefore Q31 and Q20 are turned ON and low level cut control output potential at collector of Q20 is obtained.

6-5. Effect, DSK Control Circuit

Outline

This circuit supplies CH A, B tally control signal, Program output DSK control signal, Preview output DSK control signal and Effect control signal to Input A, Input B board and Output board corresponding to CUT switch, EFF and DSK switches on Input PV-PG board.

Details

The NAND gate IC4 (b) supplies CH A, B tally control signal to Input A and Input B board for pilot and tally lamp ON/OFF control.

The input signal at pin 12 of IC4 (d) is supplied from $\bar{Q}$ output at pin 2 of IC7, and this potential is controlled by Cut ON/OFF switch. While Cut switch is OFF, $\bar{Q}$ output potential at pin 2 of IC7 is low level, when Cut switch is ON, $\bar{Q}$ output potential at pin 2 of IC7 is high level.

The another input signal at pin 13 of IC4 is supplied from $\bar{Q}$ output at pin 3 of IC6, and this potential is controlled by EFF switch on the Input PV-PG board. Ordinary $\bar{Q}$ output potential at pin 3 of IC6 is high level except when the EFF switch is depressed. Therefore the NAND gate output potential at pin 11 of IC4 is supplied always high potential to the Input A and Input B board when EFF switch is ON, also when EFF switch and CUT switch are OFF. However when EFF switch is OFF and CUT switch is ON, the input potential at pin 12 and pin 13 of IC4 become high level. Therefore output potential at pin 11 of IC4 becomes low level and low level is supplied to the Input A and Input B board.

The AND gate IC1 (b) is supplied DSK ON/OFF control signal to the preview output circuit on OUTPUT board. The input signal at pin 5 of IC1 is supplied from Q output at pin 1 of IC7, and this potential is controlled by Cut ON/OFF switch. The another input signal at pin 6 of IC1 is supplied from Q output at pin 7 of IC6, and this potential is controlled by DSK switch on the Input PV-PG board. Ordinary Q output potential at pin 7 of IC6 is low level except when the DSK switch is depressed on Input PV-PG board. Therefore the AND-gate output potential at pin 4 of IC1 is low level when Cut switch ON, and this low level is supplied to preview output circuit on OUTPUT board. However when Cut switch is OFF and the DSK switch on the Input PV-PG board is depressed, the potential at pin 4 of IC1 becomes high level and this high level is supplied to the preview output circuit on OUTPUT board.

The AND gate IC1 (c) supplies DSK ON/OFF control signal to the program output circuit on the OUTPUT board. The input signal at pin 8 of IC1 is supplied from $\bar{Q}$ output at pin 2 of IC7. The another input signal at pin 9 of IC1 is supplied from Q output at pin 7 of IC6. Therefore the AND gate output potential at pin 10 of IC1 is low level except when CUT switch is ON and DSK switch is depressed on the Input PV-PG board, and this potential is supplied to the program output circuit on the OUTPUT board.

7. Wipe Process Board

The Wipe Process board contains following circuits

7-1. Vertical Interval Switching and Pilot Lamp Control Circuit 27

7-2. Vertical Wipe Wave Process Circuit 28

7-3. Horizontal Wipe Wave Process Circuit 29

7-4. Normal/Reverse Control Circuit 30

7-1 Vertical Interval Switching and Pilot Lamp Control Circuit

Outline

Wipe Process board contains the Normal/Reverse selector switch, the Wipe mode selector switch, and the Modulation ON/OFF switch, and switches the video signal within the vertical interval switching (V.I.S.) duration .

This circuit is similar with Input A, Input B, Input C and Input PV-PG board.

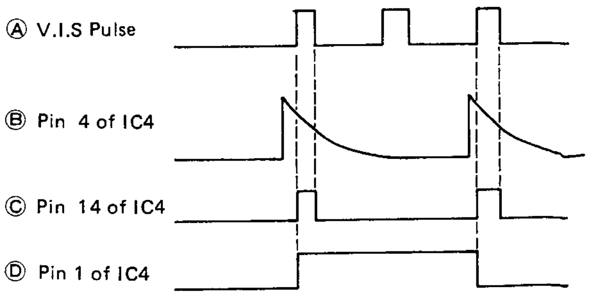
Details

When the power switch of WJ-5600 is turned ON, +9V DC is supplied, and C1 is turned ON, then the reset terminals of each D flip-flop inside IC2 become low level and each Q and $\bar{Q}$ output terminals are set to low level and high level respectively.

The V.I.S. pulse is supplied to pin 2 of AND gate IC1 (a) from pin 13 (b) of CN23. The output of an OR gate from D1 to D3 signal selected by Normal/Reverse selector switches of NORM, REV and NORM-REV is obtained at pin 12 of IC 1(a). When NORM switch is depressed, high potential at anode of D1 is applied to pin 12 of IC1 (a) and at the same time pin 5 of IC2 (a) becomes high level. Within this period of time, the V.I.S. pulse is supplied to pin 9 of IC2 through pin 11 of IC1 (a) as the clock pulse. Since all D inputs are low level except pin 5 of IC2 (a), the output of flip-flop at pin 7 of IC2 (a) becomes high level and all other outputs remain low level. This condition is kept until next clock pulse is applied to clock terminal at pin 9 of IC4 by depressing other normal/ reverse selector switch.

The V.I.S pulse also supplied to pin 13 of IC (b) and Wipe Mode Selector switches SHARP, SOFT and BORDER switch are switched within vertical interval.

The V.I.S. pulseⒶ is also suppied to pin 12 of J-K flip-flop IC4. When the modulation (MOD) ON-OFF switch is depressed, the potential at pin 9 of IC4 becomes high level Ⓑ. At this time, the V.I.S. pulse obtained at $\bar{Q}$ output at pin 14 of IC4 Ⓒ is supplied to C input at pin 3 of IC4. The potential at Q output at pin 1 of IC4 is changed by each rising timing of C inputⒹ. Therefore when the modulation (MOD) ON-OFF switch is depressed, Q output at pin 1 of IC4 becomes high level, and when the modulation switch is depressed again Q output at pin 1 of IC4 becomes low level.



TRUTHTAELE

INPUTS						OUTPUTS'	
C^t	J	K	S	R	Qn±	Q	$\bar{Q}$
↑	1	X	0	0	0	1	0
↑	X	0	0	0	1	1	0
↑	0	X	0	0	0	0	1
↑	X	1	0	0	1	0	1
↓	X	X	0	0	X	Qn	$\bar{Q}$n
X	X	X	1	0	X	1	0
X	X	X	0	1	X	0	1
X	X	X	1	1	X	1	1

x =Don t care

t =Level charge

± =Present state

n =Next state

Qn,$\bar{Q}$n =No change

Fig. J-K flip-flop

7-2 Vertical (V.) Wipe Wave Process Circuit

Outline

This circuit receives V. waveform from Waveform Gen. board and consists of H. and V. waveform mix control circuit, V. wipe border SHARP/SOFT/BORDER control circuit and V. waveform delete control circuit and produces V. wipe gate pulse which is supplied to Normal/Reverse control circuit and H. wipe wave process circuit.

Details

The vertical (V.) waveform signal is supplied to base of phase splitter Q8 from Waveform Gen. board and inverted V. waveform obtained at collector of Q8 is supplied to NORM-REV control Q10 through buffer Q9. The V. waveform obtained at emitter of Q8 is supplied to NORM-REV control Q11. The NORM-REV control Q10 and Q11 is switched by normal/reverse control signal supplied from flip-flop Q23 and Q24. Then the controlled V. waveform is supplied to schmitt trigger circuit Q16 to Q20 through amplifier Q12 and buffer Q13.

The H.V. mix control Q14 is switched by wipe pattern selector switches and Q14 turns ON when ◪ or ◙ pattern switch is selected.

Then V. waveform is mixed with horizontal (H.) waveform at base of Q30. However, when other wipe pattern is selected, the base of Q14 is low level and switched OFF.

The schmitt trigger circuit consisting of Q16 to Q20 produces V. gate pulse from V. waveform for wiping. The width of V. wipe gate pulse is controlled by changing the base DC voltage of Q16, which is determined by V. wipe control voltage corresponding to combination of variable resister with V. wipe lever passed through V. wipe wave DC bias Q15. The Q18 is switch for SHARP/SOFT wipe. While SOFT wipe switch is selected, Q18 is switched OFF and output pulse rises gradually by the resistance of R45 and R47.

The Q17 and Q19 are switch for BORDER wipe. While BORDER WIPE switch and ▬ or ▣ pattern switch are selected, Q17 is switched ON and output pulse rises gradually by resistance of R45 and R47 and V. triangle border width VR2.

While BORDER WIPE switch and other pattern switches of ▬ and ▣ are selected, Q19 is switched ON and output pulse rises gradually by resistance of R45 and R47 and V. sawtooth/parabola border width VR1.

Q21 is for V. waveform deletion. While ◨ , ◪ , ◫ or ◙ pattern switch is selected, Q21 is switched ON and V. schmitt trigger circuit turns OFF.

The V. wipe gate pulse at collector of Q20 is supplied to V. wipe wave output Q22.

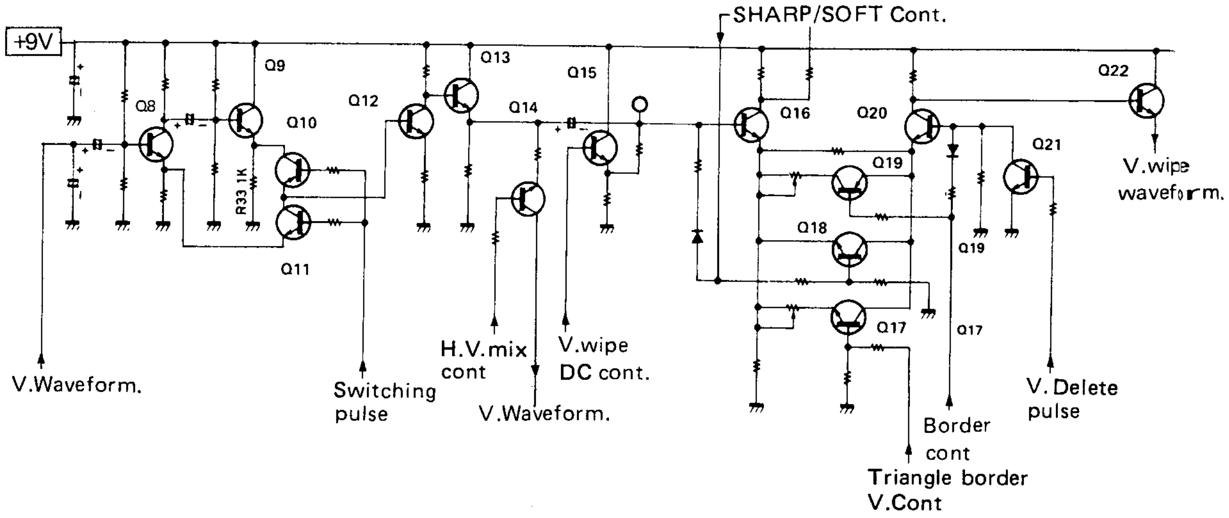
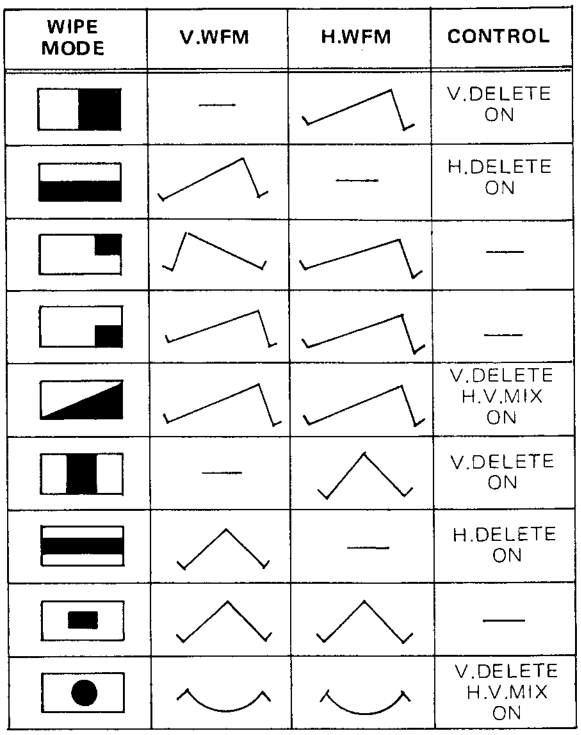


Fig. 7-2



WIPE MODE	V.WFM	H.WFM	CONTROL
	—		V.DELETE ON
		—	H.DELETE ON
			—
			—
			V.DELETE H.V.MIX ON
	—		V.DELETE ON
		—	H.DELETE ON
			—
			V.DELETE H.V.MIX ON

Fig. 7-3

7-3. Horizontal (H.) Wipe Wave Process Circuit

Outline

This circuit receives H. waveform from Waveform Gen. board, V. waveform from V. wipe wave process circuit and modulation wave from Modulation board.

This circuit consist of H. SHARP/SOFT/BORDER control circuit and H. delete control circuit and produces H. wipe gate pulse which is supplied to Normal/ Reverse control circuit.

This circuit similar to the vertical wipe wave process circuit.

Details

The phase splitter Q25 receives H. waveform from Waveform Gen. board and inverted H. waveform at collector of Q25 goes into Q27 through buffer Q26, also H. waveform at emitter of Q25 goes into Q28. The Q27 and Q28 are switched by Normal/Reverse control signal from flip-flop of Q23 and Q24. Then the H. waveform is supplied through amplifier Q29 and buffer Q30 to schmitt trigger circuit consisting of Q32, Q34, Q35, Q36 and Q37.

The schmitt trigger circuit of Q32 and Q34 to Q37 produces H. gate pulse from H. waveform, which is necessary for Wiping.

The width of H. wipe gate pulse is controlled by changing the base DC voltage of Q32, which is supplied by H. wipe control voltage from variable resister of H. Wipe lever passed through H. wipe wave DC bias Q31 and mixed at base of Q32 with modulation wave which is supplied from Modulation board. The Q35 is the switching transistor for SHARP/SOFT wipe. While SOFT wipe switch is selected, the Q35 is switched OFF and output pulse rises gradually by R89 and R91. The Q34 and Q36 are switching transister for BORDER wipe. While BORDER wipe switch and ◫ or ▣ pattern switch are slelected, the Q34 is switched ON and output pulse rises gradually by R89, R91 and VR4(H. BORDER TRIANGLE WIDTH). While BORDER wipe switch and all other wipe pattern switches of ◫ and ▣ are selected, the Q36 is switched ON and output pulse rises gradually by R89, R91, and VR3(H. BORDER SAWTOOTH, PARABOLA WIDTH). Transistor Q38 is for H. waveform deletion while ▬ or ▬ pattern switch is selected, the Q38 is switched ON, and the H. schmitt trigger circuit is turned OFF. The H. wipe gate pulse at collector of Q37 is supplied to H. wipe wave output Q40.

7-4. Normal/Reverse Control Circuit

Outline

This circuit selects Normal or Reverse output wipe waveform, and controlled by Wipe lever limit switches and Normal/Reverse selector switches.

Details

The H. and V. wipe waveform output at emitter of Q22 and Q40 are mixed at bases of Q41 and Q42 after they pass through the AND gate D9 and D20 and the OR gate D10 and D21 respectively. A Normal/Reverse switching selection circuit consisting of Q45 and Q46 select Q41 or Q42 output wipe waveform for Normal-Reverse control. Then this selected wipe waveform goes into wipe waveform output switching transistor Q47, Q47 is turned ON in wiping mode, which is selected WIPE or WIPE KEY switch on Wipe/ Key control, and the selected wipe waveform is supplied to wipe wave selection circuit on Modulation board as a internal wipe pulse signal.

The NormalReverse switching consisting of Q45 and Q46 controlls Q43 and Q44. When either ◳, ◲ or ▣ wipe pattern switch is slected the Q46 is switched ON and the potential at collector of Q45 changes repeat "H" and "L" according to the control voltage from flipflop Q23 and Q24 and thus Q43 and Q44 are controlled. When any other button of ◳, ◲ and ▣ pattern selector switch is selected, the Q43 remains ON. While Q46 is switched OFF, and output waveform from D9 and D20 is sent out as a wipe pulse signal.

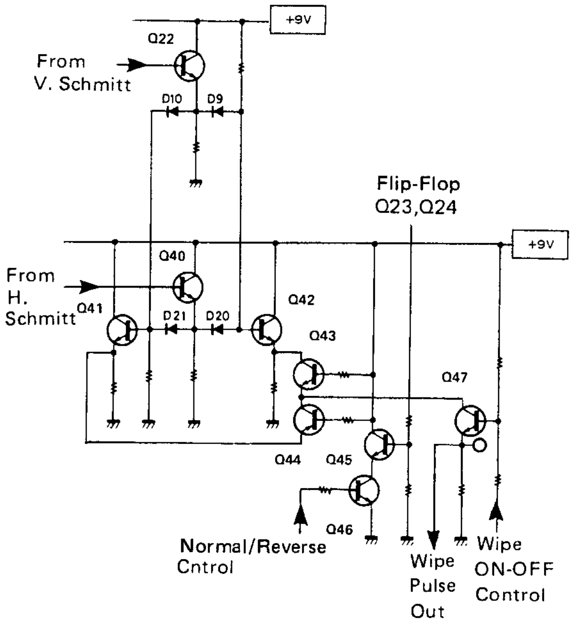


Fig. 7-4

The transistors Q23 and Q24 make up a flip-flop circuit which works in conjunction with the Wipe lever limit switches within vertical interval when one of NORM (normal), NORM-REV (normal-reverse), REV (reverse) mode is selected and control signal is supplied from IC5. The pin 1 and pin 15, pin 4 and pin 5 of IC5 are connected when REV switch is selected on the Normal/ Reverse Selector. The pin 2 and pin 15, pin 3 and pin 4 of IC5 are connected when NORM switch is selected on Normal/Reverse Selector. When NORM-REV switch is selected on Normal/Reverse Selector, pin 2 and pin 15, pin 4 and pin 5 of IC5 are connected due to low potential is supplied to pins 9 and 10 of IC5, thus flip-flop consisting Q23 and Q24 keeps previous condition.

The Normal-Reverse control consisting of Q10 and Q11 switches vertical waveform polarity by control voltage which is supplied from flip-flop of Q23 and Q24, the Q27 and Q28 switches horizontal waveform polarity by control voltage which is supplied from flip-flop of Q23 and Q24 as vertical circuit.

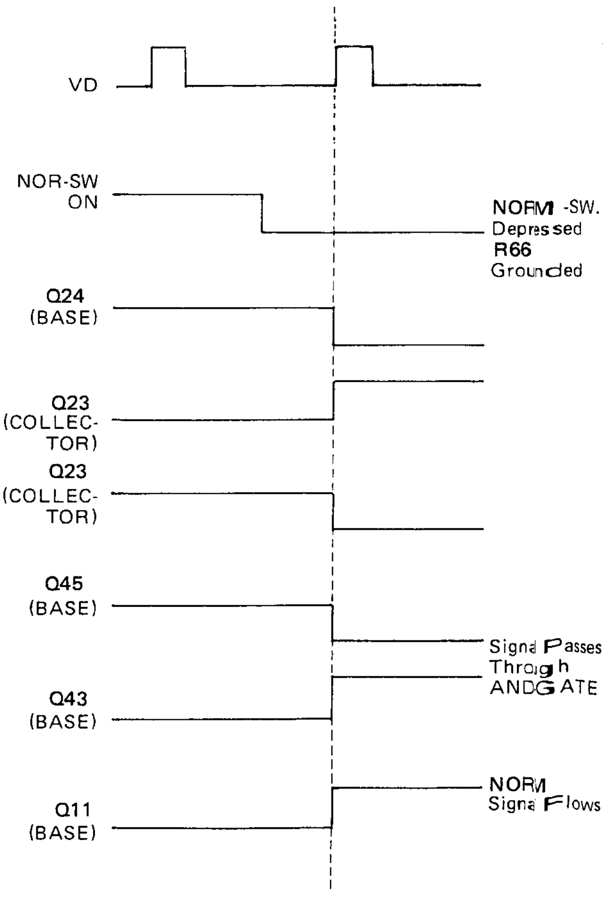


Fig. 7-5

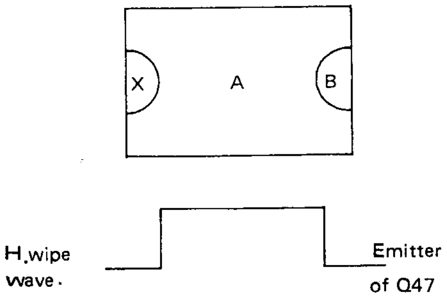
7-5. Positioner Cancel Control Circuit

Outline

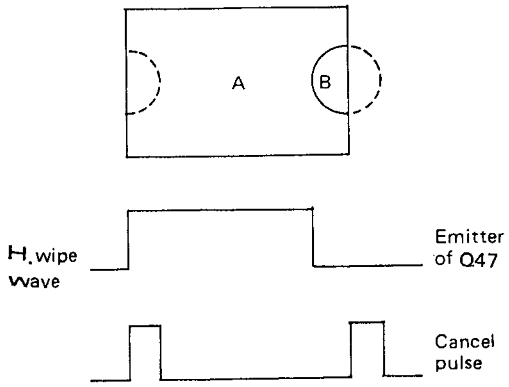
When positioner (POSI) switch is ON and postioner lever is moved, this circuit receives cancel pulse from Waveform Gen. board and generates control signal to delete H.V. wipe wave signal.

Details

Q33 and Q39 are controlled by cancel pulse (Fig.8-4-2) which is supplied from exclusive-NOR circuit on Waveform Gen. board. When the cancel pulse enters to the base of Q33 and Q39 to turn them ON, and thus bases of Q20, and Q37 are grounded through D7, D15, Q39 and Q23, or bases of Q22, and Q40 are grounded through D8, D16, Q33 and Q24. Therefore vertical and horizontal wipe waveform are not supplied to output. Thus, when positioner (POSI) switch is ON and positioner lever is moved and if the wipe waveform (X) appears in the area as shown in Fig.7-5-1, the cancel pulse is generated in order to eliminate the waveform (X). (Fig.7-5-1)



In case of no cancel pulse supplied.



In case of cancel pulse supplied.

Fig. 7-5-1

8. Waveform Gen Board

The waveform Gen. Board contains following circuits.

8-1. Wipe Pattern Select Circuit 31
8-2. Horizontal Waveform Generator Circuit 31
8-3. Vertical Waveform Generator Circuit 33
8-4. Others Circuit 33

8-1. Wipe Pattern Select Circuit

Outline

This circuit supplies control signal to H.V waveform generator circuit and wipe process board, and operates with wipe pattern select circuit on the Modulation board.

Details

The pattern clock control signal is supplied to vertical interval switching circuit on modulation board from D1 to D5. The pattern clock signal from modulation board through pin 17 (a, b) of CN24 is supplied to pin 9 of IC1. Therefore this pattern select switches are vertical interval switching using with flip-flop circuit IC1. The diodes D6 to D19 are OR gate, control signal is supplied to H,V waveform generator circuit and wipe process board.

8-2. Horizontal Waveform Generator Circuit

Outline

This circuit generates the horizontal (H.) triangle, sawtooth and parabola waveform and they are supplied to the Wipe Process board.

Details

The horizontal drive (HD) pulse from sync generator is supplied through inverter Q11 to monostable multivibrator (M.M.V.) IC4 (a).

The output Ⓐ is obtained at pin 9 of IC4 (a) and rise timing of output pulse is controlled by VR7 (H. CENT). This output pulse is supplied to next M.M.V. and pin 12 of IC2 (b).

The output Ⓑ is obtained at pin 3 of IC4 (b) and start timing of output pulse delays 1/2 blanking width from rise timing of HD pulse.

This 1/2 blanking width is controlled by VR7, when the positoner (POSI) switch is switched OFF.When positioner (POSI) switch is switched ON and positioner lever is moved, the voltage at the base of Q12 differ from original voltage and the value of the time constant of IC4 (a) and IC4 (b) will be changed. Therefore it is possible to shift the phase of H. wipe waveform from its starting point (a 1/2 of blanking duration)Ⓑ.

The IC4 (c) is a monostable multivibrator to produces a pulse of 1/2 H. width Ⓒ for H. triangle pulse generator circuit of Q10.

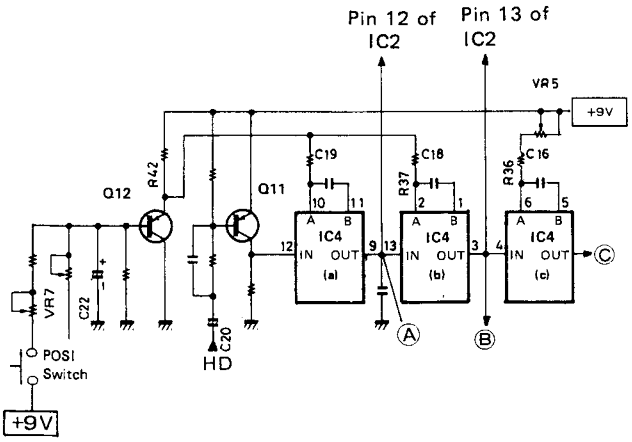
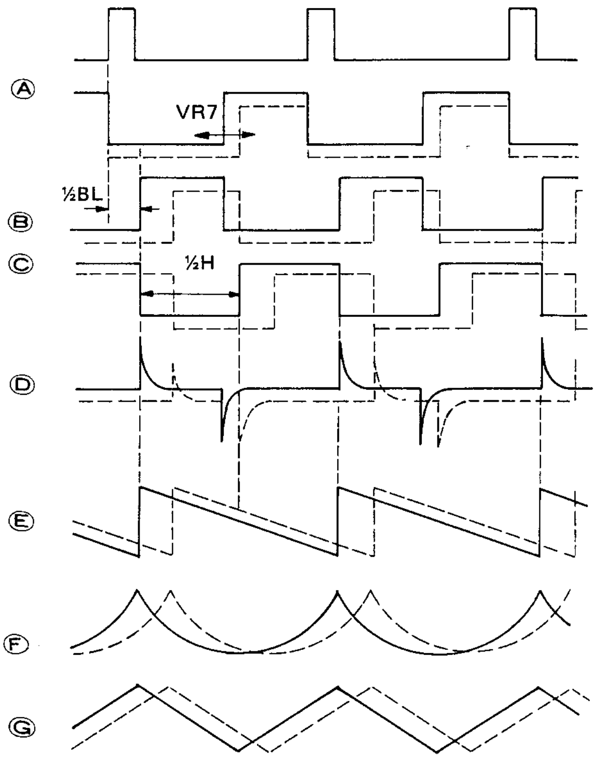

Pin 12 of IC2
Pin 13 of IC2
VR5
+9V
R42
Q12
Q11
C19
R37
C18
R36
C16
IC4 (a)
IC4 (b)
IC4 (c)
IN OUT
A B
VR7
C22
C20
HD
POSI Switch
+9V
Ⓐ
Ⓑ
Ⓒ

Fig. 8-2-1



Heavy Line : Positioner switch OFF.
Pashed Line: Positioner switch ON and Lever is moved.

Fig. 8-2-2

The H. sawtooth waveformⒺand H. parabola waveform Ⓕare shaped from output pulse Ⓑ obtained at pin 3 of IC4. The H. wipe waveform output pulseⒷat pin 3 of IC4 is fed through control-current-differential circuit consisting of C29, R64 to base of Q21, and changed to pulse Ⓓ. The control-current-integration circuit Q19, C27, R60 produces a sharp H. sawtooth waveform Ⓔ. This signal passes through buffer Q18, Q17 and H. sawtooth output switching Q14 and the signal is controlled by VR9 (H. SAWTOOTH) and then supplied to the H. wipe wave process circuit on Wipe Process board. Also the H. sawtooth waveform is supplied to bootstrap circuit consisting of Q16,C24,C25, and R53,produces a H. parabola waveform Ⓕ. This waveform passes through buffer Q15 and H parabola waveform output switching Q13 and the signal is controlled by VR8 (H. PARABOLA) and then supplied to the H. wipe wave process circuit on Wipe Process board.

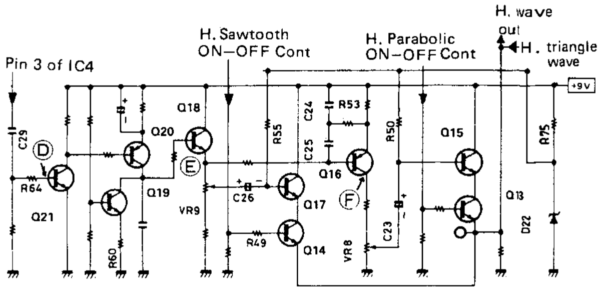

Pin 3 of IC4
H. Sawtooth ON–OFF Cont
H. Parabolic ON–OFF Cont
H. wave out
H. triangle wave
+9V
C29
Ⓓ
R64
Q21
Q20
Q19
R60
Q18
Ⓔ
C26
VR9
R49
Q17
Q14
R55
C25
C24
R53
Q16
Ⓕ
C23
VR8
R50
Q15
Q13
R75
D22

Fig. 8-2-3

The 1/2 H. pulse Ⓒ is supplied to bootstrap circuit consisting of Q10,C14,C15, and R34 from pin 7 of IC4 for produce a H. triangle waveform Ⓖ. This waveform passes through buffer Q9 and H. triangle outputswitching Q8 and the signals are controlled by VR4 (H. TRIANGLE) and then supplied to the H. wipe wave process circuit on Wipe Process board.

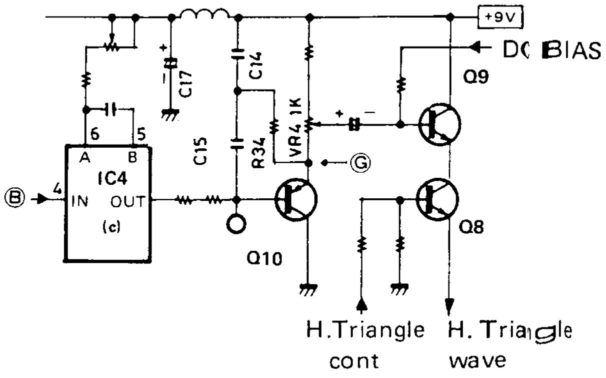

+9V
DC BIAS
Q9
C17
C14
C15
R34
VR4 1K
Ⓖ
IC4 (c)
A B
6 5
4
IN OUT
Ⓑ
Q10
Q8
H.Triangle cont
H. Triangle wave

Fig. 8-2-4

8-3. Vertical Waveform Generator Circuit

Outline

This circuit generates the vertical (V.) triangle, sawtooth, negative sawtooth and parabola waveform and they are supplied to the Wipe Process board.

Details

The vertical drive (VD) pulse from sync generator is supplied through inverter Q6 to monostable multivibrator (M.M.V.) IC3 (a).

The output Ⓐ is obtained at pin 3 of IC3 (a) and rise timing of output pulse is controlled by VR2 (V.CENT). This output pulse is supplied to next M.M.V. and pin 2 of IC2 (a).

The output Ⓑ is obtained at pin 7 of IC3 (b) and start timing of output pulse delays 1/2 blanking width from rise timing of VD pulse. This 1/2 blanking width is controlled by VR2, when the positioner (POSI) switch is switched OFF. When positioner (POSI) switch is switched ON and positioner lever is moved, the voltage at the base of Q7 differ from original voltage level of the time constant IC3 (a) and IC3 (b) will be changed. Therefore it is possible to shift the phase of V. wipe waveform from its starting point (a 1/2 of blanking duration) Ⓑ.

The IC3 (c) is a monostable multivibrator to produce a pulse of 1/2 V. width Ⓒ for V. triangle pulse Ⓖ generator circuit of Q27.

The V. sawtooth waveform Ⓔ and V. parabola waveform Ⓕ are shaped from output pulse Ⓑ obtained at pin 7 of IC3. The wipe waveform output pulse Ⓑ is fed through control-current-differential circuit consisting of C42, R100 to base of Q36 and changed to pulse Ⓓ. The control-current-integration circuit consisting of Q34, C39, R96 produces a sharp V. sawtooth waveform Ⓔ. This waveform passes through buffer Q35 and Q33. This waveform is supplied to base of invertor Q32, sawtooth waveform (negative V. sawtooth) obtained at collector of Q32 is supplied to V. negative sawtooth output switching Q25 through the buffer Q30, controlled by VR12 (V. NEG SAWTOOTH), V. sawtooth waveform obtained at emitter of Q32 is supplied to V. sawtooth output switching Q22 through the buffer Q31, controlled by VR13 (V. SAWTOOTH), to the V. wipe wave process circuit on wipe process board. Also the V. sawtooth waveform at emitter of Q33 is supplied to bootstrap circuit consisting of Q29, C34, C35, R84 produces a V. palabola waveform Ⓕ. This waveform passes through buffer Q28, V. parabola waveform output switching Q23, and controlled by VR11 (V. PARABOLA) to the V. wipe wave process circuit on Wipe Process board.

The 1/2 V. pulse Ⓒ from pin 9 of IC3 is supplied to bootstrap circuit consists of Q27, C31, C32, R79 for produces a V. triangle waveform Ⓖ. This waveform passes through buffer Q26, V. triangle output switching Q24 and controlled by VR10 (V. TRIANGLE) to the V wipe wave process circuit on Wipe Process board.(Fig. 8-2-2)

8-4. Other Circuit

DC bias voltage determined by the zener diode D22 and resister R75 is supplied to the waveform output transister Q17 and others.

The Exclusive–NOR IC2 receives H. and V. wavefom from IC4 and IC3, then this output signal is supplied to Q33 and Q39 on Wipe Process board for wipe waveform cancel control when positioner switch ON and positioner lever moved through gate D20 and D21.

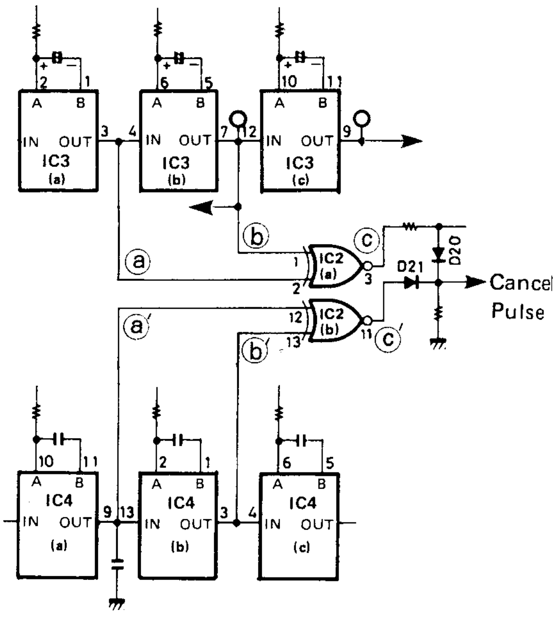
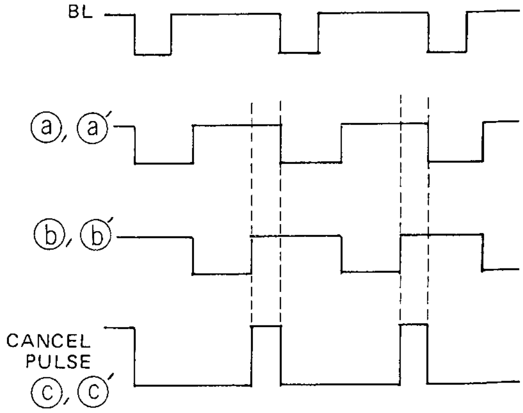


Fig. 8-4-1



*Position lever at left and up side from center.

Fig. 8-4-2

9. Modulation Board

The modulation board contains following circuits.

9-1. Wipe Pattern Select Circuit 34
9-2. Modulation Wave Generator Circuit 34
9-3. Wipe Wave Int/Ext Select Circuit 34
9-4. Border Pulse Generator Circuit 35

9-1. Wipe Pattern Select Circuit

Outline

This circuit supplies control signal to H.V. waveform generator circuit on waveform generator board and H.V. wipe wave process circuit on wipe process board.
The wipe pattern select circuit is switched in the vertical interval switching (V.I.S.) duration.

Details

When the power switch is turned ON, +9V DC is supplied, and C3 is turned ON, then the reset terminals of each D flip-flop inside IC2 become low level and each Q and $\overline{Q}$ output terminlas are set to low level and high level respectively.
The V.I.S. pulse Ⓐ is supplied to pin 8 of AND gate IC2 (b) from pin 13 (a) (b) of CN25. The output of an OR gate D1 to D5 signal selected by the wipe pattern selector switches is obtained at pin 9 of IC1 (b).
When the pattern ◨ is depressed, high potential at anode of D1 is applied to pin 9 of IC1 (b) and at the same time pin 3 of IC2 (a) becomes high level Ⓑ. Within this period of time, the V.I.S. pulse is supplied to pin 9 of IC2 (a) through AND gate IC1 (b) as the clock pulse Ⓒ. Since all D inputs are low level except pin 3 of IC2 (a), the output of flip-flop at pin 2 of IC2 (a) becomes high level Ⓓ and all other outputs remain low level. This condition is kept until next clock pulse is applied to clock terminal of IC2 by depressing other wipe pattern select switch.

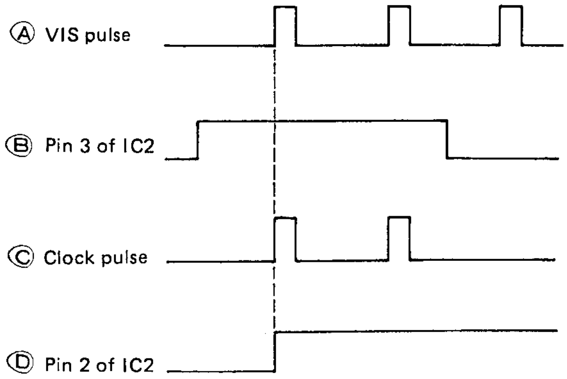


Fig. 9-1-1

The high level output at pin 2 of IC2 (a) is supplied to pilot lamp control Q1 for switching ON of ◨ wipe pattern lamp, pin 13 of wipe cont AND gate IC1 (c) and pin 14(b) of CN 25 through D7, and pin 9 (a) of CN 25 through D6 as V. delete out signal used on wipe process board.
The clock pulse obtained at pin 10 of IC1 (b) is supplied to pin 9 of IC1 in wipe pattern select circuit on waveform generator board through pin 18 (b) of CN25.
The output signals of OR gate of D6, D8, D12, D13 and D14 are supplied to wipe process board.
The output signals of OR gate of D10, D11 and D15 are supplied to waveform generator board.

9-2 Modulation Wave Generator Circuit

Outline

This circuit generates border modulation wave signal when the modulation (MOD) ON/OFF switch is depressed on wipe process board and this signal is supplied to H. wipe wave process circuit on wipe process board.

Details

When the modulation ON/OFF switch on wipe process board is depressed, high potential is supplied to base of ON/OFF control Q16. This high potential turns OFF Q16 and pin 5 of IC4 becomes high level. Then IC4 becomes oscillator and output obtained at pin 7 is supplied to H. wipe wave process circuit on wipe process board through buffer Q17, VR3 (BORDER MODULATION AMP.) and buffer Q18.
VR2 (BORDER MODULATION FREQ.) is a control for adjusting the frequency of the border.
VR11 (FREQUENCY PRESET) is a control for presetting the frequency of the border.

9-3 Wipe Wave Int/Ext Select Circuit

Outline

This circuit receives internal and external wipe signals and selects them by switching IC which is controlled by wipe pattern select switch and then wipe wave signal is supplied to DSK, BGD board.

Details

Internal wipe wave signal supplied from wipe process board through pins 21 (a) (b) of CN25 is supplied pins 1, 2, and 15 of switching IC5.

External wipe pattern signal supplied from external pattern connector on rear panel through pin 2(a)(b) of CN25 is supplied to gate of Q25. External wipe pattern signal is clamped by clamp pulse supplied to gate of Q26 whose level is controlled by VR10 (EXT PATTERN DC LEVEL).Then the clamped external wipe pattern signal is supplied to pins 4 and 5 of switching IC5 through buffer Q24, amplifier Q23 and buffer Q22. When the wipe pattern select switch of EXT is depressed, high potential is supplied to pin 10 of IC5.
When the border switch is depressed, high potential is supplied to pin 9 of IC5.
When the high potential is supplied to pin 10 of IC5, X1 and Y1 terminals are connected to X and Y terminals respectively.
When the high potential is supplied to pin9 of IC5, X2 and Y2 terminals are connected to X and Y terminals respectively.
When the both pins 9 and 10 of IC5 are high potential, X3 and Y3 terminals are connected to X and Y terminals respectively.

9-4 Border Pulse Generator Circuit

Outline

This circuit generates border pulse and border pulse is supplied to border wipe amplifier circuit on the effect, mix board.

Details

Wipe wave is supplied to base of amplifier Q7 through buffer Q6 and VR4 (BORDE POSITION) from pin 13 of IC5. The wipe wave supplied at base of Q7 is amplified and obtained at emitter and collector, and pulse is supplied to base of Q11 through differential amplifier circuit consisting of Q9 and Q10. This differential amplifier circuit operates as NAM (non additive mixer) circuit, therefore higher level of wipe wave on bases of Q9 and Q10 is obtained at emitters of Q9 and Q10. Q11, Q12 and Q13 consist of differential amplifier and the pulse obtained at base of Q11 is amplified and supplied to border wipe amplifier circuit on the effect, mix board through border pulse ON/OFF control Q14 and buffer Q15.
When the border switch on the wipe process board is not depressed, low potential is supplied to base of border pulse ON/OFF control Q14 and turns ON the Q14 and turns OFF Q15. Then the border pulse is not supplied to effect, mix board.
However, when the border switch is depressed, Q14 is turned OFF by high potential supplied from wipe process board and Q15 turns ON, then borde pulse is suppoied to effect, mix board.
VR5 (BORDER PULSE LEVEL) is a control for adjusting the level of the border pulse.
VR1 (BORDER WIDTH) is a control for adjusting the width of the border pulse.

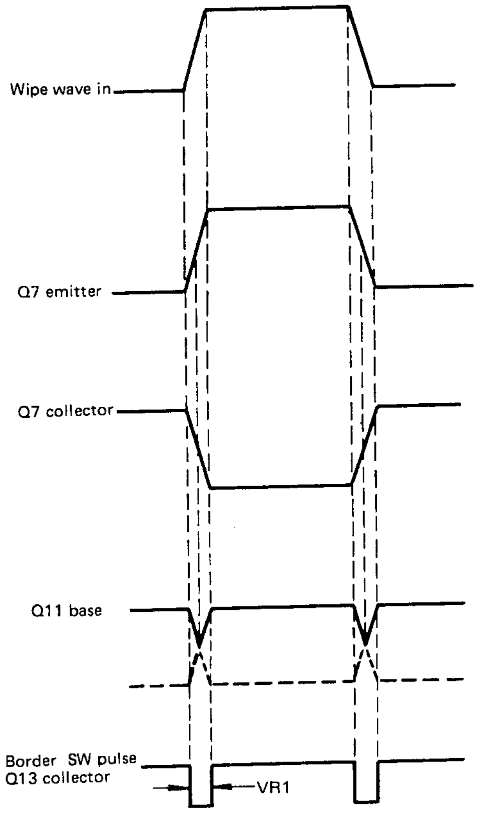


Fig. 9-4-1

10. Lever Board

This lever board mainly consists of lever connection board and position SW bottom board and contains following circuits.

10-1 Gen-Lock Selection Circuit 35
10-2 DSK Selection Circuit 36
10-3 CUT Selection Circuit 36
10-4 Position Control Circuit 36

10-1 Gen-Lock Selection Circuit

Outline

When the Gen-Lock select switch is depressed, this circuit supplies high potential to lamp ON/OFF control Q1 for switching ON and sync separation circuit on sync, C/Bar board for VBS switching.

Details

When the power switch is turned ON, +9V DC is supplied to C3 on level connection board and then the reset terminal of pin 12 of IC1 (b) becomes low level and Q and $\bar{Q}$ output terminals are set to low level and high level respectively.

When the Gen-Lock select switch is depressed, high potential is supplied to pin 13 of clock input of IC (b), then Q output of flip-flop of IC1 (b) becomes high level and $\bar{Q}$ output remains low level. The high level of Q output at pin 15 of IC1 (b) is supplied to VBS switching Q27 on sync separation circuit of Sync,C/Bar board for Gen-Lock sync operation.

When the sync generator IC12 on Sync, C/Bar board is in Gen-Lock mode, low potential is supplied to pin 12 of NOR gate IC2 (c) and high potential output at pin 11 turns ON Q1.

10-2 DSK Selection Circuit

Outline

When the DSK select switch is depressed, this circuit supplies high potential to lamp ON/OFF control Q2 for switching ON, program out processing circuit on output board and DSK pulse generator circuit on DSK, BGD board for DSK switching.

Details

When the power switch is turned ON, +9V DC is supplied to C3 on level connection board and then the reset terminal of pin 4 of IC 1 (a) becomes low level and a output terminal is set to low level.

The NOR gates of IC2 (a) and IC2 (b) consists of flip-flop, which output is connected to pin 3 of clock input of J-K flip-flop. The V.I.S. pulse is supplied to pin 1 of flip-flop IC2 (a).

When the DSK switch is depressd, low level at pin 3 of IC1 (a) is changed to high level on next V.I.S. pulse timing, thus Q output terminal at pin 1 of IC1 (a) becomes high level. It is supplied to base of Q2 for switching ON program out processing circuit on output board and DSK pulse generator circuit on DSK, BGD board for DSK switching through pin 13 (a) of CN26.

10-3 CUT Selection Circuit

Ourline

When the cut switch is depressed, this circuit supplies high potential to lamp ON/OFF control Q3 for switching ON and low potential to cut contrtol circuit on input PV-PG board for video reversing on program line and preview line.

Details

When the power switch is turned ON, +9V DC is supplied to C3 on lever connection board and then the reset terminal of pin 4 of IC3 (a) becomes low level and Q and $\bar{Q}$ output terminals are set low level and high level respectively.

The $\bar{Q}$ output pin 14 of J-K flip-flop IC3 (b) is connected to clock input at pin 3 of IC3 (a). The V.I.S. pulse is supplied to pin 12 of reset terminal of IC3 (b).

When the cut switch is depressed, high potential is supplied to set terminal, and $\bar{Q}$ output at pin 14 changes by next V.I.S. pulse. This clock signal changes Q output and $\bar{Q}$ output as high level and low level respectively. Then cut lamp Q3 is turned ON and low level is supplied cut control circuit on input PV-PG board through 13 (b) terminal of CN26.

10-4 Position Control Circuit

Outline

When the positioner switch is depressed, this circuit supplies DC bias corresponding to the position of control to the H.V. waveform generator circuit on waveform generator board.

Details

This circuit consists of two J-K flip-flops, lamp ON /OFF control, position SW H.V. output and positioer volume control. The position ON/OFF switch is connected to set terminal pin 7 of IC1 (a) and the V.I.S. pulse is supplied reset terminal pin 4 of IC1 (a).

When the power switch is turned ON, +9V DC is supplied to C3 on Position-1 board, and then the reset terminal of pin 12 of IC1 (b) becomes low level and Q and Q output terminals are set low level and high level respectively

When the positioner switch is then depressd, Q and $\bar{Q}$ outputs at pins 15 and 14 of IC1 (b) are turned high level and low level respectively. The high level at pin 15 of IC1 (b) turns lamp ON/OFF control Q3 ON and position SW H.V. output Q4 and Q5, and the low level at pin 14 of IC1 (b) turns position VR control Q 1 and Q2. Thus DC bias corrersponding to the position of control is supplied to H.V. waveform generator circuit on waveform generator board through pins 4 (a) (b), 5 (a) (b), 6 (a) (b) and 7 (a) (b) of CN26.

11. Sync. C/Bar Board

The Sync, C/Bar board contains the following circuits.

11-1 Color Bar Signal Generator Circuit 37
11-2 Matrix Circurt 37
11-3 Balance Madulator Circult 38
11-4. Int 17MHz/14MHz Oscillation Circuit 38
11-5. Sync Generator Circuit 38
11-6. Sync Separation Circuit 39
11-7 Gen-Lock 14 MHz Oscillator Circuit 40
11-8. Ext 14 MHz Oscillator Circuit 41
11-9. SC Phase Shifter Circuit. 41
11-10. SC Out Circuit .41

11-1 Color Bar Signal Generator Circuit

Outline

This circuit generates the red (R), green (G) and blue (B) bar signal for making a color bar signal. The R, G and B bar signals are then fed to the matrix circuit.

Details

A NAND gate IC1 (a) and an inverter IC (b) make up the oscillator whose oscillating frequency is set to approximately 134 kHz by VR1 (BAR WIDTH). When the C/7, Color bar (C/B) Selector switch on the front panel is set to color bar (C/B) position, the low potencial is sent to base of oscillator reset Q1 through pin 19 (a) of CN27 and the composite pre-blanking (CP BL) pulse Ⓐ is fed to the pin 14 at IC1 (a) through Q1 to reset the oscillator. As a result, the signal Ⓑ is obtained at pin 11 of IC1 (b). The signal Ⓑ is fed to the clock input pin 15 of R.G.B counter IC2 and is counted down. The B bar signal Ⓒ obtained at pin 6 of IC2, the R bar signal Ⓓ at pin 11 and the G bar signal Ⓔ at pin 14 are fed to the matrix circuit.

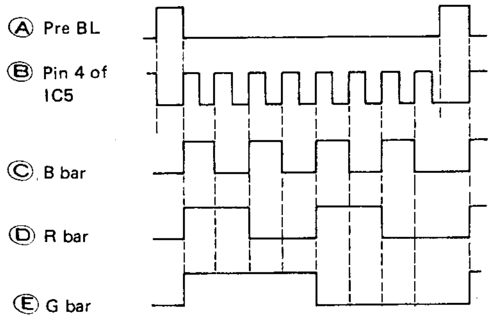


Fig. 11-1-1 R,G,B Bar Signal

11-2 Matrix Circuit

Outline

This circuit generates luminance (Y) and R-Y, B-Y color difference signal from R, G, and B bar signals of R.G.B bar counter IC2.

Details

The B bar signal Ⓒ, the R bar signal Ⓓ and the G bar signal Ⓔ from R, G, B counter is supplied to resistor-matrix circuit consisting of R9 to R14 which arranges in the ratio of R, G and B signal to 0.3R + 0.59G + 0.11B. And then mixed signal Ⓕ is supplied to base of amplifier Q3 through buffer Q2 and is controlled the gain by VR2 (Y GAIN). Also the B, R and G bar signal from R, G, B counter IC2 is supplied to AND gate circuit consisting D2 to D4 and the gated signal Ⓖ is obtained at pin 4 of IC1 (e). The gated signal Ⓖ is then supplied to base of Q3 through inverter IC1 (e), IC1 (f) and is controlled gain by VR3 (WHITE GAIN).

The mixed signal Ⓕ and gated signal Ⓖ is mixed at base of amplifier Q3, and is obtained as luminance (Y) signal Ⓗ at collector of Q3. The Y signal Ⓗ is sent to pin 9 of balance modulator IC3.

The B-Y matrix Q4 is received B bar signal at emitter from pin 6 of IC2 through VR4 (B-Y WHITE BALANCE) also Q4 is received mixed signal Ⓕ at base from emitter of Q2. Then the B-Y color difference signal Ⓘ obtained at collector of Q4 is supplied to pin 12 of balance modulator IC3 through VR5 (B-Y GAIN) and buffer Q5.

The R-Y matrix Q6 is received R bar signal at emitter from pin 11 of IC2 through VR6 (R-Y WHITE BALANCE), also Q6 is received mixed signal Ⓕ at base from emitter of Q2. Then the R-Y color difference signal Ⓙ obtained at Q6 is supplied to pin 10 of balance modulator IC3 through VR7 (R-Y GAIN) and buffer Q7.

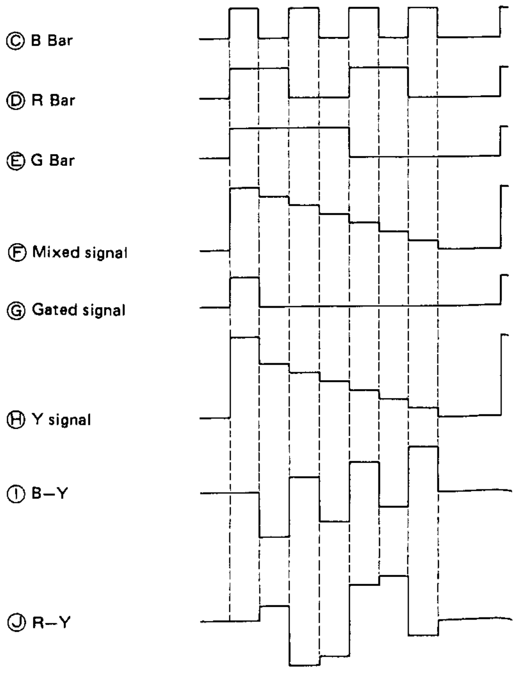


Fig. 11-2-1 Matrix signal

11-3 Balance Modulator (Chrominance) Circuit

Outline

This circuit receives the B-Y, R-Y color difference signal and the Y signal from respective matrix circuit. Also receives the two kinds of SC signals which is SC1 signal and SC2 signal from sync generator circuit. The modulated, and mixed signal which is a color bar signal is sent out to other circuit.

Details

The subcarrier (SC2) signal is sent through VR8 (SC QUAD) to buffer Q10. The SC2 signal at the emitter of Q10 is sent through band pass filter (BPF) CF2 and buffer Q11 to pin 15 of balance modulator IC3 for modulation of R-Y signal.

The SC1 signal whose phase is alternated every line is sent through buffer Q8, BPF CF1 and buffer Q9 to pin 16 of IC3 for modulation of B-Y signal.

The two SC signals fed through pin 15 and pin 16 of IC3 are sent through SC amplifiers to the each modulator in IC3 respectively. The B-Y, R-Y color difference signals fed through pin 12 and pin 10 of IC3 are sent through clamp circuit to the each modulators where these signal modulate the gated SC signals. The modulated B-Y and R-Y signal thus mode are sent to R-Y, B-Y mixed to confirm the chrominance signal.

The chrominance signal obtained at pin 3 of IC3 is supplied to 4.43 MHz band pass filter (BPF) consisting L3 to L5 and C16 to C18 where harmonics of 4.43 MHz is removed from the chrominance signal and sine-wave of 4.43 MHz remains. The chrominance signal is fed through pin 5 of IC3 to luminance (Y), chrominance (c) mix circuit in IC3.

The Y signal at collector of Q3 is supplied through pin9 of IC3 and clamp circuit to Y, C mix circuit in IC3.

The Y and C mix signal which is color bar signal obtained at pin 8 of IC3, is sent out through buffer Q12 to other circuit.

VR9 (R-Y CARRIER BALANCE) and VR10 (B-Y CARRIER BALANCE) are adjusted the DC level at pins 11 and 13 of IC3 to minimize the carrier leak from the modulator.

11-4 Int 17MHz/14MHz Oscillator Circuit

Outline

This circuit oscillates the 14MHz frequency in the internal sync mode and sends it to the sync generator IC. In the gen-lock/external sync mode, this circuit stops oscillating the 14MHz frequency.

Details

When no signal is supplied to pin 37 of sync generator IC8, internal 17MHz oscillator consisting of crystal oscillator X2, CT2 (4.43MHz ADJ) and C48 oscillates 17MHz frequency. The oscillated 17MHz signal is sent to IC8, it is compared in phase with the signal oscillated by voltage controlled crystal oscillator (VCXO) consisting of X3, CT3 (FIELD DETECT), C50 and C51, and the phase difference is converted into the DC voltage.

The DC voltage corresponding to the phase difference is obtained at pin 46 of IC8 and sent to the VCXO to controlled the oscillating frequency by changing the capacitance of variable capacitance diode D7. The frequency-controlled signal is then fed to IC8 through pin 41 and it is compared with the 17MHz signal in phase. In this way, the phase lock loop (PLL) is made and pulses locked with the subcarrier signal are generated from IC8 respectively. When the PLL is stabilized, the VCXO oscillates approximately 14MHz. CT2 is a control for setting the subcarrier frequency by controlling the internally oscillated 17MHz frequency. CT3 is for setting lock range of VCXO.

11-5. Sync Generator Circuit

Outline

This circuit receives the 17 MHz signal in internal sync mode or external sync mode, and generates all sync signals which are used in the special effect generator and sends out to other systems from special effectgenerator.

Details

The 4.43 MHz subcarrier signal (SC1) is obtained at pin 24 of sync generator IC 8 and it is sent to the SC out circuit and balance modulator circuit.

The 4.43 MHz, subcarrier signal (SC2) is obtained at pin 21 of sync generator IC8 and it is sent to the SC.A output IC7(a) and balance modulator circuit.

The burst subcarrier (B.SC) pulse Ⓐ is obtained at pin 20 of sync generator IC8 and it is sent to burst generator circuit on output board through the buffer Q25.

The horizontal drive (HD) pulse Ⓑ at pin 17 of sync generator IC8 is sent out to HD output connector on rear panel through the connector board, also sent out to horizontal waveform generator on waveform gen. board through the inverter IC10(b).

The composite sync pulse Ⓒ at pin 14 of sync generator IC8 is sent out to the sync output connector on rear panel through connector board, and is sent out to clamp pulsu generator circuit on DSK,BGD board through the inverter IC10(C).

The burst flag pulse (BFP) Ⓓ at pin 13 of sync generator IC8 is sent out to the BFP output connector on rear panel through the connector board. The composite pre-blanking (pre BL) pulse Ⓔ at pin 9 of sync generator IC8 is sent out to the color bar signal generator circuit. The composite blanking (BL) pulse Ⓕ at pin 7 of sync generator IC8 is sene out to BL output connector on rear panel through connector board, and sent out to sync separation circuit respectively. Also sent out to output board, DSK, BGD board and effect mix board through inverter IC10(b).

The horizontal scanning start (Hs) pulse Ⓖ at pin 11 of IC8 is sent to balance modulator IC3.

The PAL pulse Ⓗ at pin 19 of IC8 is sent to the PAL pulse output connector on rear panel through the connector board.

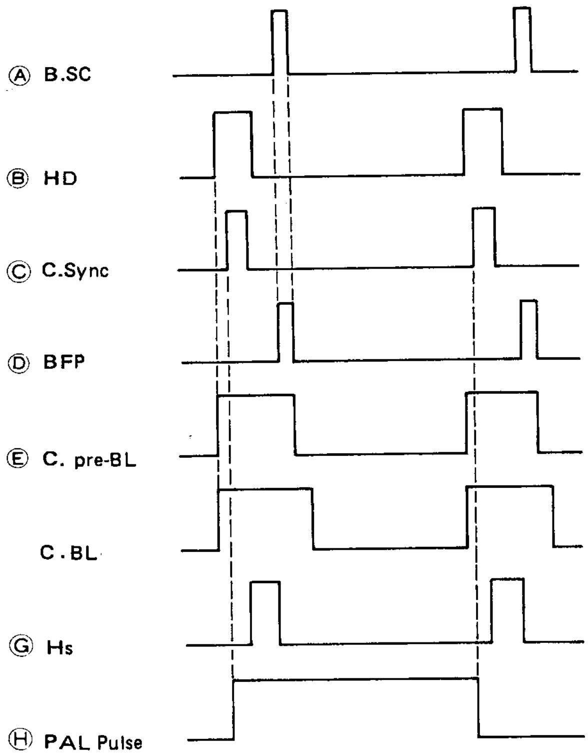


Fig. 11-5-1 Sync Signal

11-6. Sync Separation Circuit

Outline

This circuit receives the black burst signal or V.B.S signal which is supplied to the GEN-LOCK input connector on rear panel, and separates the sync and burst signal from the gen-lock signal. The separated sync and burst signal are fed to the sync generator circuit for the gen-lock/external sync mode.

Details

The black burst or V.B.S signal (gen-lock signal) Ⓐ is sent through connector board and pin 9 (a) of CN27 to the collector of Q13. The control potential of switching transistor Q13 is supplied to base of Q13 from GEN-lock ON/OFF switch. Therefore when GEN-LOCK ON/OFF switch is ON, the base of Q13 becomes high level and turns Q13 ON. Thus gen-lock signal obtained at emitter of Q13 and is sene to burst separation and sync separation circuit. When the GEN-LOCK ON/OFF switch is OFF, the Q13 turns OFF, and gen-lock signal blocked.

The base of sync separation Q22 is received gen-lock signal through buffer Q21 from Q13. The separated sync signal obtained at collector of Q22 is sent through amplifier Q23 and NOR gate (inverter) IC5 (a) to pin 37 of IC8 in the sync generator circuit, the sync generator IC8 is converterted into the gen-lock/external sync mode and pulses which are synchronized with the separated sync signal is generated.

If the sync signal is not applied to pin 37 of IC8, the sync generator IC8 remains in the internal sync mode.

The separated sync signal Ⓑ obtained at the pin 1 of IC5 (a) is also sent to breeze way pulse generator consisting of IC5 (b), C39, R77, Q24 and IC5 (c).

The negative sync signal Ⓑ obtained at pin 4 of NOR gate (invertor) IC5 is sent through control-current-differential circuit consisting of C39 and R77, and rectifier D5 to base of switching Q24 and is changed to pulse Ⓒ. The negative breeze way gate pulse Ⓓ obtained at collector of switching Q24 is sent through NOR gate (inverter) IC5 (c) to pin 11 of IC5 (d) E.

The gen-lock signal Ⓐ obtained at emitter of Q13 is also sent to burst gate consisting of Q14 and Q15. The positive blanking (BL) signal Ⓖ is sent to base of Q15 from sync generator IC8. The Q15 turns OFF during positive portion of BL signal and Q15 turns ON during negative portion of BL signal. As a result, sync and burst signal are detected. The detected signal Ⓗ is fed to 4.43 MHz band pass filter consisting of L6 and C29 to remove the low frequency component and detect only burst signal Ⓘ. The detected burst signal is sent through amplifier consisting Q16 to Q20 to pin 12 of NOR gate IC5 (d). The NOR gate IC5 is removed noise where the breeze way position, and pin 13 of IC5 (d) obtained detected burst signal is supplied to pin 35 of sync generator IC8. And the sync generator generates the subcarrier (SC) signal which is synchronized with the detected burst signal.

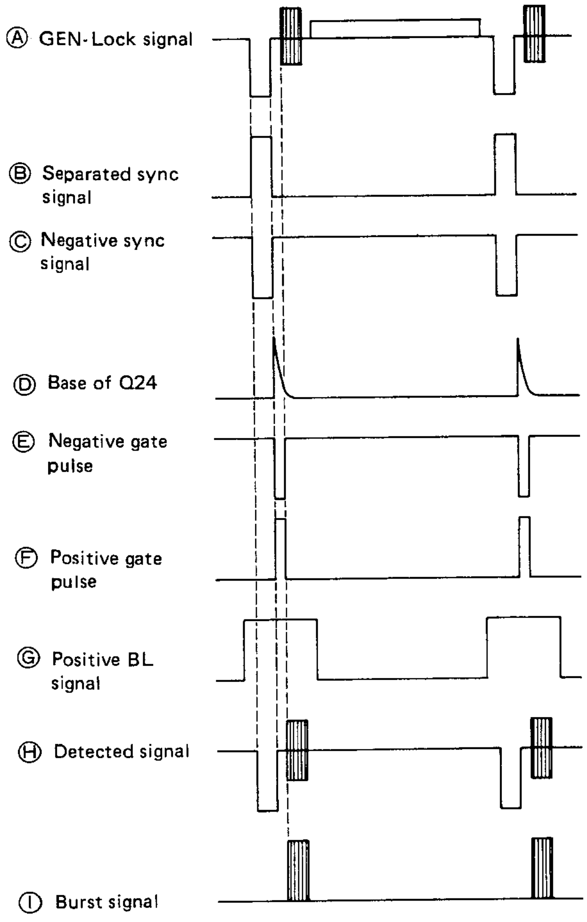


Fig. 11-6-1 Burst Signal

11-7. Gen-Lock 17 MHz Oscillator

Outline

When the sync signal separated from the gen-lock signal is sent to the sync generator IC8, the H sync signal is compared with the horizontal drive (HD) pulse in phase in the sync generator IC8 and converted into the DC voltage which controls this circuit to oscillate the 14 MHz frequency. It is sent to the sync generator IC8 to generate the HD pulse. In this way, the phase lock loop (PLL) circuit is made in the gen-lock/external sync mode and the 17 MHz frequency is controlled to generates the HD pulse whose phase coincides with that of gen-lock sync signal. The sync generator IC8 is reset vertically in the IC8 by the sync signal supplied to the IC8.

Details

When the sync signal separated from the gen-lock signal in the sync separation circuit is sent to pin 37 of sync generator IC8, the HD pulse generated in IC8 and horizontal (H) sync signal separated from the sync signal are compared in phase in IC8. The phase difference is converted into the DC voltage and obtained at pin 45 of IC8. It is fed to the 17 MHz voltage controlled oscillator (VCO) consisting of D8, C54 to C56, C58, L10, IC9 (a) and CT4 (H.LOCK) and controls the oscillating frequency by changing the capacitance of variable capacitance diode D8. The pin 3 of IC9 (a) receives gen-lock detect control from pin 38 of sync generator IC8 when gen-lock/external sync mode, this potential is low level, and start oscillating of 14 MHz.

The 17 MHz frequency is fed back to pins 42 of IC8 through buffer IC9 (b) to generate the HD pulse. In this way, the phase lock loop (PLL) circuit is made and the frequency of 17 MHz VCO is controlled in order to generate the HD pulse whose relative phase matches that of H sync signal of gen-lock sync signal. CT4 (H. LOCK) is a control for setting the lock range of the PLL circuit. The relative phase between the HD pulse and the H gen-lock sync is adjusted by the DC voltage supplied to pin 1 of IC8. It is used to eliminate a horizontal phase difference between incoming gen-lock signal and internal oscillator. VR13 (H. PHASE) is changed DC voltage of supplying to pin 1 of IC8.

11-8. Ext 17 MHz Oscillator Circuit

Outline

In the gen-lock/external sync mode, this circuit oscillates the 17 MHz to make the subcarrier (SC) signal whose frequency/phase is same as the burst signal of gen-lock signal.

Details

In the gen-lock/external sync mode, the SC signal generated in sync generator IC8 and the burst signal separated from the gen-lock signal and sent to pin 35 of IC8 are compared in phase in IC8. The phase difference in comparison is converted into the DC voltage and obtained at pin 36 of IC8 and it is sent through ripple filter consisting of C43, C44, C72, R84 and R86 to 17 MHz voltage controlled crystal oscillator (VCXO) conisiting of crystal oscillator X1, D6, C45 and CT1 (COLOR LOCK) to control the oscillating frequency by changing the capacitance of variable capacitance diode D6.

The 17 MHz frequency is fed back to pins 28 and 29 of IC8 to generate the SC signal. In this way, the phase lock loop (PLL) circuit is made and the frequency of VCXO is controlled in order to generate the SC signal whose frequency and relative phase matches that of gen-lock burst signal.

CT1 (COLOR LOCK) is a control for adjusting the lock range of the PLL circuit.

11-9 SC Phase Shifter

Outline

In the system using multiple cameras, the burst signal on each camera video signal should be adjusted to same phase. This circuit shifts the phase of subcarrier (SC) signal generated in the sync generator IC to adjust the phase of burst signal.

Details

The SC signal obtained at pin 22 of sync generator IC8 is sent to pin 10 of monostable multivibrator IC6 (b). The output of IC6 (b) at pin 12 is fed to pin 25 of sync generator IC8.

11-10 SC Out Circuit

Outline

These circuit receives subcarrier-1 (SC 1), subcarrier-2 (SC 2) signals from sync generator circuit and sends out to SC output connector on rear panel through connector board and other circuits.

Details

The SC1 signal is fed from the sync generator circuit through buffer Q26 to the band pass filter (BPF) CF3 whose center frequency is 4.43 MHz. After harmonics of 4.43 MHz is removed by the BPF, the SC1 signal is fed through buffer Q27, amplifier Q28 and buffer Q29 to push-pull amplifier consisting of Q30 to Q33. The obtained SC1 signal with 4 Vp-p at TP6 is sent to SC output connector through pin 17 (a) of CN27 and connector board.

The SC2 signal is fed from sync generator circuit to the SC.A output IC7 (a), where the 4.43 MHz SC2 signal is count down by 1/2 and the 2.215 MHz frequency is sent out to the other circuit through pin 18 (a) of CN27 from pin 3 of IC7 (a).

12. Mother Board

The mother board contains following circuits.

12-1 Intercom Circuit 41

12-2 C/7-C/BAR Switching Circuit............ 42

12-1 Intercom Circuit

Outline

When the special effect generator (S.E.G.) is used with studio cameras, audio communication is required between cameras and S.E.G.. Therefore intercom circuit is provided.

Details

When the intercom jack is connected to S.E.G. connector CN2, the talk signal is supplied to the cameras through buffer Q1 and pin 9 of CN13. The intercom signals of the cameras are supplied to the S.E.G. intercom jack through pin 10 of CN13 and amplifier Q3, Q4 and Q5.

12-2 C/7-C/BAR Switching Circuit

Outline

This circuit selects video 7 signal and color bar signal and selected signal becomes input video signal. This circuit also supplies high or low control signal to color bar generator circuit on SYNC, C/BAR board for color bar ON/OFF control and video switching circuit on Input A,B,C, and PV-PG board for video switching.

Details

When C/7-C/B select switch is set at C/7 position, high potential is supplied to base of Q10 of color bar generator circuit on SYNC, C/BAR board through pins 19 (a) (b) of CN27 for stop generating color bar signal, pin 8 of TALLY CONT AND gate IC3 (a) on Input A, B, C board and pin 2 of TALLY CONT AND gate IC3 (a) on Input PV-PG board. At this time, the video 7 signal is supplied to video switching circuit through switching Q7.

When C/7-C/B select switch is set at C/B position, low potential is supplied to base of Q10 of color bar generat or circuit or SYNC, C/BAR board through pins 19 (a) (b) of CN27 for generating color bar signal, pin 8 of TALLY CONT AND gate IC3 (a) on Input A, B, C, board and pin 2 of TALLY CONT AND gate IC3 (a) on Input PV-PG board. At this time, color bar signal is supplied to video switching circuit through switching Q6.

13. Connector Board/Termination Board

Outline

Incoming video signals whose receipted at input terminals are supplied to corresponding circuit through buffers respectively.

Signals whose produced inside SEG are sent out the output terminal on the rear panel. The termination switch changes impedance of input terminal for 75 ohms or High-Z.

Details

The input 1-8, DSK and Gen-Lock signals are supplied to the corresponding video input circuit through buffer Q1 to Q11 respectively. When termination switches SW1-SW10 are set to 75 ohms position, input impedance of input terminals become 75 ohms, otherwise high impedance. The incoming red (R), green (G), blue (B) and external pattern signals are supplied to the R.G.B. input mixer circuit on chroma key board through buffers Q11 - Q14 respectively. The high level is supplied to bases of Q20 - Q27 corresponding to the selected input selector to turns Q20 - Q27 ON respoectively, therefore the collectors of Q20 - Q27 is grounded and the tally lamp of the connected cameras are lighted.

- Black burst process circuit

The burst signal Ⓐ fed to buffer Q19, the blanking signal Ⓑ fed to inverter Q32, and the sync signal Ⓒ fed to inverter Q34 are mixed at base of Q18 through matrix resister R89, R201 and R202 respectively. And the mixed signal Ⓓ is supplied to clip circuit consisting of Q18 and Q17, where the blanking level of the mixed signal is suppressed and the black burst signal Ⓔ is supplied to black burst output connector through output Q16 and Q15.

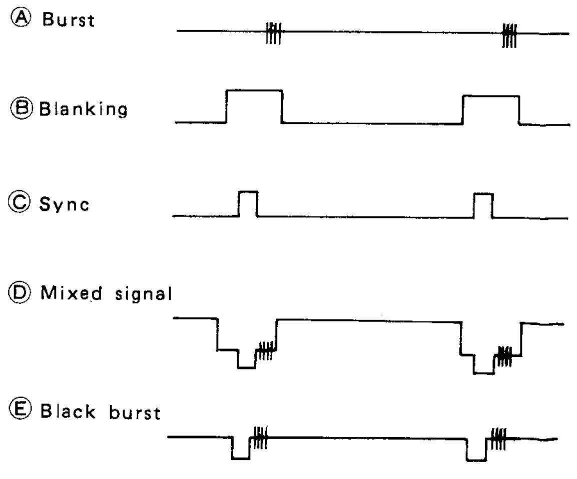


Fig. 13-1 Black burst Signal

- Sync output circuit

The horizontal drive pulse (HD), vertical drive pulse (VD) composite blanking pulse (BL), sync signal (SYNC), and burst flag pulse (BFP) from Sync, C/Bar board are supplied to each corresponding output connector through inverter and buffer respectively.

The subcarrier signal (SC) from Sync, C/Bar board is supplied to SC output connector.

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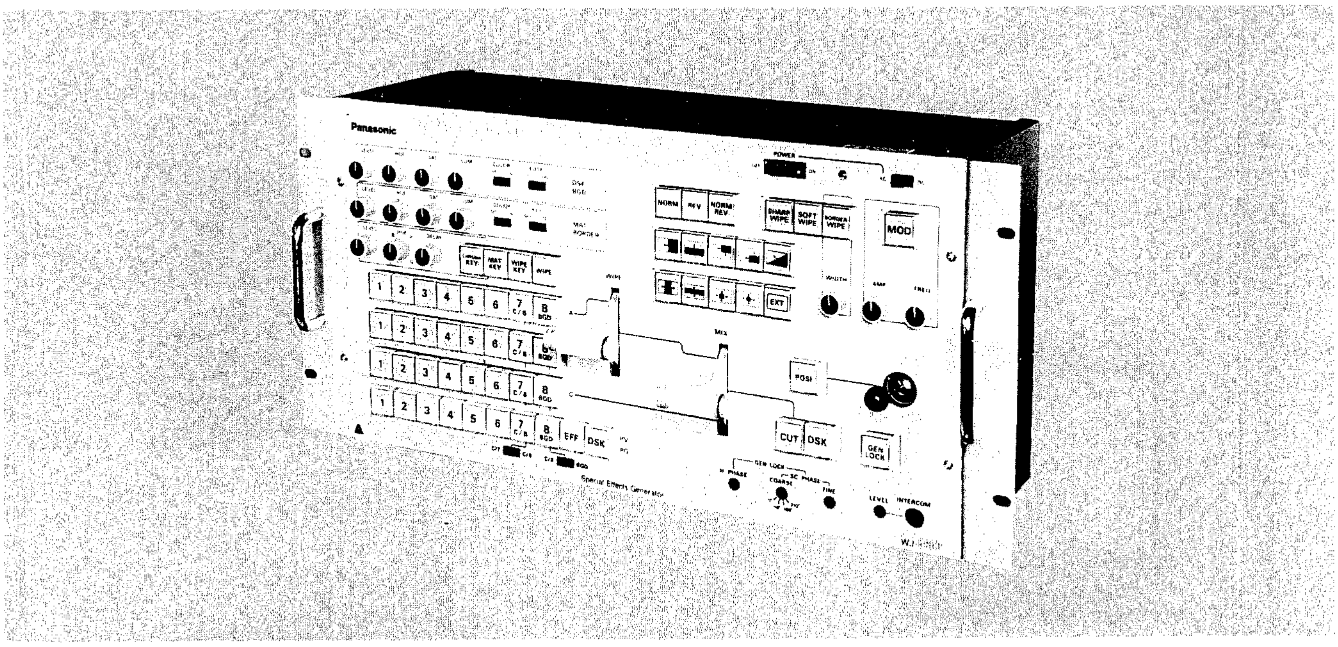
Service Manual

Vol. 2

Adjustment Procedures

Special Effects Generator
WJ-5600



CONTENTS

1. Test Equipment Required 1
2. Disassembling Procedure 1, 2
   - 2-1 For Adjustment 1, 2
   - 2-2 For Lever Unit 2
   - 2-3 For Rear Panel 2
3. Adjustment Procedure .... 3 ～ 28
   - 3-1 Connection and Setting Up for Adjustment 3
   - 3-2 Adjustment .... 4 ～ 28

Panasonic

Matsushita Electric Trading Co., Ltd.
P.O. Box 288, Central Osaka Japan

Adjustment Procedure

1. TEST EQUIPMENT REQUIRED

The following equipments are required for adjustment of Special Effects Generator WJ-5600.

- Oscilloscope (dual trace, delayed, 30MHz bandwidth, with three probes, one must be 1:1)
- Frequency counter
- Underscanned color video monitor (or underscanned B/W video monitor)
- Digital voltmeter (DVM)
- Vectorscope (capable of measuring Differential Gain and Differential Phase)
- Waveform monitor (If waveform monitor is not available, oscilloscope can be used as a substitute.)
- Video signal generator (with built-in color bar, stairstep, modulated stairstep, and crosshatch signal)
- Extension board (Part No. YWJ5500ZK13)

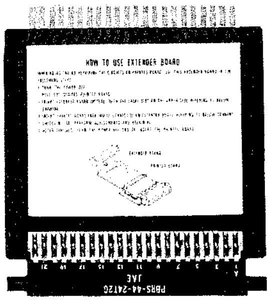


Fig. 1-1

2. Disassembling Procedure

2-1 For Adjustment

- Pull out fourteen knobs on front panel. (Fig. 2-1-1)

Pull out 14 knobs

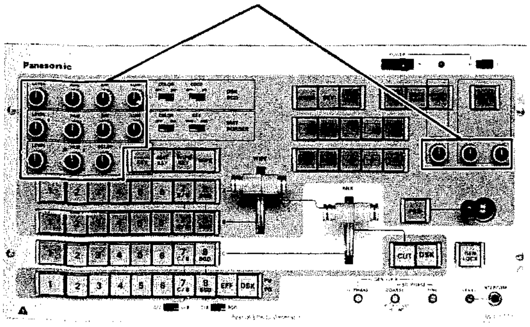


Fig. 2-1-1

- Shift the left side (red mark) of WIPE and MIX lever knob to left, and separate WIPE and MIX lever alternately. (Fig. 2-1-2)

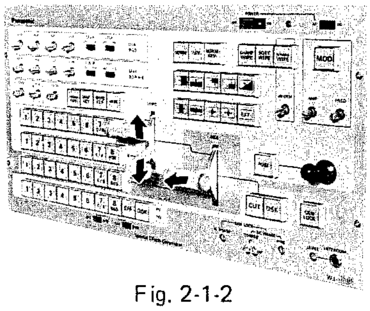
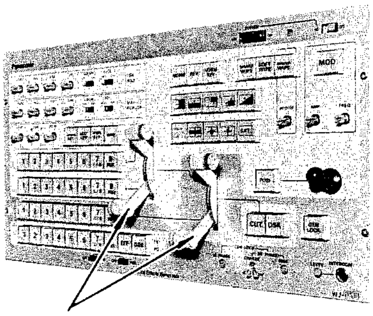


Fig. 2-1-2

- Remove each two screws which hold the WIPE and MIX lever knobs. (Fig. 2-1-3, Fig. 2-1-4)



Remove two screws

Fig. 2-1-3

Remove two screws

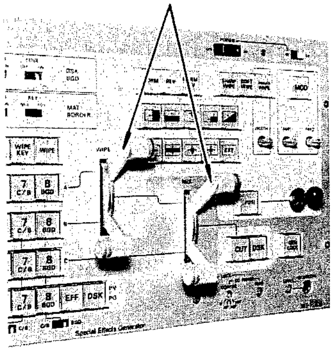
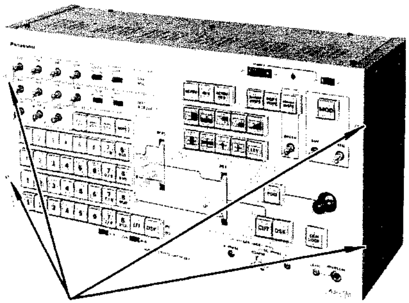


Fig. 2-1-4

- Remove four screws which hold the front panel and remove the front panel from S.E.G unit. (Fig. 2-1-5)



Remove four screws

Fig. 2-1-5

- Remove the Hold plate from S.E.G unit. (Fig. 2-1-6)

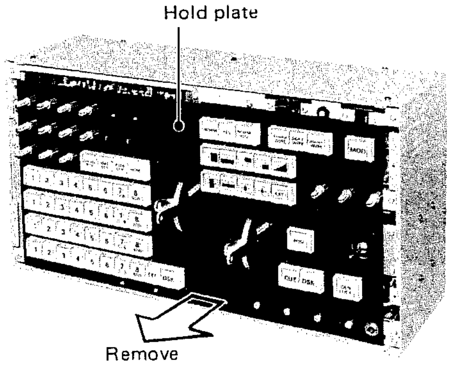

Hold plate
Remove

Fig. 2-1-6

- Remove five screws which hold the top panel and remove the top panel from S.E.G unit. (Fig. 2-1-7)

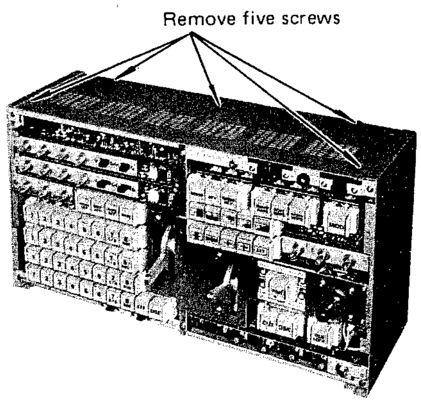

Remove five screws

Fig. 2-1-7

- Remove four screws which hold the bottom panel and remove the bottom panel from S.E.G unit. (Fig. 2-1-8)

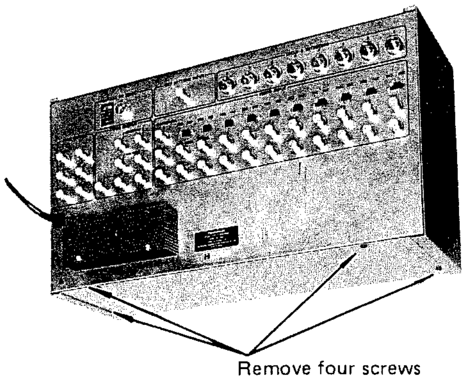

Remove four screws

Fig. 2-1-8

2-2 For Lever Unit

- Remove four screws which hold the Lever Unit and remove the Lever unit by pulling it. (Fig. 2-2-1, Fig. 2-2-2)

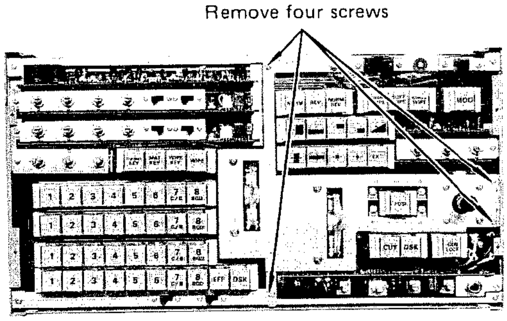

Remove four screws

Fig. 2-2-1

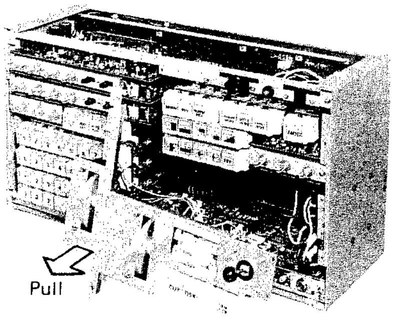


Fig. 2-2-2

2-3 For Rear Panel

- Disconnect seven connectors which connect combination rear panel and connector board with Mother board. (Fig. 2-3-1, Fig. 2-3-2)

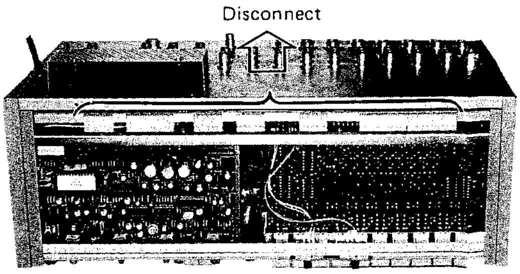

Disconnect

Fig. 2-3-1

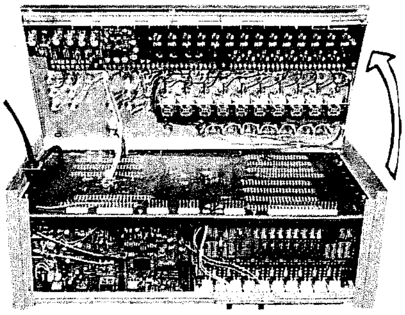


Fig. 2-3-2

3. ADJUSTMENT PROCEDURE

3-1 Connection and Setting Up for Adjustment

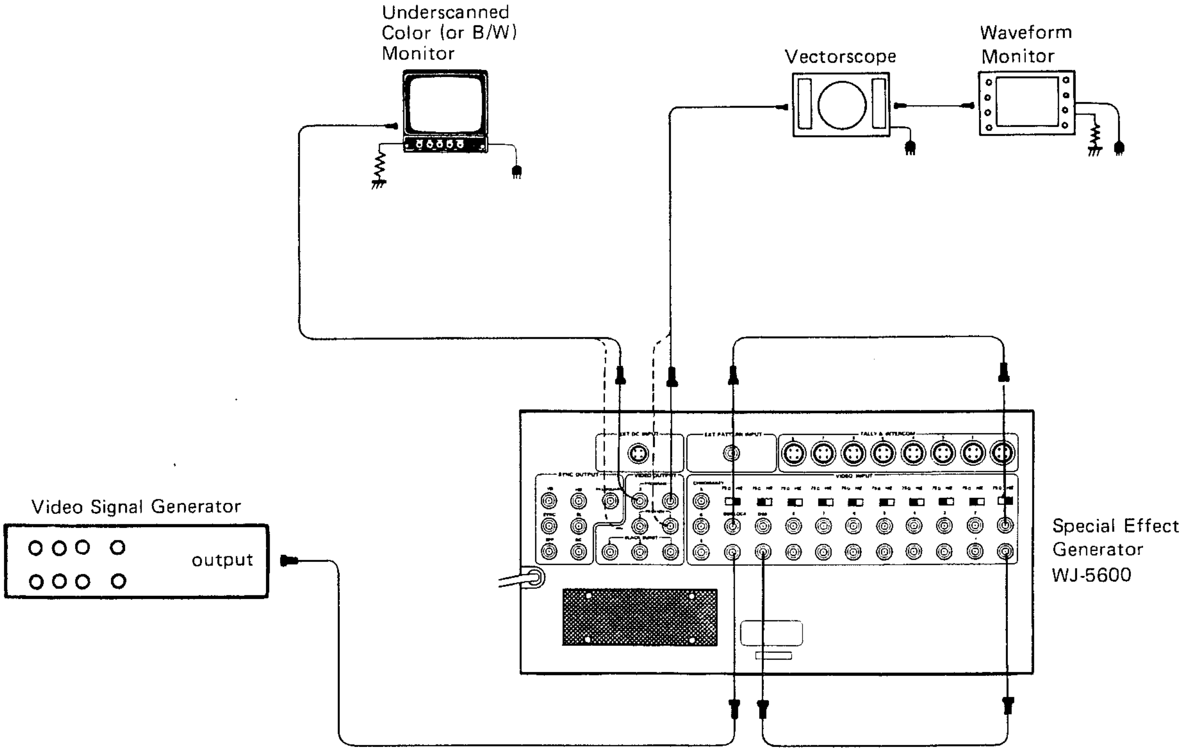

Underscanned
Color (or B/W)
Monitor
Vectorscope
Waveform
Monitor
Video Signal Generator
output
Special Effect
Generator
WJ-5600

Fig. 3-1-1

Connection and Set-up

- Connect the coaxial cables between OUTPUT connector of video signal generator and the Video Input connector DSK through the GEN-LOCK connector and Video Input 1 connector of WJ-5600.
- Set the video termination switch of Video Input 2 to 8 and DSK with 75 ohms position.
- Set the video termination switch of GEN-LOCK and Video Input 1 with Hi-Z position.
- Connect the coaxial cable between PROGRAM-1 (or PREVIEW-1) OUTPUT of WJ-5600 and video input connector of underscanned color video monitor (or underscanned B/W video monitor) when instructed.
- Set the video termination switch of color video monitor with 75 ohms.
- Connect the coaxial cables between PROGRAM-2 (or PREVIEW-2) OUTPUT of WJ-5600 and video input of the waveform monitor through the vectorscope when instructed.
- Terminate the video input of the waveform monitor with 75 ohms.
- Set the GEN-LOCK ON/OFF switch to ON position.
- Set the Cut ON/OFF switch to OFF position.
- Turn ON the power switch of Special Effects Generator for at least 30 minutes prior to adjustment.
  Note : TP in the manual refers to a test point on the printed circuit board.

Extension Board

- When adjusting, use the extension boards except Mother board or Position boards. (standard accessories as shown in Fig. 3-1-2)

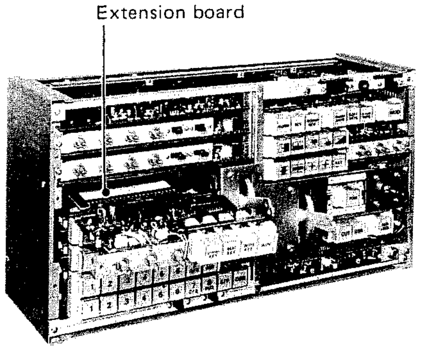

Extension board

Fig. 3-1-2

3-2 Adjustment

- Refer to the separate booklet for the test points and adjusting controls.

(1) +9V adjustment

Test point :	Pin 20 (b) of CN27	Sync,C/Bar Board
Adjust :	VR1 (+9V ADJ)	Mother Board

- Remove the Waveform Gen. Board and Modulation Board from the unit.
- Connect the digital voltmeter (DVM) to pin 20(b) of CN27 on the Sync, C/Bar board.
- Adjust VR1 (+9V ADJ) for +9V ±0.02V.
- Place the Waveform Gen. Board and Modulation Board to the unit.

(2) 4.43MHz adjustment

Test point :	SC Output	Rear Panel
Adjust :	CT2 (4.43MHz ADJ.)	Sync,C/Bar Board

- Set the GEN-LOCK ON/OFF switch to OFF position.
- Connect the frequency counter to SC output connector on rear panel.
- Adjust CT2 (SC FREQUENCY) for 4.433618MHz ± 3Hz.

(3) Field detect adjustment

Test point :	TP8	Sync, C/Bar Board
Adjust :	CT3 (FIELD DETECT)	Sync, C/Bar Board

- Set the GEN-LOCK ON/OFF switch to OFF position.
- Connect the oscilloscope to TP8 on the Sync, C/Bar board.
- Trigger the oscilloscope at H.rate (Use HD output connector on rear panel).
- Set the oscilloscope input coupling selector to DC position.
- Adjust CT3 (FIELD DETECT) so that the signal level becomes 1.8V from ground level.

(4) External sync adjustment

Test points :	TP9	Sync,C/Bar Board
	TP7	Sync,C/Bar Board
Adjusts :	CT4 (H LOCK)	Sync,C/Bar Board
	CT1 (COLOR LOCK)	Sync,C/Bar Board

- Supply color bar or black burst signal to Video Input connector 1 through GEN-LOCK connector from video signal generator.
- Set the GEN-LOCK ON/OFF switch to ON position.
- Connect oscilloscope to TP9 on the Sync, C/Bar board.
- Trigger the oscilloscope at H. rate (Use HD output connector on rear panel).
- Set the oscilloscope input coupling selector to DC position.
- Adjust CT4 (H. LOCK) so that the signal level becomes 2.5V from ground level. (Fig. 3-2-1)
- Connect oscilloscope to TP7 on the Sync, C/Bar board.
- Adjust CT1 (COLOR LOCK) so that the signal level becomes 1.5V from ground level. (Fig. 3-2-2)

Note : Make sure subcarrier frequency of the video signal generator is 4.433618MHz ± 5Hz.

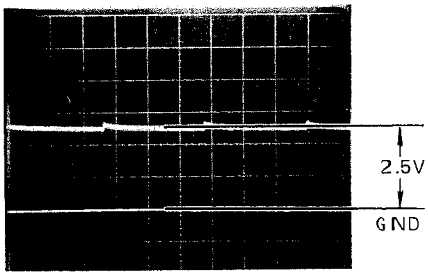


Fig. 3-2-1

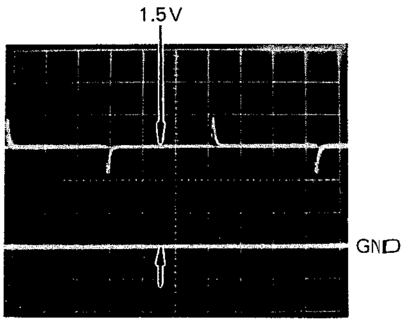


Fig. 3-2-2

(5) Horizontal phase adjustment

Test points :	Program Output	Rear Panel
	Pin 9 (a) of CN27	Sync,C/Bar Board
Adjusts :	VR13 (H. PHASE)	Sync,C/Bar Board

- Supply color bar or black burst signal to Video Input connector 1 through GEN-LOCK connector from video signal generator.
- Connect oscilloscope to Program Output connector on the rear panel and pin 9 (a) of CN27 (VBS IN) on the Sync, C/Bar board.
- Trigger the oscilloscope at H.rate (Use HD output connector on rear panel).

- Expand the H sync period on the oscilloscope.
- Confirm that the sync of VBS signal at pin 9 (a) of CN27 (VBS IN) leads by more than 0.5 μsec and lags more than 0.5μsec sync signal at Program Output connector on the rear panel as VR13 (H. PHASE) is turned through its range.
- After confirming the above step, adjust VR13 so that the leading edges of both sync signals are coincident. (Fig. 3-2-3)

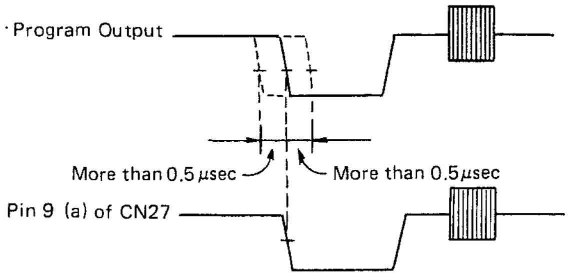


Fig. 3-2-3

(6) Confirmation of subcarrier (SC) phase

Test point :	Program Output	Rear Panel
Adjusts :	SW1 (SC PHASE-COARSE)	Sync,C/Bar Board
	VR12 (SC PHASE-FINE)	Sync,C/Bar Board
Observe :	Vectorscope, Color Video Monitor	

- Supply color bar signal to Video Input connector 1 through GEN-LOCK connector from video signal generator.
- Connect the vectorscope and the color video monitor to Program Output connector.
- Set the C/7, C/B selector switch to color bar (C/B) position.
- Select No. 7 switches on the Video Input A selector and the Video Input B selector.
- Set the MIX lever to top position.
- Supply an external subcarrier signal to the external subcarrier reference (EXT CW ϕREF) connector of vectorscope from the signal generator.
- Set the burst mode (ϕREF) of the vectorscope to the EXT position.
- Set SW1 (SC PHASE COARSE SWITCH) to the 0° position and turn VR12 (SC PHASE FINE) to fully counterclockwise.
- Confirm that the burst phase changes more than 90°, 180° and 270° when SW1 is set to the 90°, 180° and 270° position.
- Confirm that the burst phase changes more than 90°, when VR12 is turned back. (The burst phase changes more than 360° by setting SW1 and VR12.)
- Reset SW1 to the 0° position and return VR12 fully counterclockwise.

(7) Horizontal centering and ½H. pulse adjustment

Test points :	TP5	Waveform Gen. Board
	Pin 2 of CN24	Waveform Gen. Board
	TP6	Waveform Gen. Board
Adjusts :	VR7 (H-CENT)	Waveform Gen. Board
	VR5 (½H. CONT)	Waveform Gen. Board

- Select the WIPE switch on the WIPE/KEY Control.
- Set the positioner (POSI) switch to OFF position.
- Connect oscilloscope to TP5 and pin 2 (a or b) of CN24 (HD) on Waveform Gen. board.
- Trigger the oscilloscope at H.rate (Use HD output connector on rear panel).
- Expand the HD period on the oscilloscope.
- Adjust VR7 (H-CENT) so that the rise timing of TP5 pulse becomes 5.5 μsec delay from decay timing of HD pulse. (Fig. 3-2-4)

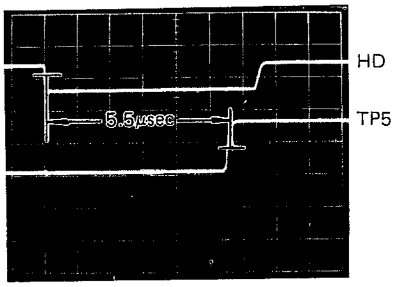


Fig. 3-2-4

- Connect the oscilloscope to TP6 on the Waveform Gen. board.
- Reset expand to normal on the oscilloscope.
- Adjust VR5 (½H. CONT) so that the pulse width becomes ½H. (Fig. 3-2-5)

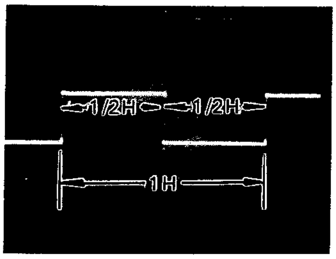


Fig. 3-2-5

(8) Vertical centering and ½V. pulse adjustment

Test points :	TP3	Waveform Gen. Board
	Pin3 of CN24	Waveform Gen. Board
	TP4	Waveform Gen. Board
Adjusts :	VR2 (V-CENT)	Waveform Gen. Board
	VR1 (½V. CONT)	Waveform Gen. Board

- Select the WIPE switch on the WIPE/KEY Control.
- Set the positioner (POSI) switch to OFF position.
- Connect oscilloscope to TP3 and pin 3 (a or b) of CN24 (VD) on Waveform Gen. board.
- Trigger the oscilloscope at V.rate (Use VD output connector on rear panel).
- Expand the VD period on the oscilloscope.
- Adjust VR2 (V-CENT) so that the rise timing of TP3 pulse becomes 800 μsec delay from decay timing of VD signal. (Fig. 3-2-6)

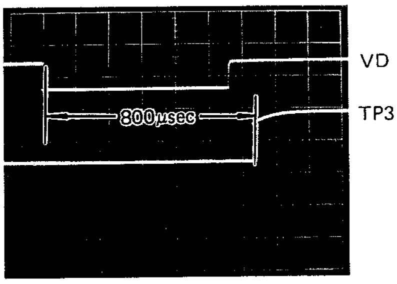


Fig. 3-2-6

- Connect the oscilloscope to TP4 on the Waveform Gen. board.
- Reset expand to normal on the oscilloscope.
- Adjust VR1 (½V. CONT) so that the pulse width becomes ½V. (Fig. 3-2-7)

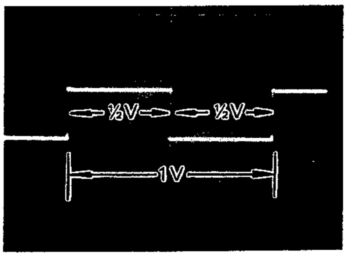


Fig. 3-2-7

(9) Horizontal sawtooth adjustment

Test point :	TP1	Waveform Gen. Board
Adjust :	VR9 (H.SAWTOOTH)	Waveform Gen. Board

- Select the WIPE switch on the WIPE/KEY Control.
- Select the SHARP WIPE switch on the Wipe Mode Selector.
- Select the wipe pattern of ◨ on the Wipe Pattern Selector.
- Connect oscilloscope to TP1 on Waveform Gen. board.
- Trigger the oscilloscope at H.rate (Use HD output connector on rear panel).
- Adjust VR9 (H.SAWTOOTH) so that the H.sawtooth amplitude becomes 1.9Vp-p. (Fig. 3-2-8)

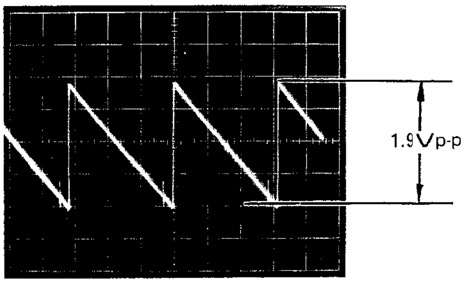


Fig. 3-2-8

(10) Horizontal parabola adjustment

Test point :	TP1	Waveform Gen. Board
Adjust :	VR8 (H.PARABOLA)	Waveform Gen. Board

- Select the WIPE switch on the WIPE/KEY Control.
- Select the SHARP WIPE switch on the Wipe Mode Selector.
- Select the wipe pattern of ⊞ on the Wipe Pattern Selector.
- Connect oscilloscope to TP1 on Waveform Gen. board.
- Trigger the oscilloscope at H.rate (Use HD output connector on rear panel).
- Adjust VR8 (H.PARABOLA) so that the H.parabola amplitude becomes 1.8Vp-p. (Fig. 3-2-9)

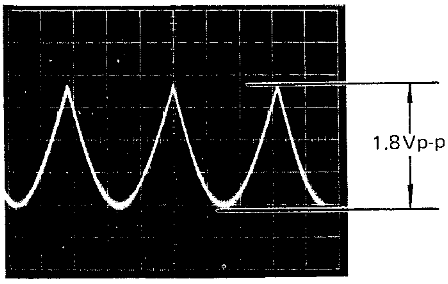


Fig. 3-2-9

(11) Horizontal triangle adjustment

Test point :	TP1	Waveform Gen. Board
Adjust :	VR4 (H.TRIANGLE)	Waveform Gen. Board

- Select the WIPE switch on the WIPE/KEY Control.
- Select the SHARP WIPE switch on the Wipe Mode Selector.
- Select the wipe pattern of ◫ on the Wipe Pattern Selector.
- Connect oscilloscope to TP1 on Waveform Gen. board.
- Trigger the oscilloscope at H.rate (Use HD output connector on rear panel).
- Adjust VR4 (H.TRIANGLE) so that the H.triangle amplitude becomes 1.6Vp-p. (Fig. 3-2-10)

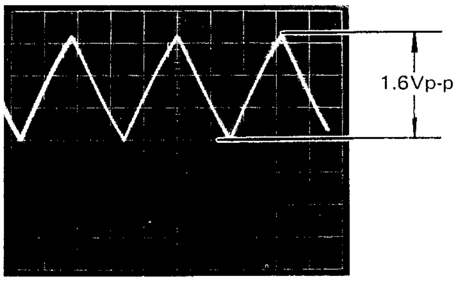


Fig. 3-2-10

Confirmation

- Supply convergence video signal to Video Input connector 1 through GEN-LOCK connector from video signal generator.
- Connect the underscanned video monitor to Program Output connector.
- Set C/8, BGD Selector switch to BGD position.
- Selects No. 1 switch on the Video Input A selector and No. 8 switch on the Video Input B selector.
- Select the WIPE switch on the WIPE/KEY control.
- Select the normal (NORM) switch on the Normal/ Reverse selector.
- Select wipe pattern of ◫ on the Wipe Pattern Selector.
- Move the Wipe lever from top to bottom or bottom to top so that the wipe edge reaches to left edge and right edge at simultaneously on the monitor screen, if not, readjust VR7 (H-CENT) on the Waveform Gen. board.
- Move the Wipe lever so that the wipe signal becomes as thin as possible.
- Confirm the wipe signal starts at the center position on the monitor screen, if not, readjust VR5 (1/2 H.CONT).
- Repeat to adjust VR5 and VR7 alternately until wipe signal starts at the center position also reaches to left and right edge at simultaneously on the monitor screen when move the Wipe lever from top to bottom or bottom to top. (Fig. 3-2-11)

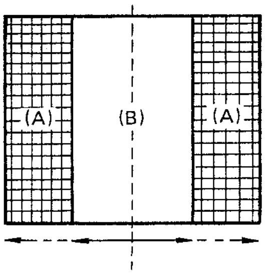


Fig. 3-2-11

(12) Vertical sawtooth adjustment

Test point :	TP2	Waveform Gen. Board
Adjust :	VR13 (V.SAWTOOTH)	Waveform Gen. Board

- Select the WIPE switch on the WIPE/KEY control.
- Select the SHARP WIPE switch on the Wipe Mode Selector.
- Select the wipe pattern of ⬓ on the Wipe Pattern Selector.
- Connect oscilloscope to TP2 on Waveform Gen. board.
- Trigger the oscilloscope at V.rate (Use VD output connector on rear panel).
- Adjust VR13 (V.SAWTOOTH) so that the V.sawtooth amplitude becomes 1.25Vp-p. (Fig. 3-2-12)

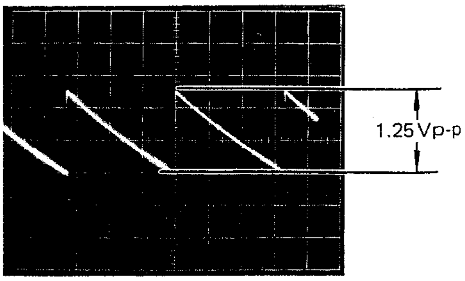


Fig. 3-2-12

(13) Vertical negative sawtooth adjustment

Test point :	TP2	Waveform Gen. Board
Adjust :	VR12 (V.NEG SAWTOOTH)	Waveform Gen. Board

- Select the WIPE switch on the WIPE/KEY Control.
- Select the SHARP WIPE switch on the Wipe Mode Selector.
- Select the wipe pattern of ◳ on the Wipe Pattern Selector.
- Connect oscilloscope to TP2 on Waveform Gen. board.
- Trigger the oscilloscope at V.rate (Use VD output connector on rear panel).
- Adjust VR12 (V.NEG SAWTOOTH) so that the V.negative sawtooth amplitude becomes 1.0Vp-p. (Fig. 3-2-13)

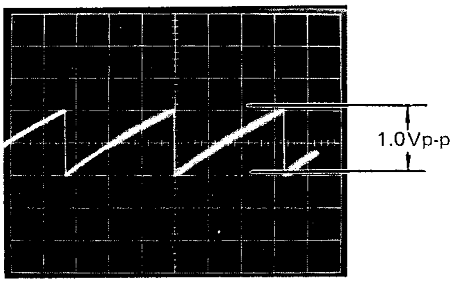


Fig. 3-2-13

(14) Vertical parabola adjustment

Test point :	TP2	Waveform Gen. Board
Adjust :	VR11 (V.PARABOLA)	Waveform Gen. Board

- Select the WIPE switch on the WIPE/KEY Control.
- Select the SHARP WIPE switch on the Wipe Mode Selector.
- Select the wipe pattern of ⊞ on the Wipe Pattern Selector.
- Connect oscilloscope to TP2 on Waveform Gen. board.
- Trigger the oscilloscope at V.rate (Use VD output connector on rear panel).
- Adjust VR11 (V.PARABOLA) so that the V.parabola amplitude becomes 0.6Vp-p. (Fig. 3-2-14)

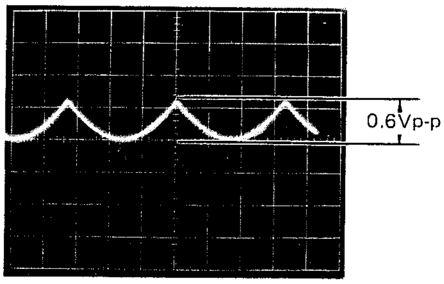


Fig. 3-2-14

(15) Vertical triangle adjustment

Test point :	TP2	Waveform Gen. Board
Adjust :	VR10 (V.TRIANGLE)	Waveform Gen. Board

- Select the WIPE switch on the WIPE/KEY Control.
- Select the SHARP WIPE switch on the Wipe Mode Selector.
- Select the wipe pattern of ⊟ on the Wipe Pattern Selector.
- Connect oscilloscope to TP2 on Waveform Gen. board.
- Trigger the oscilloscope at V.rate (Use VD output connector on rear panel).
- Adjust VR10 (V.TRIANGLE) so that the V.triangle amplitude becomes 1.2Vp-p. (Fig. 3-2-15)

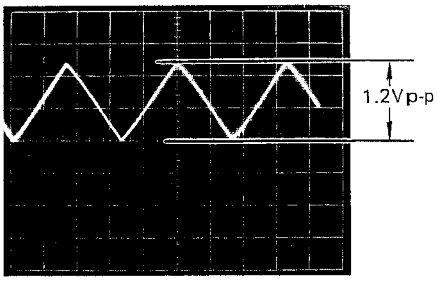


Fig. 3-2-15

Confirmation

- Supply convergence video signal to Video Input connector 1 through GEN-LOCK connector from video signal generator.
- Connect the underscanned video monitor to Program Output connector.
- Set C/8, BGD Selector switch to BGD position.
- Selects No. 1 switch on the Video Input A selector and No. 8 switch on the Video Input B selector.
- Select the WIPE switch on the WIPE/KEY control.
- Select wipe pattern of ⊟ on the Wipe Pattern Selector.
- Move the Wipe lever from top to bottom or bottom to top so that the wipe edge reaches to upper edge and bottom edge at simultaneously on the monitor screen, if not, readjust VR2 (V-CENT) on the Waveform Gen. board.
- Move the Wipe lever so that the wipe signal becomes as thin as possible.
- Confirm the wipe signal starts at the center position on the monitor screen, if not, readjust VR1 (1/2 V.CONT).
- Repeat to adjust VR1 and VR2 alternately until wipe signal starts at the center position, also reaches upper and bottom edge at simultaneously on the monitor screen, when move the Wipe lever from top to bottom or bottom to top. (Fig. 3-2-16)

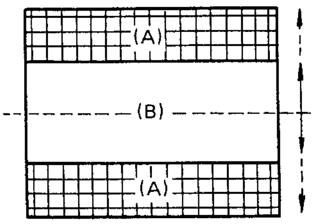


Fig. 3-2-16

(16) H. V. positioner adjustment

Test point :	Program Output	Rear Panel
Adjust :	VR6 (H.POSITION)	Waveform Gen. Board
	VR3 (V.POSITION)	Waveform Gen. Board
Observe :	Underscanned color (or B/W) video monitor	

- Connect the underscanned color (or B/W) video monitor to the Program Output connector.
- Supply convergence video signal to Video Input connector 1 through the GEN-LOCK connector from the video signal generator.
- Selects No. 1 switch on the Video Input A selector and No. 8 switch on the Video Input B selector.
- Select the WIPE switch on the WIPE/KEY control.
- Select the SHARP WIPE switch on the Wipe Mode Selector.
- Select wipe mode of ⊞ on the Wipe Pattern Selector.
- Set the Positioner (POSI) ON/OFF switch to ON position.
- Set the Mix lever to top position.
- Set the Wipe lever so that the circle appear as shown in Fig. 3-2-17.
- Adjust VR6 (H.POSITION) so that the rest of circle becomes same (A=B) when positioner lever is moved to left and right ends.
- Adjust VR3 (V.POSITION) so that the rest of circle becomes same (C=D) when positioner lever is moved to upper and lower ends. (Fig. 3-2-17)

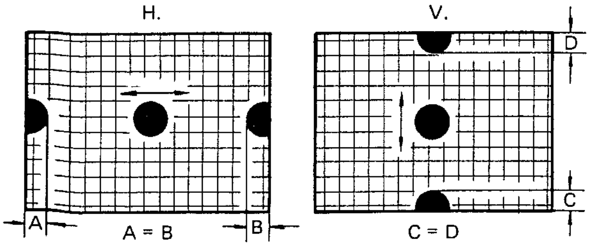


Fig. 3-2-17

(17) Horizontal and vertical wipe balance adjustment

Test Point :	Program Output	Rear Panel
Adjust :	VR8 (H.WIPE BALANCE-1)	Modulation Board
	VR9 (H.WIPE BALANCE-2)	Modulation Board
	VR6 (V.WIPE BALANCE-1)	Modulation Board
	VR7 (V.WIPE BALANCE-2)	Modulation Board
Observe :	Underscanned color (or B/W) video monitor	

- Supply convergence video signal to Video Input connector 1 through GEN-LOCK connector from video signal generator.
- Connect the underscanned color (or B/W) video monitor to Program Output connector.
- Selects No. 1 switch on the Video Input A Selector, and No. 8 switch on the Video Input B Selector.
- Select the SHARP WIPE switch on the Wipe Mode Selector.
- Select the WIPE switch on the WIPE/KEY control.
- Set Wipe Border Modulation (MOD) switch to OFF position.
- Select Normal (NORM) switch on the Normal/Reverse control.
- Select wipe pattern of ◨ on the Wipe Pattern Selector.
- Set the Mix lever to top position.
- Adjust VR8 (H.WIPE BALANCE-1) so that the wipe edge reaches to the monitor screen edge when move the Wipe lever from top to lower and stop it at the point wherethe just before the Wipe lever touch lower limit switch.
- Adjust VR9 (H.WIPE BALANCE-2) so that the wipe edge reaches to the monitor screen edge when move the Wipe lever from bottom to upper and stop it at the point where the just before the Wipe lever touch upper limit switch.
- Select wipe pattern of ◪ on Wipe Pattern Selector.
- Adjust VR6 (V.WIPE BALANCE-1) so that the wipe edge reaches to upper edge and side edge at simultaneously on the monitor screen when move the Wipe lever from top to lower and stop it at the point where the just before the Wipe lever touch lower limit switch.
- Adjust VR7 (V.WIPE BALANCE-2) so that the wipe edge reaches to upper edge and side edge at simultaneously on the monitor screen when move the Wipe lever from bottom to upper and stop it at the point where the just before the Wipe lever touch upper limit switch. (Fig. 3-2-18)

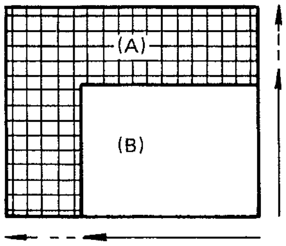


Fig. 3-2-18

Confirmation

- Supply convergence video signal to Video Input connector 1 through GEN-LOCK connector.
- Connect the underscanned video monitor to the Program Output connector.
- Set the C/8, BGD Selector to BGD position.
- Selects No. 1 switch on the Video Input A Selector and No. 8 switch on the Video Input B Selector.
- Select the normal (NORM) switch on the Normal/Reverse Selector.
- Select the WIPE switch on the WIPE/KEY Control.
- Select the SHARP WIPE on the Wipe Mode Selector.
- Select wipe pattern of ◳ on the Wipe Pattern Selector.
- Confirm the wipe edge reaches to bottom edge and left edge at simultaneously on the monitor screen when Wipe lever is moved from top to lower and from bottom to upper, if not, readjust VR12 (V. NEG SAWTOOTH) on the Waveform Gen. board. (Fig. 3-2-19)
- Select wipe pattern of ◪ on the Wipe Pattern Selector.
- Confirm the wipe edge reaches to both corner at simultaneously on the monitor screen when Wipe lever is moved from top to lower and from bottom to upper, if not, readjust VR13 (V. SAWTOOTH) on the Waveform Gen. board. (Fig. 3-2-20)
- Select wipe pattern of ◲ on the Wipe Pattern Selector.
- Confirm the wipe edge reaches to upper edge and left edge on the video monitor at simultaneously when Wipe lever is moved from top to lower and from bottom to upper, if not, readjusts VR6 (V.WIPE BALANCE-1) and VR7 (V.WIPE BALANCE-2) on the Modulation Board. (Fig. 3-2-18)
- Repeat to adjust VR12, VR13 on the Waveform Gen. board and VR6, VR7 on the Modulation board until three patterns of ◳, ◪ and ◲ are properly effected when Wipe lever is moved.
- Select wipe pattern of ⊞ on the Wipe Pattern Selector.
- Confirm the wipe edge reaches to bottom, upper, left and right edge on the monitor screen simultaneously when Wipe lever is moved from top to lower and from bottom to upper, if not, readjusts VR10 (V. TRIANGLE) on the Waveform Gen. board.

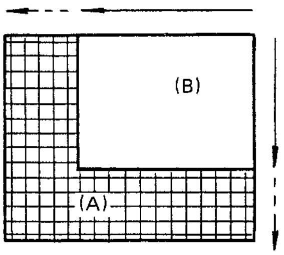


Fig. 3-2-19

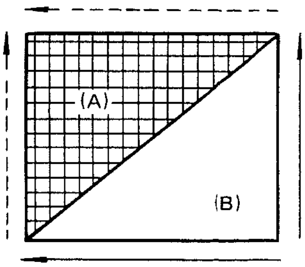


Fig. 3-2-20

(18) Border pulse adjustment

Test points :	TP2	Modulation Board
	TP3	Modulation Board
Adjusts :	VR5	Modulation Board
	(BORDER PULSE LEVEL)	
	VR4	Modulation Board
	(BORDER POSITION)	
Observe :	Waveform monitor	

- Supply stairstep video signal to Video Input connector 1 through GEN-LOCK connector from the video signal generator.
- Select the WIPE switch on the WIPE/KEY control.
- Select the BORDER WIPE switch on the Wipe Mode Selector.
- Set C/8, BGD Selector to BGD position.
- Select the normal (NORM) switch on the Normal/Reverse Selector.
- Selects No. 1 switch on the Video Input A Selector and No. 8 switch on the Video Input B Selector.
- Select wipe pattern of ⬓ on the Wipe Pattern Selector.
- Set the Positioner (POSI) ON/OFF Switch to OFF position.
- Set the Wipe lever to middle position.
- Set the Mix lever to top position.
- Connect the video monitor to the Program Output connector.
- Connects the oscilloscope to TP2 and TP3 on the Modulation Board.
- Trigger the oscilloscope at V.rate (Use VD output connector on rear panel).
- Adjust VR5 (BORDER PULSE LEVEL) so that the level of TP2 and TP3 signals become same (A = B). (Fig. 3-2-21)

- Connect the oscilloscope to Program Output connector or observe waveform monitor.
- Control the WIDTH (Border Wipe Width Control) so that the border line becomes as thin as possible.
- Adjust VR4 (BORDER POSITION) so that the border line is overlayed the wipe edge. (Fig. 3-2-22)

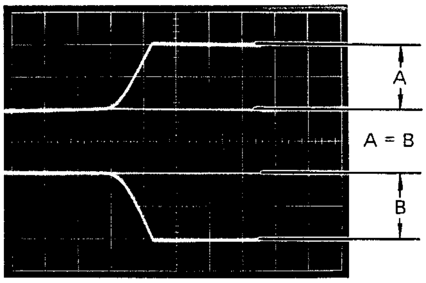


Fig. 3-2-21

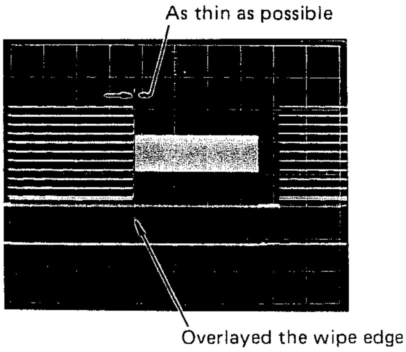


Fig. 3-2-22

(19) External wipe pattern DC level adjustment

Test point :	TP1	Modulation Board
Adjust :	VR10 (EXT PATTERN DC LEVEL)	Modulation Board

- Supply stairstep video signal to EXT PATTERN INPUT connector.
- Select wipe pattern of EXT on Wipe Pattern Selector.
- Connect oscilloscope to TP1 on Modulation board.
- Trigger the oscilloscope at H.rate (Use HD output connector on rear panel).
- Set the oscilloscope input coupling selector to DC position.
- Adjust VR10 (EXT PATTERN DC LEVEL) so that the blanking level becomes 3.0V from ground level. (Fig. 3-2-23)

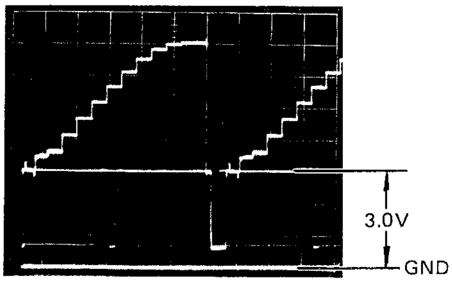
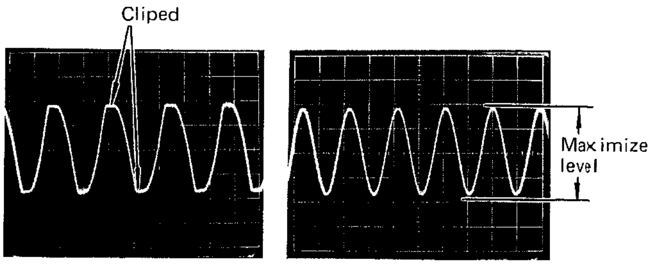


Fig. 3-2-23

(20) Wipe border modulation frequency adjustment

Test point :	TP5	Modulation Board
Adjust :	VR11 (FREQUENCY PRESET)	Modulation Board

- Select the WIPE switch on the WIPE/KEY Control.
- Set the Wipe Border Modulation (MOD) switch to ON position.
- Turn the VR2 (BORDER MODULATION FREQUENCY) to fully counterclockwise.
- Turn the VR3 (BORDER MODULATION AMP) to fully clockwise.
- Connect the oscilloscope to TP5 on the Modulation board.
- Adjust VR11 (FREQUENCY PRESET) so that the sine wave becomes maximum level(with unclip sine wave). (Fig. 3-2-24)



NO GOOD GOOD

Fig. 3-2-24

(21) BL killer DC bias adjustment

Test point :	TP2	Output Board
Adjust :	VR3 (BL KILLER DC BIAS-1)	Output Board

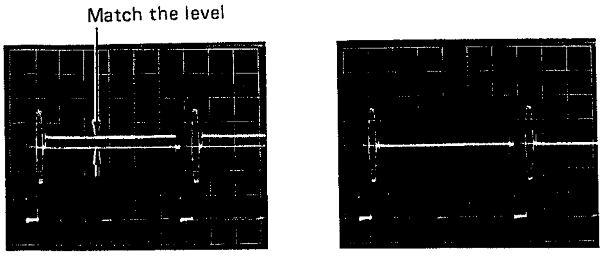
- Connect digital voltmeter (DVM) to TP2 on output board.
- Adjust VR3 (BL KILLER DC BIAS-1) to +5.5V.

(22) Program setup adjustment

Test point :	TP6	Output Board
Adjust :	VR2 (PROGRAM SETUP-1)	Output Board

- Select No. 2 switch on the Video Input Preview/Program selector (Non video signal is supplied on No.2).
- Set the CUT ON/OFF switch to ON position.
- Connect oscilloscope to TP6 on Output board.

- Trigger the oscilloscope at H.rate (Use HD output connector on rear panel).
- Adjust VR2 (PROGRAM SETUP-1) so that the setup level becomes same as blanking level. (Fig. 3-2-25)


Match the level

NO GOOD GOOD

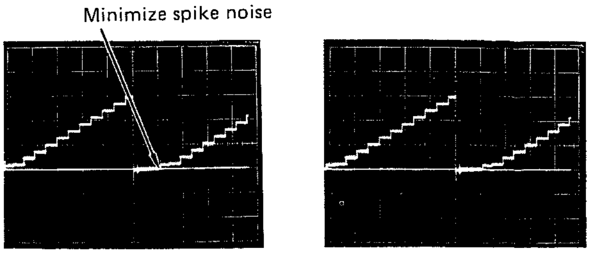
Fig. 3-2-25

(23) Program output BL spike noise compensation adjustment

Test point :	TP3	Output Board
Adjusts :	*VR4 (PROGRAM GAIN-1)	Output Board
	VR5 (BL SPIKE COMP.-1)	Output Board
	*VR6 (PROGRAM GAIN-2)	Output Board

- Supply stairstep video signal to Video Input connector 1 through GEN-LOCK connector from video signal generator.
- Select No. 1 switches on the Video Input Preview/Program selector.
- Set CUT ON/OFF switch to ON position.
- Connect oscilloscope to TP3 on the Output board.
- Trigger the oscilloscope at H.rate (Use HD output connector on rear panel).
- *Turn the VR4 (PROGRAM GAIN-1) to fully clockwise and VR6 (PROGRAM GAIN-2) to fully counterclockwise.
- Adjust VR5 (BL SPIKE COMP.-1) so that the spike noise on the blanking period becomes minimum. (Fig. 3-2-26)

***Asterisk marked of adjustments are subjected to delete in future production.**


Minimize spike noise

NO GOOD GOOD

Fig. 3-2-26

(24) Program output DG, DP adjustment

Test point :	Program Output	Rear Panel
Adjust :	VR7 (PROGRAM DG, DP)	Output Board
Observe :	Vectorscope	

- Supply modulated stairstep video signal to video input connector 1 through GEN-LOCK connector from video signal generator.
- Connect vectorscope to Program Output connector.
- Select No. 1 switch on the Video Input Preview/Program selector.
- Set CUT ON/OFF switch to ON position.
- Adjust VR7 (PROGRAM DG, DP) so that the DG, DP becomes minimum on the vectorscope.

(25) Program output video, burst and sync gain adjustment

Test point :	Program Output	Rear Panel
Adjusts :	VR9 (PROGRAM GAIN-3)	Output Board
	VR10 (BURST GAIN-1)	Output Board
	VR11 SYNC GAIN-1)	Output Board
Observe :	Waveform monitor	

- Supply stairstep video signal to Video Input connector 1 through GEN-LOCK connector from video signal generator.
- Select No. 1 switch on the Video Input Preview/Program selector.
- Set the CUT ON/OFF switch to ON position.
- Connect oscilloscope with 75 ohms termination to Program Output connector or observe waveform monitor.

- Trigger the oscilloscope at H.rate (Use HD output connector on rear panel).
- Adjust VR9 (PROGRAM GAIN-3) so that the video level from blanking to top stair becomes 0.7Vp-p.
- Adjust VR10 (BURST GAIN-1) so that the burst gain becomes 0.3Vp-p.
- Adjust VR11 (SYNC GAIN-1) so that the sync gain becomes 0.3Vp-p.
- Adjust VR9, VR10 and VR11 alternately until the each gain becomes correct levels. (Fig. 3-2-27)

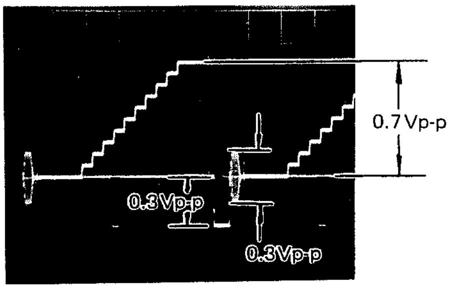


Fig. 3-2-27

(26) Preview BL killer DC bias adjustment

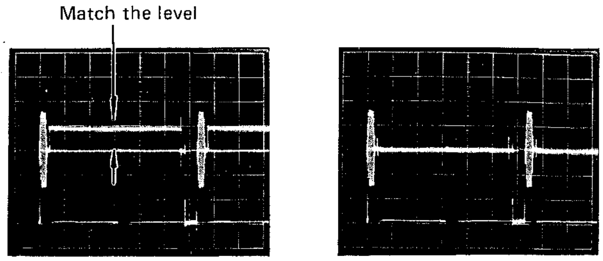
Test point :	TP13	Output Board
Adjust :	VR23 (BL KILLER DC BIAS-2)	Output Board

- Connect digital voltmeter (DVM) to TP13 on Output board.
- Adjust VR23 (BL KILLER DC BIAS-2) for +5.5V.

(27) Preview setup adjustment

Test point :	TP15	Output Board
Adjust :	VR21 (PREVIEW SETUP)	Output Board

- Select No. 2 switch on the Video Input Preview/Program selector (Non video signal is supplied on No. 2).
- Connect the oscilloscope to TP15 on the Output board.
- Trigger the oscilloscope at H.rate (Use HD output connector on rear panel).
- Adjust VR21 (PREVIEW SETUP) so that the setup level becomes the same as blanking level. (Fig. 3-2-28)



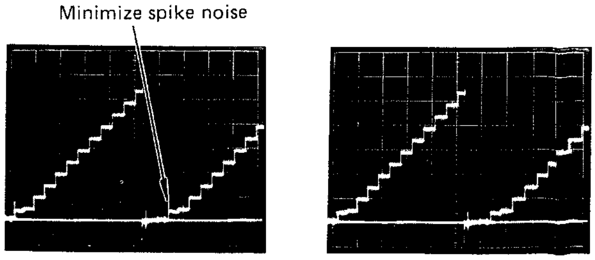
NO GOOD GOOD

Fig. 3-2-28

(28) Preview output BL spike noise compensation adjustment

Test point :	TP14	Output Board
Adjusts :	*VR22 (PREVIEW GAIN-1)	Output Board
	VR24 (BL SPIKE COMP.-2)	Output Board
	*VR25 (PREVIEW GAIN-2)	Output Board

- Supply stairstep video signal to Video Input connector 1 through GEN-LOCK connector from video signal generator.
- Select No. 1 switch on the Video Input Preview/Program selector.
- Connect oscilloscope to TP14 on Output board.
- Trigger the oscilloscope at H.rate (Use HD output connector on rear panel).
- *Set VR22 (PREVIEW GAIN-1) to fully clockwise and VR25 (PREVIEW GAIN-2) to fully counterclockwise.
- Adjust VR24 (BL SPIKE COMP.-2) for minimum spike noise. (Fig. 3-2-29)



NO GOOD GOOD

Fig. 3-2-29

*** Asterisk marked of adjustments are subjected to delete in future production.**

(29) Preview output DG, DP adjustment

Test point :	Preview Output	Rear Panel
Adjust :	VR26 (PREVIEW DG, DP)	Output Board
Observe :	Vectorscope	

- Supply modulated stairstep video signal to Video Input connector 1 through GEN-LOCK connector from video signal generator.
- Connect the oscilloscope to Preview Output connector.
- Select No. 1 switch on the Preview/Program selector.
- Adjust VR26 (PREVIEW DG, DP) so that the DG, DP becomes minimum on the vectorscope.

(30) Preview output video, burst and sync gain adjustment

Test point :	Preview Output	Rear Panel
Adjusts :	VR29 (PREVIEW GAIN-3)	Output Board
	VR30 (BURST GAIN-2)	Output Board
	VR31 (SYNC GAIN-2)	Output Board
Observe :	Waveform monitor	

- Supply stairstep video signal to Video Input connector 1 through GEN-LOCK connector from video signal generator.
- Select No. 1 switch on the Video Input Preview/Program selector.
- Set the CUT ON/OFF switch to OFF position.
- Connect the oscilloscope with 75 ohms termination to Preview Output connector or observe waveform monitor.
- Trigger the oscilloscope at H.rate (Use HD output connector on rear panel).
- Adjust VR29 (PREVIEW GAIN-3) so that the video level from blanking to top stair becomes 0.7Vp-p.
- Adjust VR30 (BURST GAIN-2) so that the burst gain becomes 0.3Vp-p.
- Adjust VR31 (SYNC GAIN-2) so that the sync gain becomes 0.3Vp-p.
- Adjust VR29, VR30 and VR31 alternately until the each gain becomes correct levels. (Fig. 3-2-30)

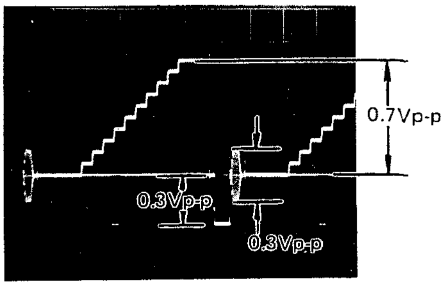


Fig. 3-2-30

(31) Wipe DC bias adjustment

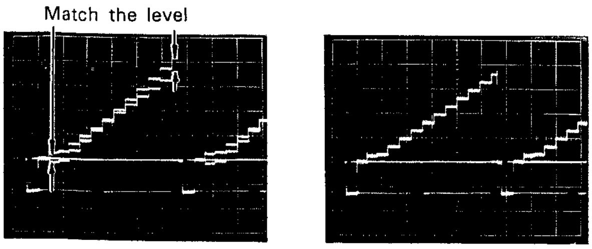
Test point :	TP13	Effect, Mix Board
Adjust :	VR25 (WIPE DC BIAS)	Effect, Mix Board

- Connect digital voltmeter to TP13 on the Effect, Mix Board.
- Adjust VR25 (WIPE DC BIAS) for +5V.

(32) Gain and pedestal balance adjustment

Test point :	TP12	Effect, Mix Board
Adjusts :	VR27 (CH-B GAIN)	Effect, Mix Board
	VR28 (CH-B SETUP)	Effect, Mix Board
	* VR24 (EFFECT GAIN-1)	Effect, Mix Board

- Supply the stairstep video signal to Video Input connector 1 through GEN-LOCK connector from video signal generator.
- Select No. 1 switches on the Video Input A selector and the Video Input B selector.
- Select the Wipe switch on the WIPE/KEY control.
- Select wipe pattern of ⬓ on the Wipe Pattern Selector.
- Set the Wipe lever to middle position.
- Set the Mix lever to top position.
- Connect the oscilloscope to TP12 on the Effect, Mix board.
- Trigger the oscilloscope at H.rate (Use HD output connector on rear panel).
- *● Turn the VR24 (EFFECT GAIN-1) to fully counter-clockwise.
- Adjust VR27 (CH-B GAIN) and VR28 (CH-B SETUP) so that the video level and pedestal level of input B stairstep signal is overlayed input A stairstep signal. (Fig. 3-2-31)



NO GOOD GOOD

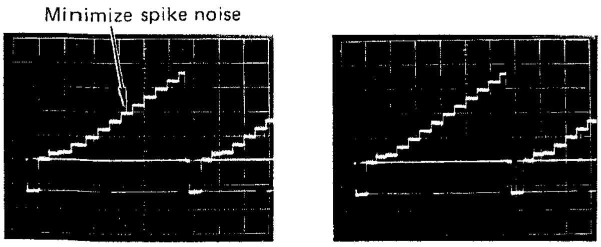
Fig. 3-2-31

*** Asterisk marked of adjustments are subjected to delete in future production.**

(33) Wipe spike compensation adjustment

Test point :	TP12	Effect, Mix Board
Adjust :	VR26 (WIPE EDGE SPIKE COMP.)	Effect, Mix Board

- Supply stairstep video signal to Video Input Connector 1 through GEN-LOCK connector from video signal generator.
- Select wipe pattern of ◨ on the Wipe Pattern Selector.
- Select the Wipe switch on the WIPE/KEY control.
- Set the Wipe lever to middle position.
- Set the Mix lever to top position.
- Connect oscilloscope to TP12 on Effect, Mix Board.
- Trigger the oscilloscope at H.rate (Use HD output connector on rear panel).
- Adjust VR26 (WIPE EDGE SPIKE COMP.) for minimum spike noise. (Fig. 3-2-32)



NO GOOD GOOD

Fig. 3-2-32

(34) Border wipe DC adjustment

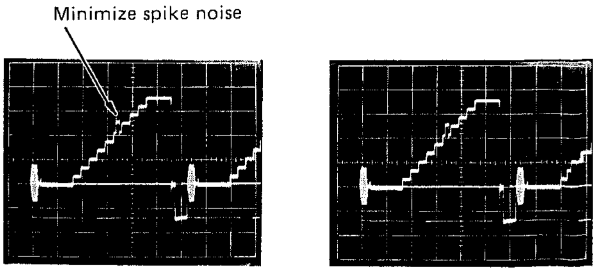
Test point :	TP7	Effect, Mix Board
Adjust :	VR17 (BORDER WIPE DC BIAS)	Effect, Mix Board

- Connect digital voltmeter (DVM) to TP7 on Effect, Mix board.
- Adjust VR17 (BORDER WIPE DC BIAS) for +5.5V.

(35) Border wipe spike comp. adjustment

Test point :	Program Output	Rear Panel
Adjust :	VR18 (BORDER EDGE SPIKE COMP.)	Effect, Mix Board
Observe :	Waveform monitor	

- Supply stairstep video signal to Video Input connector 1 through GEN-LOCK connector from the video signal generator.
- Connect the oscilloscope with 75 ohms termination to Program Output connector or observe waveform monitor.
- Trigger the oscilloscope at H. rate (Use HD output connector on rear panel).
- Select No. 1 switches on the Video Input A selector and the Video Input B selector.
- Select the WIPE switch on the WIPE/KEY control.
- Select the BORDER WIPE switch on the Wipe Mode Selector.
- Select the wipe pattern of ◨ on the Wipe Pattern Selector.
- Set the Border Wipe Width Control to fully clockwise.
- Set the WIPE lever to the middle position and MIX lever to the top position.
- Set the Color ON/OFF switch on the MAT/BORDER control to OFF position.
- Turn the luminance (LUM) on the MAT/BORDER control to middle position.
- Adjust VR18 (BORDER EDGE SPIKE COMP.) so that the spike noise at border wipe edge becomes minimum. (Fig. 3-2-33)



NO GOOD GOOD

Fig. 3-2-33

(36) Effect video level adjustment

Test point :	TP5	Effect, Mix Board
Adjust :	VR16 (EFFECT GAIN-2)	Effect, Mix Board

- Supply stairstep video signal to Video Input connector 1 through GEN-LOCK connector from video signal generator.

- Select No. 1 switch on the Video Input A selector.
- Set the Wipe lever and Mix lever to top position.
- Select WIPE switch on the Wipe/Key Control.
- Connect oscilloscope to TP5 on Effect, Mix Board.
- Trigger the oscilloscope at H.rate (Use HD output connector on rear panel).
- Adjust VR16 (EFFECT GAIN-2) so that the stairstep signal is 0.7Vp-p. (Fig. 3-2-34)

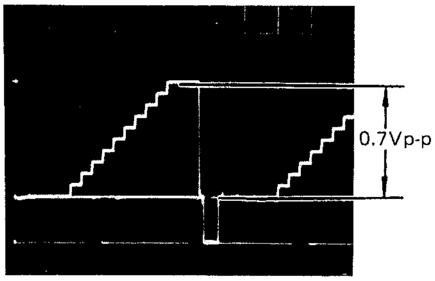


Fig. 3-2-34

(37) Effect DG/DP adjustment

Test point :	Program Output	Rear Panel
Adjusts :	VR15 (EFFECT DG/DP-2)	Effect, Mix Board
	VR23 (EFFECT DG/DP-1)	Effect, Mix Board
Observe :	Vectorscope	

- Supply the modulated stairstep video signal to the Video Input connector 1 through GEN-LOCK connector from the video signal generator.
- Connect the vectorscope to Program Output connector.
- Select No. 1 switches on the Video Input A selector and the Video Input B selector.
- Select EFF switch on the Preview/Program selector.
- Set the CUT ON/OFF switch to ON position.
- Adjust VR23 (EFFECT DG, DP-1) and VR15 (EFFECT DG/DP-2) alternetely so that the DG/DP becomes minimum on vectorscope.

(38) Mix DC bias adjustment

Test points :	TP4	Effect, Mix Board
	TP3	Effect, Mix Board
Adjusts :	VR11 (MIX DC BIAS-1)	Effect, Mix Board
	VR12 (MIX DC BIAS-2)	Effect, Mix Board

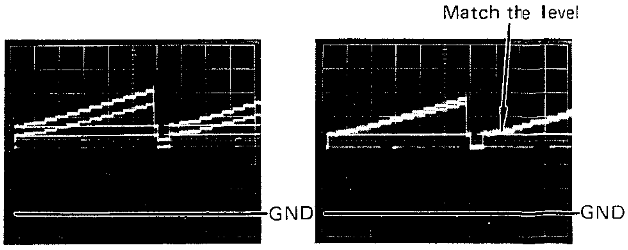
- Connect digital voltmeter (DVM) to TP4 on the Effect, Mix board.
- Adjust VR11 (MIX DC BIAS-1) for +4.5V.
- Connect digital voltmeter (DVM) to TP3 on the Effect, Mix board.
- Adjust VR12 (MIX DC BIAS-2) for +3.2V.

(39) Mix pedestal adjustment

Test points :	TP5	Effect, Mix Board
	TP10	Effect, Mix Board
Adjust :	VR14 (EFFECT SETUP)	Effect, Mix Board

Supply stairstep video signal to Video Input connector 1 through GEN-LOCK connector from video signal generator.

- Select No. 1 switches on the Video Input A, Input B and the Input C selector.
- Connect oscilloscope to TP5 and TP10 on Effect, Mix board.
- Trigger the oscilloscope at H.rate (Use HD output connector on rear panel).
- Set the input coupling selector on the oscilloscope to DC position.
- Adjust VR14 (EFFECT SETUP) so that both pedestal levels of video signal become equal. (Fig. 3-2-35)



NO GOOD GOOD

Fig. 3-2-35

(40) Mix gain adjustment

Test point :	TP9	Effect, Mix Board
Adjusts :	VR30 (CH-C GAIN)	Effect, Mix Board
	VR13 (EFFECT GAIN-3)	Effect, Mix Board

- Supply stairstep video signal to Video Input connector 1 through GEN-LOCK connector from video signal generator.
- Select No. 1 switches on the Video Input A selector, Video Input B selector and Video Input C selector.
- Connect oscilloscope to TP9 on the Effect, Mix board.

- Trigger the oscilloscope at H.rate (Use HD output connector on rear panel).
- Set Mix lever to bottom position.
- Adjust VR30 (CH-C GAIN) so that the level of waveform is 0.7Vp-p. (Fig. 3-2-36)
- Set Mix lever to top position.
- Adjust VR13 (EFFECT GAIN-3) so that the level of waveform is 0.7Vp-p. (Fig. 3-2-36)

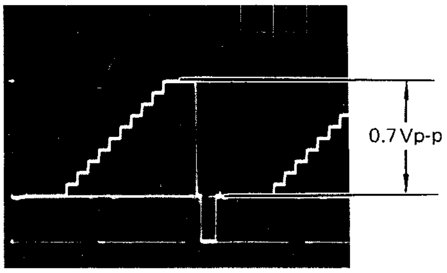


Fig. 3-2-36

(41) Mix balance adjustment

Test point :	TP9	Effect, Mix Board
Adjusts :	VR1 (CH-C MIX BALANCE-1)	Position-1 Board
	VR2 (CH-C MIX BALANCE-2)	Position-1 Board
	VR3 (EFFECT MIX BALANCE-1)	Position-2 Board
	VR4 (EFFECT MIX BALANCE-2)	Position-2 Board

- Supply stairstep video signal to Video Input connector 1 through GEN-LOCK connector from video signal generator.
- Select No. 1 switches on the Video Input A selector, Video Input B selector and Video Input C selector.
- Connect oscilloscope to TP9 on Effect, Mix board.
- Trigger the oscilloscope at H.rate (Use HD output connector on rear panel).
- Adjust VR1 (CH-C MIX BALANCE-1) and VR2 (CH-C MIX BALANCE-2) so that the waveform does not change when Mix lever is moved from upper position to bottom position.
- Adjust VR3 (EFFECT MIX BALANCE-1) and VR4 (EFFECT MIX BALANCE-2) so that the waveform does not change when Mix lever is moved from bottom position to upper position. (Fig. 3-2-37)

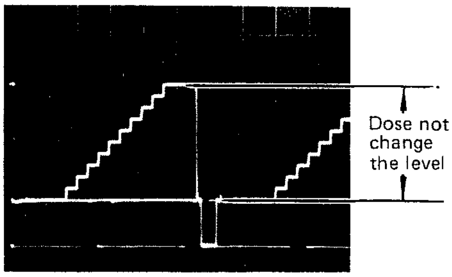


Fig. 3-2-37

(42) Mix DG/DP adjustment

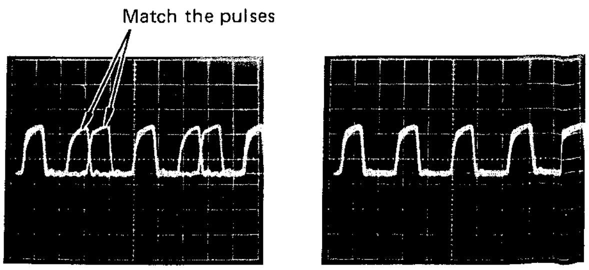
Test point :	Program Output	Rear Panel
Adjust :	VR21 (MIX DG/DP)	Effect, Mix Board
Observe :	Vectorscope	

- Supply modulated stairstep video signal to Video Input connector 1 through GEN-LOCK connector from video signal generator.
- Connect the vectorscope to the Program Output connector.
- Select No.1 switch on the Video Input C selector.
- Set the Mix lever to bottom position.
- Adjust VR21 (MIX DG/DP) so that the DG/DP becomes minimum on the vectorscope.

(43) Mat, border SC duty adjustment

Test point :	TP1	Effect, Mix board
Adjust :	VR24 (SC DUTY)	Effect, Mix board

- Set the Color ON/OFF switch to ON position on the MAT/BORDER Control.
- Connect the oscilloscope to TP1 on the Effect, Mix board.
- Trigger the oscilloscope at Internal.
- Adjust VR24 (SC DUTY) so that the two pulses match. (Fig. 3-2-38)



NO GOOD GOOD

Fig. 3-2-38

(44) Mat, border hue preset adjustment

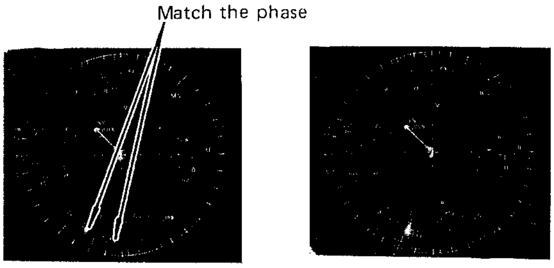
Adjusts :	CT1 (HUE PRESET-1)	Effect, Mix board
	CT2 (HUE PRESET -2)	Effect, Mix board
Observe :	Vectorscope	

- Connect the terminated vectorscope to Program Output connector.
- Select the No. 2 switch on the Video Input A and Video Input B selector. (Non video signal is supplied on No. 2)
- Set the Color ON/OFF switch to ON position on the Mat, Border Control.
- SET the saturation (SAT) control to fully clockwise on the Mat, Border Control.
- Select the WIPE switch on the Wipe/Key Control.
- Set the Wipe lever to middle position.
- Select the BORDER WIPE switch on the Wipe Mode Selector.
- Turn the Border Wipe Width Control to fully clockwise.
- Select the ⊞ switch on the Wipe Pattern Selector.
- Pay attention to moving vector on the vectorscope, when turns the HUE control on the Mat/Border Control to clockwise.
- Note the position of vector, when HUE control at fully counterclockwise.
- Adjust CT2 (HUE PRESET-2) so that the phase of vector is changed 380°, when HUE control turns to fully clockwise from fully counterclockwise.
- Repeat adjusting until phase of vector is changed 380° when turns HUE control to fully clockwise from fully counterclockwise.
- Pay attention to the moving vector on the vectorscope, when turns the HUE control on the Mat/Border Control to counterclockwise.
- Note the position of vector, when HUE control at fully clockwise.
- Adjust CT1 (HUE PRESET-1) so that the phase of vector is changed 380°, when HUE control turns to fully counterclockwise from fully clockwise.
- Repeat adjusting until phase of vector is changed 380°, when turns the HUE control to fully counterclockwise from fully clockwise.

(45) Mat, border chroma phase adjustment

Adjust :	VR6 (SC PHASE)	Effect, Mix Board
Observe :	Vectorscope	

- Connect the terminated vectorscope to Program Output Connector.
- Select the No. 2 switch on the Video Input A and Video Input B selector (Non video signal is supplied on No. 2).
- Select the EFF switch on the Video Input Preview/ Program selector.
- Set the CUT ON/OFF switch to ON position.
- Select the WIPE switch on the Wipe/Key Control.
- Set the Wipe lever to middle position.
- Select the BORDER WIPE switch on the Wipe Mode Selector.
- Turn the Border Wipe Width Control to fully clockwise.
- Select the ⊞ switch on the Wipe Pattern Selector.
- Set the switch to NTSC mode on the vectorscope.
- Set the HUE control to center position on the Mat/ Border Control.
- Set the Color ON/OFF switch to ON position on the Mat, Border Control.
- Set the saturation (SAT) control to fully clockwise on the Mat, Border Control.
- Adjust VR6 (SC PHASE) so that the two vectors becomes one above another on the vectorscope. (Fig.3-2-39)



NO GOOD GOOD

Fig. 3-2-39

(46) Border wipe width H. V. balance adjustment

Test point :	Program Output	Rear Panel
Adjust :	VR1 (V.SAW/PARA BORDER WIDTH)	Wipe Process Board
	*VR2 (V.TRIANGLE BORDER WIDTH)	Wipe Process Board
	VR3 (H.SAW/PARA BORDER WIDTH)	Wipe Process Board
	VR4 (H.TRIANGLE BORDER WIDTH)	Wipe Process Board
Observe :	Color (or B/W) video monitor	

- Supply convergence video signal to Video Input connector 1 through GEN-LOCK connector from video signal generator.
- Connect the waveform monitor to Program Output connector.
- Selects No. 1 switch on the Video Input A Selector and No. 8 switch on the Video Input B Selector.
- Select the WIPE switch on the WIPE/KEY control.
- Select the BORDER WIPE switch on the Wipe Mode Selector.
- Turn Border Wipe Width Control to fully clockwise.
- * Turn VR2 (V. TRIANGLE BORDER WIDTH) to fully clockwise.
- Adjust VR1 (V. SAW/PARA BORDER WIDTH) so that the border width becomes same, when changed wipe pattern ⬓ and ⊟ .
- Select wipe pattern of ⊞ on Wipe Pattern Selector.
- Adjust VR4 (H.TRIANGLE BORDER WIDTH) so that the H. and V. border signal width becomes the same (A=B). (Fig. 3-2-40)
- Select wipe pattern of ◳ on Wipe Pattern Selector.
- Adjust VR3 (H.SAW/PARA BORDER WIDTH) so that the H. and V. border signal width becomes the same (C=D). (Fig. 3-2-41)

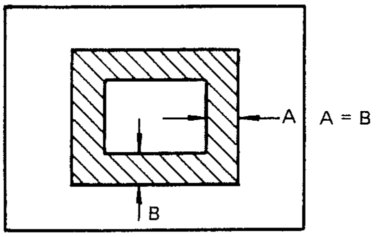


Fig. 3-2-40

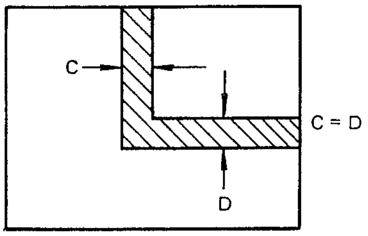


Fig. 3-2-41

*** Asterisk marked of adjustments are subjected to delete in future production.**

(47) BL killer DC bias adjustment

Test point :	Emitter of Q13	Effect, Mix Board
Adjust :	VR9	Effect, Mix Board
	(BL KILLER DC BIAS)	

- Connect digital voltmeter to emitter of Q13 on the Effect, Mix board.
- Adjust VR9 (BL KILLER DC BIAS) so that the DC level at emitter of Q13 becomes +5.5V.

(48) Matt/Border luminance setup adjustment

Test point :	Program Output	Rear Panel
Adjust :	VR5	Effect, Mix Board
	(LUMINANCE SETUP)	
Observe :	Waveform monitor	

- Connect oscilloscope with 75 ohms termination to Program Output connector or observe waveform monitor.
- Trigger the oscilloscope at H.rate (Use HD output connector on rear panel).
- Select the MAT KEY switch on WIPE/KEY Control.
- Set color ON/OFF switch to OFF position and turn Luminance (LUM) control to fully counterclockwise and set KEY switch to POS position and set LEVEL control to fully counterclockwise on MAT/BORDER Control.
- Adjust VR5 (LUMINANCE SETUP) so that the MAT setup level becomes 0V. (Fig. 3-2-42)

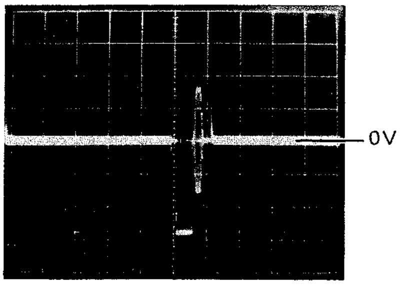


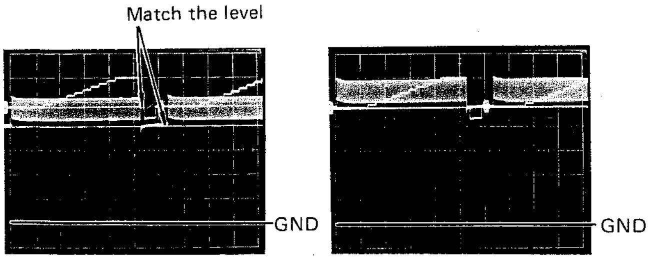
Fig. 3-2-42

(49) Border setup adjustment

Test points :	TP6	Effect, Mix Board
	TP8	Effect, Mix Board
Adjust :	VR20	Effect, Mix Board
	(BORDER SETUP)	

- Supply stairstep video signal to Video Input connector 1 through GEN-LOCK connector from video signal generator.

- Select No. 1 switches on the Video Input A selector and the Video Input B selector.
- Set the saturation (SAT) and luminance (LUM) control to fully clockwise and Color ON/OFF switch to ON position on MAT/BORDER Control.
- Connect the oscilloscope to TP6 and TP8 on Effect, Mix board.
- Trigger the oscilloscope at H.rate (Use HD output connector on rear panel).
- Set the oscilloscope input coupling selector to DC position.
- Adjust VR20 (BORDER SETUP) so that the both DC level of blanking become equal. (Fig. 3-2-43)



NO GOOD GOOD

Fig. 3-2-43

(50) Matt/Border gain and chroma phase adjustment

Test point :	Program Output	Rear Panel
Adjust :	VR8	Effect, Mix Board
	(BORDER GAIN-2)	
	VR10	Effect, Mix Board
	(MAT CHROMA PHASE)	
	VR19	Effect, Mix Board
	(BORDER GAIN-1)	
Observe :	Waveform monitor, Vectorscope	

- Supply stairstep video signal to Video Input connector 1 through GEN-LOCK connector from video signal generator.
- Select No. 1 switches on the Video Input A and Input B Selector.
- Select the WIPE KEY switch on WIPE/KEY Control.
- Select the BORDER WIPE switch on Wipe Mode Selector.
- Set Color ON/OFF switch on MAT/BORDER Control to ON position.
- Select wipe pattern of ◨ on Wipe Pattern Selector.
- Set the Wipe lever to middle position.
- Turn the Border Wipe Width Control (WIDTH) to fully clockwise.
- Turn the LEVEL control to fully counterclockwise, and luminance (LUM) control to center position, and saturation (SAT) control to fully clockwise, and HUE control to center position on the MAT, BORDER control.
- Connect the vectorscope to the Program Output connector.
- Set the switch to NTSC mode on the vectorscope.
- Adjust VR10 (MAT CHROMA PHASE) so that the two vector become 180° difference on vectorscope. (Fig. 3-2-44)
- Set COLOR ON/OFF switch on MAT/BORDER Control to OFF position.
- Turn luminance (LUM) control to fully counterclockwise.
- Connect oscilloscope with 75 ohms termination to Program Output connector or observe waveform monitor.
- Trigger the oscilloscope at H.rate (Use HD output connector on rear panel).
- Adjust VR19 (BORDER GAIN-1) so that the border signal becomes 0V. (Fig. 3-2-45)
- Turn luminance (LUM) control to center position.
- Adjust VR8 (BORDER GAIN-2) so that the border signal becomes equal to mat signal level. (Fig. 3-2-46)

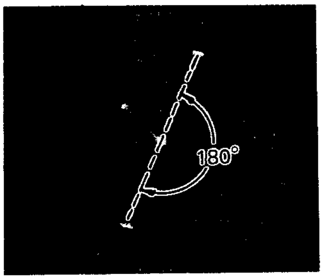
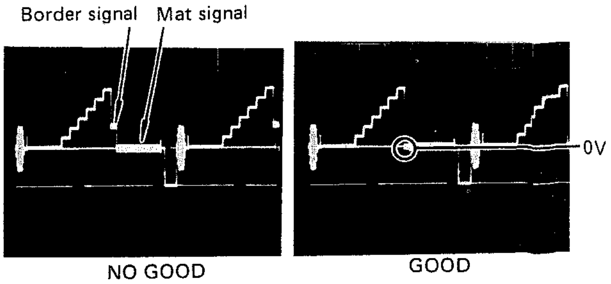
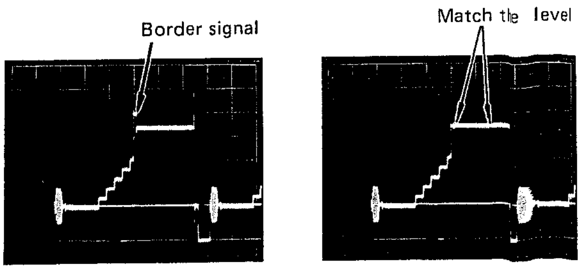


Fig. 3-2-44



NO GOOD GOOD

Fig. 3-2-45



NO GOOD GOOD

Fig. 3-2-46

(51) Matt/Border color DG, DP setting

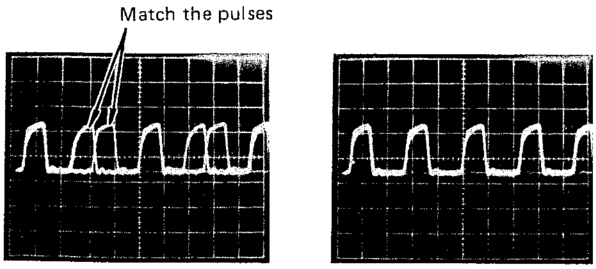
Adjust :	VR7 (MAT/BORDER DG, DP)	Effect, Mix Board

- Set VR7 (MAT/BORDER DG, DP) to mechanical center.

(52) DSK, BGD SC duty adjustment

Test point :	TP1	DSK, BGD Board
Adjust :	VR6 (SC DUTY)	DSK, BGD Board

- Set the Color ON/OFF switch to ON position on the DSK/BGD Control.
- Connect the oscilloscope to TP1 on the DSK, BGD board.
- Trigger the oscilloscope at Internal.
- Adjust VR6 (SC DUTY) so that the two pulses match. (Fig. 3-2-47)



NO GOOD GOOD

Fig. 3-2-47

(53) DSK, BGD hue preset adjustment

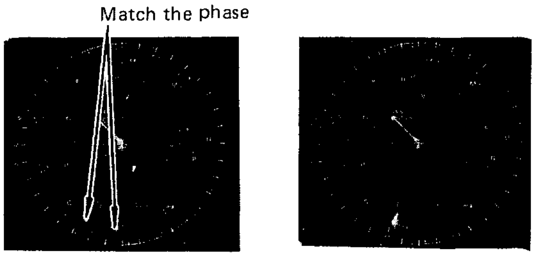
Adjusts :	CT1 (HUE PRESET-1)	DSK, BGD Board
	CT2 (HUE PRESET-2)	DSK, BGD Board
Observe :	Vectorscope	

- Connect the terminated vectorscope to Program Output connector.
- Set the C/8, BGD Selector switch to BGD position.
- Select the No. 8 (BGD) switch on the Video Input Preview/Program Selector.
- Set the CUT ON/OFF switch to ON position.
- Set the Color ON/OFF switch to ON position on the DSK/BGD Control.
- Set the saturation (SAT) control to fully clockwise on the DSK/BGD Control.
- Pay attention to moving vector on the vectorscope, when turns the HUE control on the DSK, BGD Control to clockwise.
- Note the position of vector, when HUE control at fully counterclockwise.
- Adjust CT2 (HUE PRESET-2) so that the phase of vector is changed 380°, when HUE control turns to fully clockwise from fully counterclockwise.
- Repeat adjusting until phase of vector is change 380°, when turns HUE control to fully clockwise from fully counterclockwise.
- Pay attention to the moving vector on the vectorscope, when turns the HUE control on the DSK, BGD Control to counterclockwise.
- Note the position of vector, when HUE control at fully clockwise.
- Adjust CT1 (HUE PRESET-1) so that the phase of vector is change 380°, when HUE control turns to fully counterclockwise from fully clockwise.
- Repeat adjusting until phase of vector is changed 380°, when turns HUE control from fully clockwise to fully counterclockwise.

(54) DSK, BGD chroma phase adjustment

Adjust :	VR15 (SC PHASE)	DSK, BGD Board
Observe :	Vectorscope	

- Connect the terminated vectorscope to Program Output connector.
- Set the C/8, BGD Selector switch to BGD position.
- Select the No. 8 (BGD) switch on the Video Input Preview/Program Selector.
- Set the CUT ON/OFF switch to ON position.
- Set the HUE control to center position on the DSK/BGD control.
- Set the saturation (SAT) control to fully clockwise on the DSK/BGD Control.
- Set the Color ON/OFF switch to ON position on the DSK/BGD Control.
- Set the switch to NTSC mode on the vectorscope.
- Adjust VR15 (SC PHASE) so that the two vectors become one above another on the vectorscope. (Fig. 3-2-48)



NO GOOD GOOD

Fig. 3-2-48

(55) BL killer DC bias adjustment

Test point :	Emitter of Q13	DSK, BGD Board
Adjust :	VR9 (BL KILLER DC BIAS)	DSK, BGD Board

- Connect digital voltmeter (DVM) to emitter of Q13 on the DSK, BGD board.
- Adjust VR9 (BL KILLER DC BIAS) for +5.5V.

(56) DSK, BGD luminance preset adjustment

Test Point :	Program Output	Rear Panel
Adjust :	VR5 (LUMINANCE PRESET)	DSK, BGD Board
Observe :	Waveform monitor	

- Set C/8, BGD Selector switch to BGD position.
- Select No. 8 (BGD) switch on the video Input A selector.
- Set the Color ON/OFF switch on DSK, BGD control to OFF position.
- Turn the luminance (LUM) to fully counterclockwise on DSK, BGD Control.
- Connect oscilloscope with 75 ohms termination to the program output connector or observe waveform monitor.
- Trigger the oscilloscope at H.rate (Use HD output connector on rear panel).
- Adjust VR5 (LUMINANCE PRESET) so that the waveform become 0V. (Fif. 3-2-49)

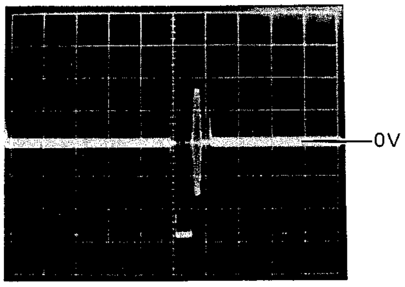


Fig. 3-2-49

(57) DSK pulse gain adjustment

Test point :	Pin 20 (a) of CN16	DSK, BGD Board
Adjust :	VR12 (DSK PULSE GAIN)	DSK, BGD Board

- Supply stairstep video signal to Video Input connector DSK through GEN-LOCK connector from video signal generator.
- Connect oscilloscope to Pin 20 (a) of CN16 on the DSK, BGD board.
- Trigger the oscilloscope at H.rate (Use HD output connector on rear panel).
- Turn the LEVEL control on the DSK, BGD Control to fully counterclockwise.
- Select WIPE switch on WIPE/KEY Control.
- Set the DSK ON/OFF switch to ON position.
- Set the oscilloscope input coupling selector to DC position.
- Adjust VR12 (DSK PULSE GAIN) so that the blanking period of DSK signal becomes 5.5V from ground level. (Fig. 3-2-50)

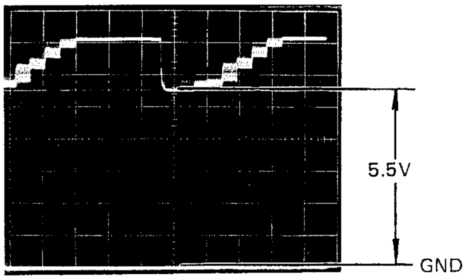


Fig. 3-2-50

(58) DSK DC bias adjustment

Test point :	TP8	Output Board
Adjust :	VR14 (DSK DC BIAS)	Output Board

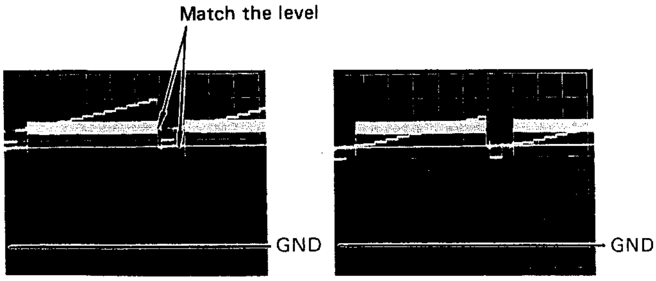
- Connect digital voltmeter (DVM) to TP8 on output board.
- Adjust VR14 (DSK DC BIAS) for +5.5V.

(59) Program/DSK setup adjustment

Test points :	TP7	Output Board
	TP9	Output Board
Adjust :	VR12 (PROGRAM SETUP-2)	Output Board

- Supply stairstep video signal to Video Input connector 1 through GEN-LOCK connector from video signal generator.
- Select No. 1 switches on the Video Input A selector and the Video Input B selector.
- Set the saturation (SAT) and luminance (LUM) control to fully clockwise on the DSK, BGD Control.
- Set the Mix lever to top position.

- Connect oscilloscope to TP7 and TP9 on the Output board.
- Trigger the oscilloscope at H.rate (Use HD output
- connector on rear panel).
- Set the oscilloscope input coupling selector to DC position.
- Adjust VR12 (PROGRAM SETUP-2) so that the blanking levels of TP7 and TP9 signal become equal. (Fig. 3-2-51)



NO GOOD GOOD

Fig. 3-2-51

(60) DSK/Program gain and spike compensation adjustment

Test point :	TP10	Output Board
Adjusts :	VR13 (PROGRAM GAIN-4)	Output Board
	VR16 (DSK/PROGRAM GAIN)	Output Board
	VR15 (DSK SPIKE COMP)	Output Board

- Supply stairstep video signal to Video Input connector DSK through GEN-LOCK connector and Input No. 1 connector from video signal generator.
- Selects No. 1 switch on the Video Input A, B and C selector.
- Set DSK ON/OFF switch to ON position.
- Set the EDGE ON/OFF switch to OFF position on DSK, BGD control.
- Connect oscilloscope to TP10 on the Output board.
- Trigger the oscilloscope at H. rate (Use HD output connector on rear panel).
- Turn the luminance (LUM) control on the DSK, Control to fully counterclockwise.
- Turn the LEVEL control on the DSK, BGD Control to fully clockwise.
- Adjust VR16 (DSK/PROGRAM GAIN) so that the DSK signal level becomes same as blanking level.
- Turn the LEVEL control on DSK, BGD Control to fully counterclockwise.
- Adjust VR13 (PROGRAM GAIN-4) so that the stair step signal becomes 0.7V from blanking level. (Fig. 3-2-52)
- Supply convergence video signal to Video Input connector DSK through GEN-LOCK connector from video signal generator.
- Turn the LEVEL control on the DSK, BGD Control to center position.
- Turn the luminance (LUM) control on the DSK, BGD Control to center position.
- Adjust VR15 (DSK SPIKE COMP.) so that the spike noise on the video signal become minimum. (Fig. 3-2-53)

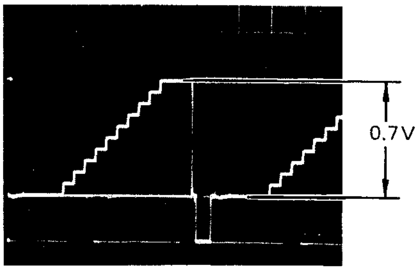
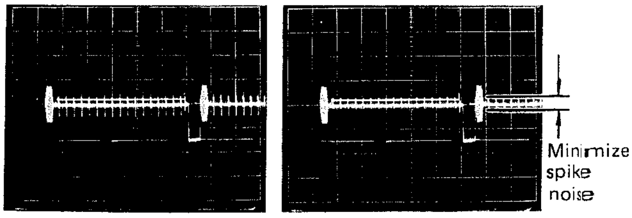


Fig. 3-2-52



NO GOOD GOOD

Fig. 3-2-53

(61) DSK, BGD DG, DP setting

Adjust :	VR7 (DSK, BGD DG.DP)	DSK, BGD Board

- Set VR7 (DSK, BGD DG.DP) to their mechanical center.

(62) DSK, BGD gain and chroma phase adjustment

Test Point :	Program Output	Rear Panel
Adjusts :	VR10 (DSK CHROMA PHASE)	DSK, BGD Board
	VR 8 (BGD GAIN)	DSK, BGD Board
Observe :	Waveform monitor, Vectorscope	

- Supply the stairstep video signal to Video Input connector DSK through GEN-LOCK connector from video signal generator.
- Connect vectorscope to Program Output connector
- Set C/8, BGD Selector switch to BGD position.
- Select No. 8 (BGD) on the Video Input A selector, Video Input B selector and Video Input C selector.
- Set the DSK ON/OFF switch to ON position.
- Set Color ON/OFF switch on the DSK, BGD Control to ON position.
- Set Edge ON/OFF switch on the DSK, BGD Control to OFF position.
- Turn LEVEL control on the DSK, BGD Control to fully counterclockwise.
- Turn luminance (LUM) control on the DSK, BGD Control to center position.
- Turn saturation (SAT) control on the DSK, BGD Control to fully clockwise.
- Adjust VR10 (DSK CHROMA PHASE) so that vector differences of DSK color and BGD color become 180°. (Fig. 3-2-54)
- Set the Color ON/OFF switch on DSK, BGD Control to OFF position.
- Connect oscilloscope with 75 ohms termination to Program Output connector or observe waveform monitor.
- Trigger the oscilloscope at H.rate (Use HD output connector on rear panel).
- Adjust VR8 (BGD GAIN) so that the BGD signal level becomes equal to DSK signal level. (Fig. 3-2-55)

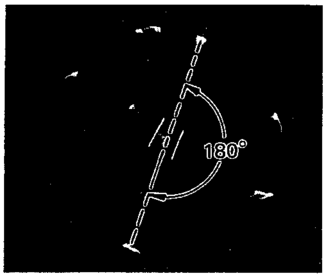
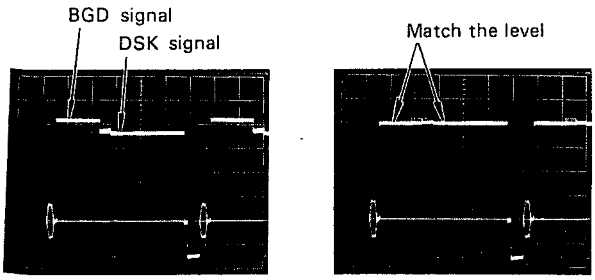


Fig. 3-2-54



NO GOOD

GOOD

Fig. 3-2-55

(63) DSK edge adjustment

Test Point :	Program Output	Rear Panel
Adjusts :	VR18 (DSK EDGE GAIN)	Output Board
	VR11 (DSK EDGE WIDTH)	DSK, BGD Board
Observe :	Waveform monitor, Underscanned Color (or B/W) video monitor	

- Supply convergence video signal to Video Input connector DSK from video signal generator.
- Connect the oscilloscope with 75 ohms termination to the Program Output connector or observe waveform monitor.
- Set the DSK ON/OFF switch to ON position.
- Set the Edge ON/OFF switch on DSK, BGD control to ON position.
- Adjust VR18 (DSK EDGE GAIN) so that edge signal becomes 0.3V undershoot from blanking level. (Fig. 3-2-56)
- Adjust VR11 (DSK EDGE WIDTH) so that the edge portion of picture becomes best on the video monitor.

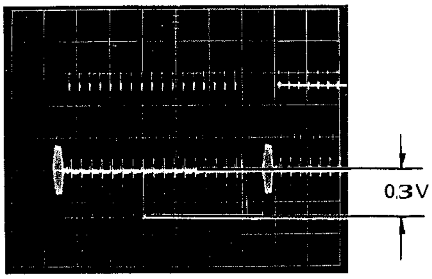


Fig. 3-2-56

(64) DSK/Program DG. DP adjustment

Test Point :	Program Output	Rear Panel
Adjust :	VR17 (DSK/PROGRAM DG.DP)	Output Board
Observe :	Vectorscope	

- Supply modulated stairstep video signal to Video Input connector 1 through GEN-LOCK connector from video signal generator.
- Connect the vectorscope to the Program Output connector.
- Select the No. 1 switch on the Video Input A selector.
- Set the DSK ON/OFF switch to ON position.
- Set the Wipe lever and Mix lever to top position.
- Adjust VR17 (DSK/PROGRAM DG. DP) so that the DG. DP becomes minimum on vectorscope.

(65) Video Input A, B and C chroma phase adjustment

Test Point :	Program Output	Rear Panel
Adjusts :	VR29 (CH-A CHROMA PHASE)	Effect, Mix Board
	VR22 (CH-C CHROMA PHASE)	Effect, Mix Board
Observe :	Vectorscope	

- Connect the vectorscope to the Program Output connector.
- Set C/7, Color Bar Selector to C/B position.
- Select No. 7 (C/B) switches on the Video Input A selector, Video Input B selector and Video Input C selectro.
- Select the WIPE switch on WIPE/KEY Control.
- Set the GEN-LOCK ON/OFF switch to OFF position.
- Set DSK ON/OFF switch to OFF position.
- Select wipe pattern of ⬓ at Wipe Pattern Selector.
- Set the Wipe lever to middle position.
- Set the Mix lever to top position.
- Adjust VR29 (CH-A CHROMA PHASE) so that the both vectors of Video Input A and Video Input B are overlaid.
- Set the Wipe lever to bottom position.
- Adjust VR22 (CH-C CHROMA PHASE) so that the vector of Video Input C and Video Input B does not changed when moved Mix lever to top and bottom.

(66) PV-PG/EFFECT Chroma phase adjustment

Test Point :	Program Output	Rear Panel
Adjusts :	VR14 (PV-PG CHROMA PHASE)	DSK, BGD Board
	VR13 (EFFECT CHROMA PHASE)	DSK, BGD Board
Observe :	Vectorscope	

- Connect the vectorscope to the Program Output connector.
- Set C/7, Color Bar Selector switch to color bar (C/B) position.
- Select No. 7 (C/B) switches on the Video Input A selector, Video Input B selector, Video Input C selector and Video Input Preview/Program selector.
- Set the GEN-LOCK ON/OFF switch to OFF position.
- Set the Wipe lever to bottom position.
- Set the Mix lever to top position.
- Adjust VR14 (PV-PG CHROMA PHASE) so that the both phase of vectors become same when CUT ON/OFF switch is switched ON and OFF alternately.
- Select EFF switch on the Preview/Program Selector.
- Adjust VR13 (EFFECT CHROMA PHASE) so that the both phase of vectors become same when CUT ON/OFF switch is switched ON and OFF alternately.

(67) Program chroma phase-1 adjustment

Test Point :	Program Output	Rear Panel
Adjust :	VR1 (PROGRAM CHROMA PHASE)	Output Board
Observe :	Vectorscope	

- Connect the vectorscope to the Program Output connector.
- Set C/7, Color Bar Selector switch to color bar (C/B) position.
- Select No. 7 (C/B) switches on the Video Input A selector, Video Input B selector and Video Input C selector.
- Turn the LEVEL control to fully clockwise on the DSK, BGD Control.
- Set the GEN-LOCK ON/OFF switch to OFF position.
- Adjust VR1 (PROGRAM CHROMA PHASE) so that the both phase of vectors become same, when DSK ON/OFF switch is switched ON and OFF alternately.

(68) Program chroma phase-2 adjustment

Test Point :	Program Output	Rear Panel
Adjust :	CT1 (PROGRAM FREQ. RESPONSE)	Output Board
	VR19 (BURST PHASE)	Output Board
Observe :	Vectorscope	

- Connect the vectorscope to the Program Output.
- Supply color bar signal to Video Input Connector 1 through GEN-LOCK connector from video signal generator.
- Select No. 1 switch on the Video Input Preview/Program selector.
- Set the GEN-LOCK ON/OF switch to ON position.
- Set the CUT ON/OFF switch to the ON position.
- Adjust CT1 (PROGRAM FREQ. RESPONSE) so that the chroma gain becomes same as input level.
- Set C/7, Color Bar Selector switch to color bar (C/B) position.
- Select No. 7 (C/B) switch on the Video Input Preview /Program selector.
- Adjust VR19 (BURST PHASE) so that the each vector falls in to its respective box ⊞ on the vectorscope. (Fig. 3-2-57)

Note :
- If all vectors dosen't falls in to its respective box, adjust step (73) to (75).
- Do not use extension board, when adjusting the (color bar phase) on Sync, C/Bar board and Output board.

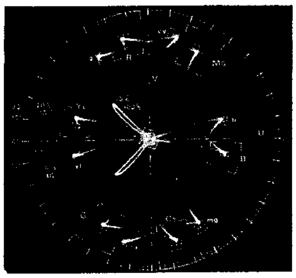


Fig. 3-2-57

(69) Preview DSK chroma phase adjustment

Test Point :	Preview Output	Rear Panel
Adjust :	VR20 (PREVIEW CHROMA PHASE)	Output Board
Observe :	Vectorscope	

- Connect the vectorscope to the Preview Output connector.
- Set C/7, Color Bar Selector switch to color bar (C/B) position.
- Set the LEVEL control to fully clockwise on the DSK, BGD Control.
- Set the GEN-LOCK ON/OFF switch to OFF position.
- Adjust VR20 (PREVIEW CHROMA PHASE) so that the both phase of vector becomes same when selected 7(C/B) switch and DSK switch on Preview/Program Selector alternately.

(70) Program/Preview chroma phase adjustment

Test Point :	Preview Output	Rear Panel
Adjusts :	CT2 (PREVIEW FREQ. RESPONSE)	Output Board
Observe :	Vectorscope	

- Connect the vectorscope to the Preview Output connector.
- Set C/7, Color Bar Selector to color bar (C/B) position.
- Select No. 7 (C/B) switches on the Video Input Preview/Program selector.
- Set the GEN-LOCK ON/OFF switch to OFF position.
- Set CUT ON/OFF switch to the OFF position.
- Adjust CT2 (PREVIEW FREQ. RESPONSE) so that each vector falls into its respective box ⊞ on vectorscope. (Fig. 3-2-57)

(71) White clip adjustment

Test points :	Program Output	Rear Panel
	Preview Output	Rear Panel
Adjusts :	VR8 (WHITE CLIP-1)	Output Board
	VR27 (WHITE CLIP-2)	Output Board
Observe :	Waveform monitor	

- Connect the oscilloscope with 75 ohms termination to the Program Output connector or observe waveform monitor.
  Set C/7, Color Bar Selector switch to color bar (C/B) position.
- Select No. 7 (C/B) switches on the Video Input A selector, Video Input B selector and Video Input C selector.
- Select EFF switch on the Video Input Preview/Program selector.
- Set the Mix lever separate and left side lever (EFF Mix lever) to top position, right side lever (INPUT C Mix lever) to bottom position.
- Adjust VR8 (WHITE CLIP-1) so that blanking level to luminance video clip level becomes 0.9V. (Fig. 3-2-58)
- Connect the oscilloscope with 75 ohms termination to the Preview Output connector or observe waveform monitor.
- Adjust VR27 (WHITE CLIP-2) so that blanking level to luminance video clip level becomes 0.9V. (Fig. 3-2-58)

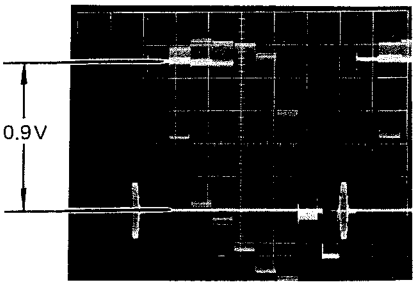


Fig. 3-2-58

(72) Color bar width adjustment

Test points :	TP5	Sync,C/Bar Board
	Pin 2a of CN27	Sync,C/Bar Board
Adjust :	VR1 (BAR WIDTH)	Sync,C/Bar Board

- Set C/7, Color Bar Selector switch to color bar (C/B) position.

- Select No. 7 (C/B) switch on the Video Input A Selector.
- Set the WIPE lever and MIX lever to top position.
- Make short contact between TP3 and TP4 on the Sync, C/Bar baord.
- Connect oscilloscope to TP5 and pin 2a of CN27 (BL. A) on the Sync, C/Bar board.
- Trigger the oscilloscope at H.rate (Use HD output connector on rear panel).
- Adjust VR1 (BAR WIDTH) so that the black bar width is 6.0μsec. (Fig. 3-2-59)

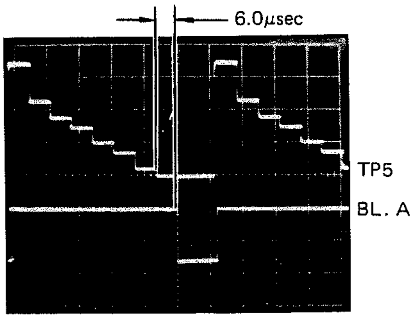


Fig. 3-2-59

(73) Color bar white balance, carrier balance adjustment

Test point :	Program Output	Rear Panel
Adjusts :	VR4 (B-Y WHITE BALANCE)	Sync,C/Bar Board
	VR6 (R-Y WHITE BALANCE)	Sync,C/Bar Board
	VR9 (R-Y CARRIER BALANCE)	Sync,C/Bar Board
	VR10 (B-Y CARRIER BALANCE)	Sync,C/Bar Board
Observe :	Waveform monitor	

- Set the C/7, Color Bar Selector switch to color bar (C/B) position.
- Select No. 7 (C/B) switch on the Video Input A Selector.
- Set the WIPE lever and MIX lever to top position.
- Connect oscilloscope with 75 ohms termination to Program Output connector or observe waveform monitor..
- Trigger the oscilloscope at H.rate (Use HD output connector on rear panel).
- Adjust VR9 (R-Y CARRIER BALANCE) and VR10 (B-Y CARRIER BALANCE) so that the carrier on the black portion of the color bar signal is minimum.
- Adjust VR4 (B-Y WHITE BALANCE) and VR6 (R-Y WHITE BALANCE) so that the carrier on the white portion of the color bar signal is minimum.
- Repeat this procedure until both carrier is minimum. (Fig. 3-2-60)

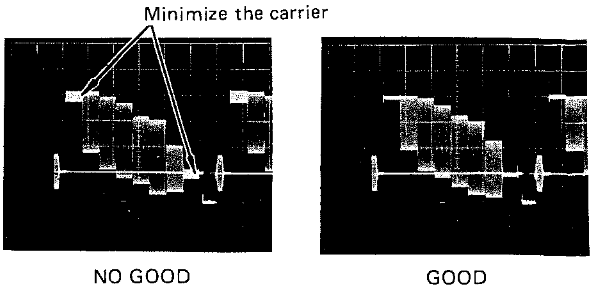


Fig. 3-2-60

(74) Color bar luminance gain adjustment

Test point :	Program Output	Rear Panel
Adjusts :	VR2 (Y GAIN)	Sync, C/Bar Board
	VR3 (WHITE GAIN)	Sync, C/Bar Board
Observe :	Waveform monitor	

- Set the C/7, Color bar selector switch to color bar (C/B) position.
- Select the No. 7 (C/B) switch on the Video Input Preview/Program selector.
- Set the CUT ON/OFF switch to ON position.
- Connect the oscilloscope with 75 ohms termination to Program Output connector on rear panel or observe waveform monitor and select the switch to luminance position on the waveform monitor.
- Make short contact between TP3 and TP4 on the Sync, C/bar board.
- Adjust VR2 (Y GAIN) so that the luminance level of yellow becomes 0.465Vp-p. (Fig. 3-2-61)
- Adjust VR3 (WHITE GAIN) so that the video level of white portion becomes 0.7Vp-p. (Fig. 3-2-61)
- Repeat this procedure until both levels becomes correct levels.

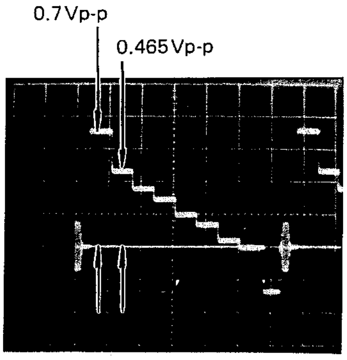


Fig. 3-2-61

(75) Color bar chroma adjustment

Adjusts :	VR5 (B–Y GAIN)	Sync, C/Bar Board
	VR7 (R–Y GAIN)	Sync, C/Bar Board
	VR8 (SC QUAD)	Sync, C/Bar Board
Observe :	Vectorscope	

- Connect the vectorscope to the Program Output connector on rear panel.
- Set the gain of vectorscope to 75% mode.
- Set the C/7, Color Bar (C/B) Selector switch to color bar (C/B) position.
- Select No. 7 (C/B) switch on the Video Input Preview/Program Selector.
- Set the CUT ON/OFF switch to ON position.
- Adjust VR5 (B-Y GAIN), VR7 (R-Y GAIN) and VR8 (SC QUAD) so that the all vectors fall into their respective boxes ⊞ on the vectorscope. (Fig. 3-2-62)
- If not all vectors fall into their respective boxes ⊞, readjust VR19 (BURST PHASE) on the Output board and readjusting the step (68) and (70).

  Note : Do not use extension board, when adjusting the this step.

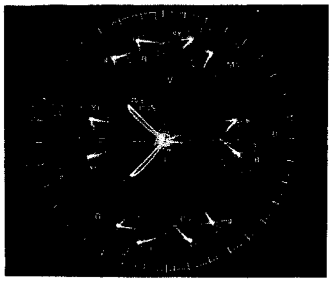


Fig. 3-2-62

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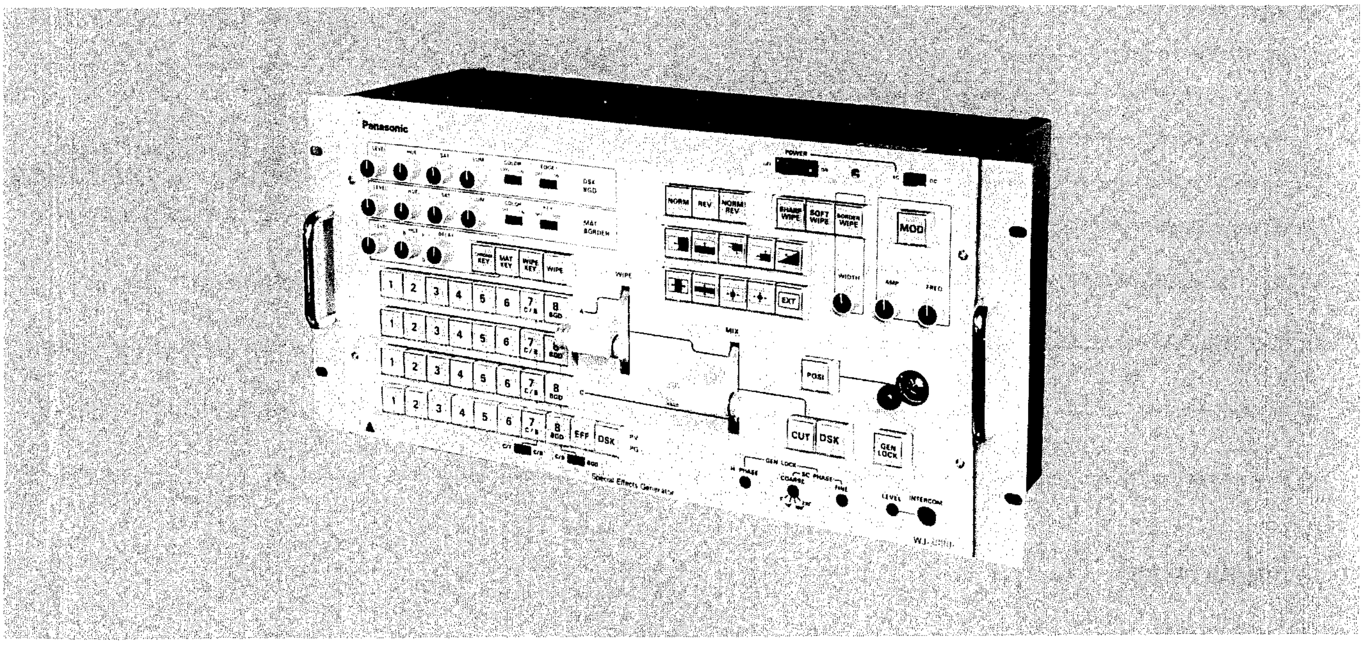
Service Manual

Location of Test Points and Adjusting Controls

Special Effects Generator
WJ-5600


Panasonic
NORM
REV
NORM/REV
SHARP WIPE
SOFT WIPE
BORDER WIPE
MOD
EXT
POSI
CUT
DSK
GEN LOCK
EFF
Special Effects Generator

CONTENTS

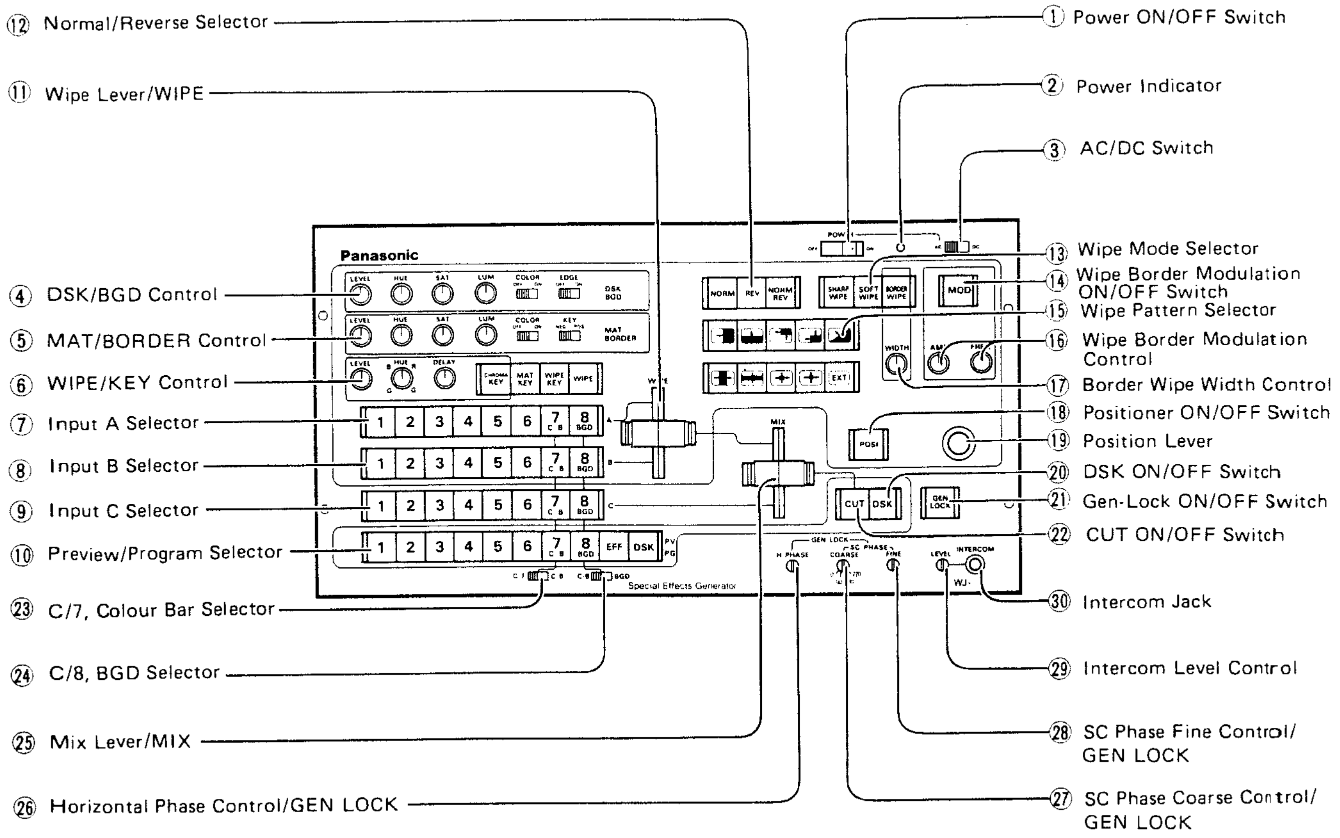
MAJOR OPERATING CONTROLS 1
OUTPUT BOARD and DSK, BGD BOARD 2
EFFECT, MIX BOARD and WIPE PROCESS BOARD 3
WAVEFORM GEN. BOARD and MODURATION BOARD 4
SYNC, C/BAR BOARD and MOTHER BOARD 5
POSITION-1 and POSITION-2 BOARD 6

Panasonic

Matsushita Electric Trading Co., Ltd.
P.O. Box 288, Central Osaka Japan

MAJOR OPERATING CONTROLS

• FRONT VIEW


⑫ Normal/Reverse Selector
⑪ Wipe Lever/WIPE
④ DSK/BGD Control
⑤ MAT/BORDER Control
⑥ WIPE/KEY Control
⑦ Input A Selector
⑧ Input B Selector
⑨ Input C Selector
⑩ Preview/Program Selector
㉓ C/7, Colour Bar Selector
㉔ C/8, BGD Selector
㉕ Mix Lever/MIX
㉖ Horizontal Phase Control/GEN LOCK
① Power ON/OFF Switch
② Power Indicator
③ AC/DC Switch
⑬ Wipe Mode Selector
⑭ Wipe Border Modulation ON/OFF Switch
⑮ Wipe Pattern Selector
⑯ Wipe Border Modulation Control
⑰ Border Wipe Width Control
⑱ Positioner ON/OFF Switch
⑲ Position Lever
⑳ DSK ON/OFF Switch
㉑ Gen-Lock ON/OFF Switch
㉒ CUT ON/OFF Switch
㉚ Intercom Jack
㉙ Intercom Level Control
㉘ SC Phase Fine Control/ GEN LOCK
㉗ SC Phase Coarse Control/ GEN LOCK
Panasonic
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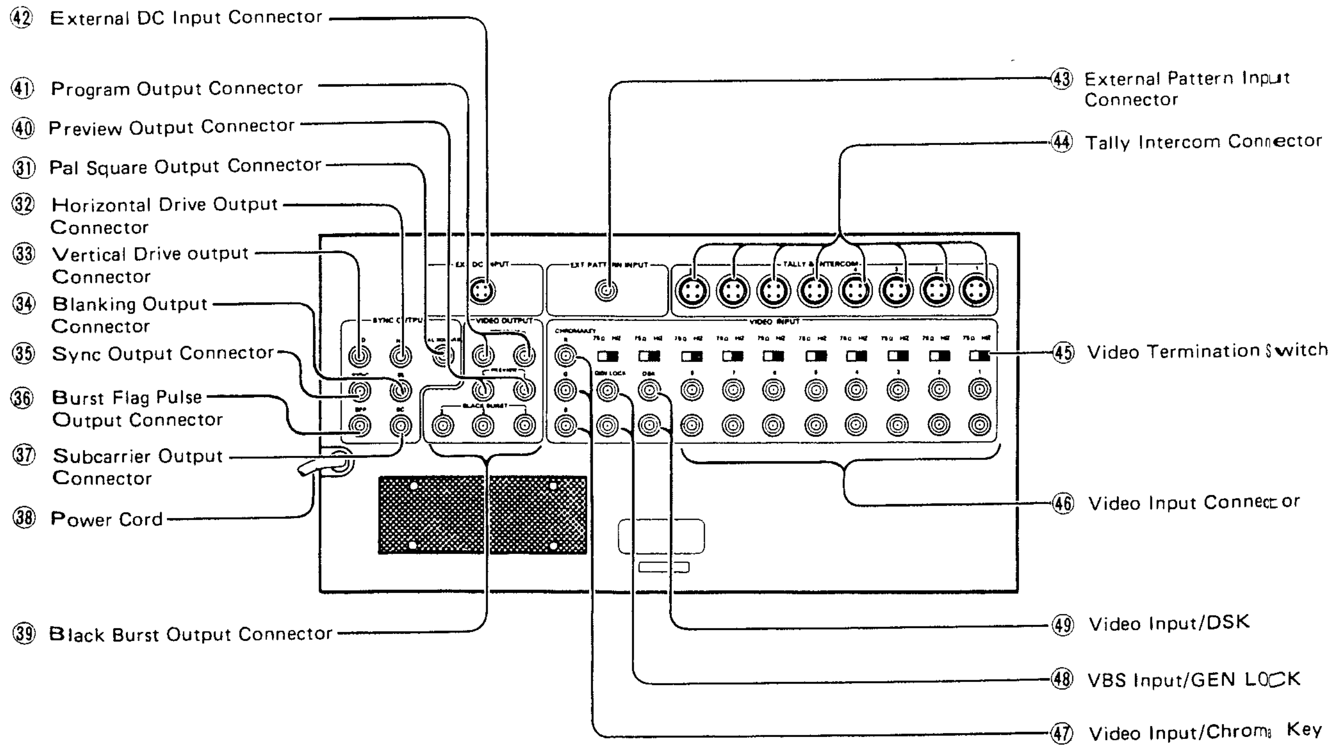
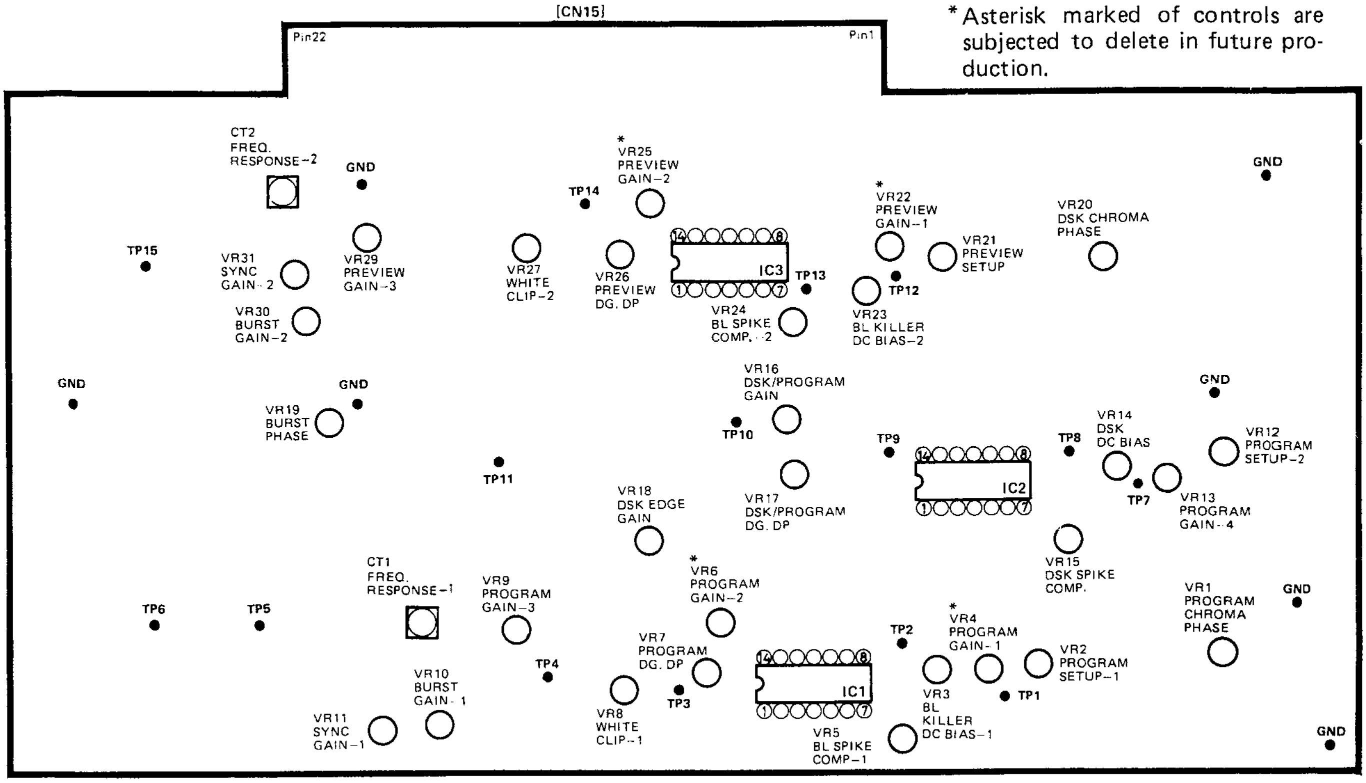
• REAR VIEW

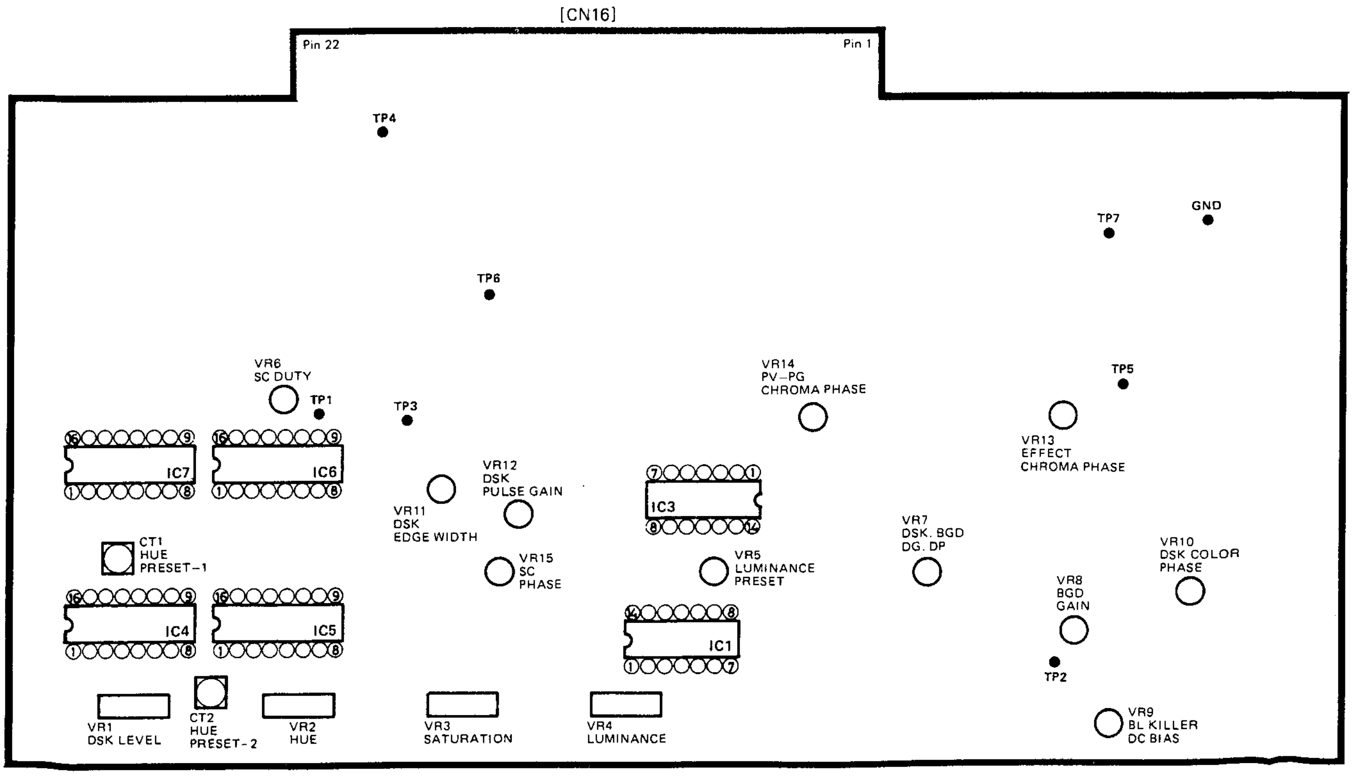

㊷ External DC Input Connector
㊶ Program Output Connector
㊵ Preview Output Connector
㉛ Pal Square Output Connector
㉜ Horizontal Drive Output Connector
㉝ Vertical Drive output Connector
㉞ Blanking Output Connector
㉟ Sync Output Connector
㊱ Burst Flag Pulse Output Connector
㊲ Subcarrier Output Connector
㊳ Power Cord
㊴ Black Burst Output Connector
㊸ External Pattern Input Connector
㊹ Tally Intercom Connector
㊺ Video Termination Switch
㊻ Video Input Connector
㊾ Video Input/DSK
㊽ VBS Input/GEN LOCK
㊼ Video Input/Chroma Key

OUTPUT BOARD — Component Side —

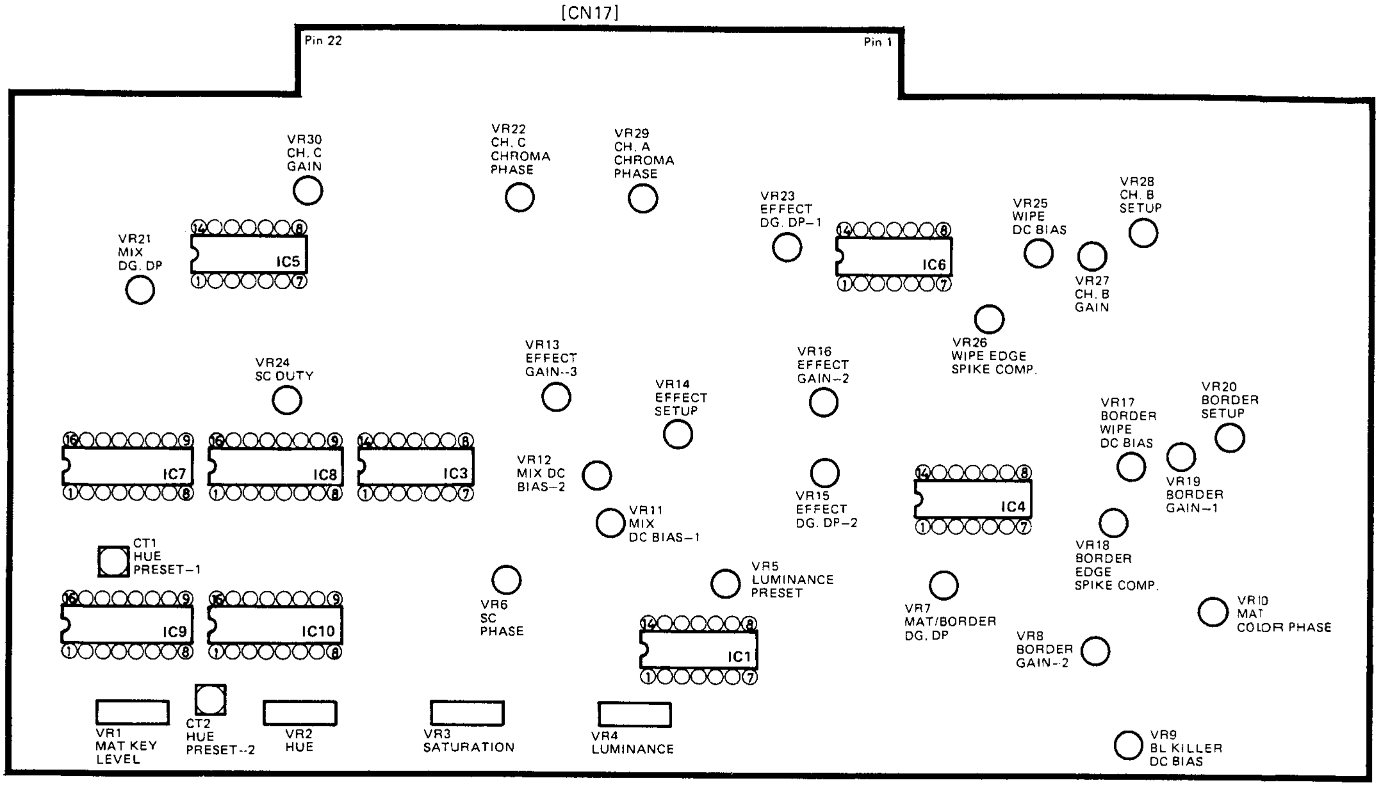
*Asterisk marked of controls are subjected to delete in future production.


[CN15]
Pin22
Pin1
CT2 FREQ. RESPONSE-2
GND
*VR25 PREVIEW GAIN-2
TP14
*VR22 PREVIEW GAIN-1
VR20 DSK CHROMA PHASE
GND
TP15
VR31 SYNC GAIN-2
VR29 PREVIEW GAIN-3
VR27 WHITE CLIP-2
VR26 PREVIEW DG. DP
IC3
TP13
VR21 PREVIEW SETUP
TP12
VR30 BURST GAIN-2
VR24 BL SPIKE COMP.-2
VR23 BL KILLER DC BIAS-2
GND
GND
VR16 DSK/PROGRAM GAIN
GND
VR19 BURST PHASE
TP10
VR14 DSK DC BIAS
TP9
TP8
VR12 PROGRAM SETUP-2
TP11
IC2
TP7
VR13 PROGRAM GAIN-4
VR18 DSK EDGE GAIN
VR17 DSK/PROGRAM DG. DP
VR15 DSK SPIKE COMP.
CT1 FREQ. RESPONSE-1
VR9 PROGRAM GAIN-3
*VR6 PROGRAM GAIN-2
VR1 PROGRAM CHROMA PHASE
GND
TP6
TP5
*VR4 PROGRAM GAIN-1
TP2
VR7 PROGRAM DG. DP
VR2 PROGRAM SETUP-1
TP4
VR10 BURST GAIN-1
IC1
TP3
VR3 BL KILLER DC BIAS-1
TP1
VR11 SYNC GAIN-1
VR8 WHITE CLIP-1
VR5 BL SPIKE COMP-1
GND

DSK, BGD BOARD — Component Side —

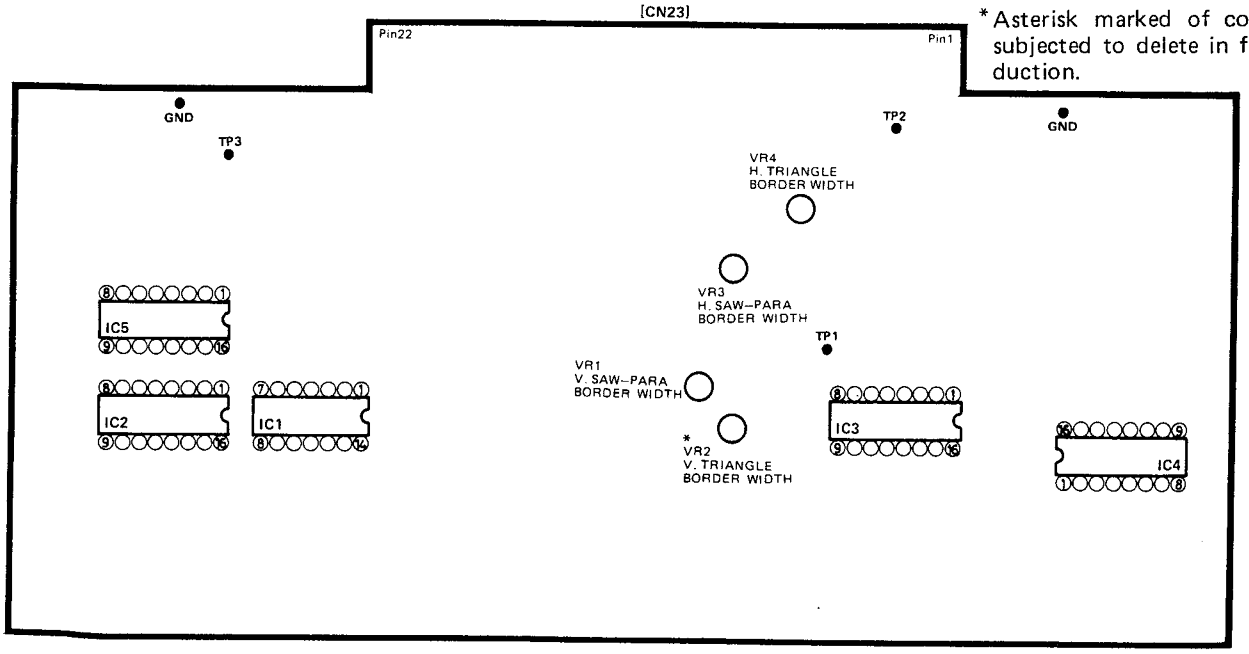

[CN16]
Pin 22
Pin 1
TP4
TP7
GND
TP6
VR6 SC DUTY
TP1
TP3
VR14 PV-PG CHROMA PHASE
TP5
IC7
IC6
VR12 DSK PULSE GAIN
VR13 EFFECT CHROMA PHASE
VR11 DSK EDGE WIDTH
IC3
VR7 DSK. BGD DG. DP
CT1 HUE PRESET-1
VR15 SC PHASE
VR5 LUMINANCE PRESET
VR10 DSK COLOR PHASE
VR8 BGD GAIN
IC4
IC5
IC1
TP2
VR1 DSK LEVEL
CT2 HUE PRESET-2
VR2 HUE
VR3 SATURATION
VR4 LUMINANCE
VR9 BL KILLER DC BIAS

EFFECT, MIX BOARD —Component Side —

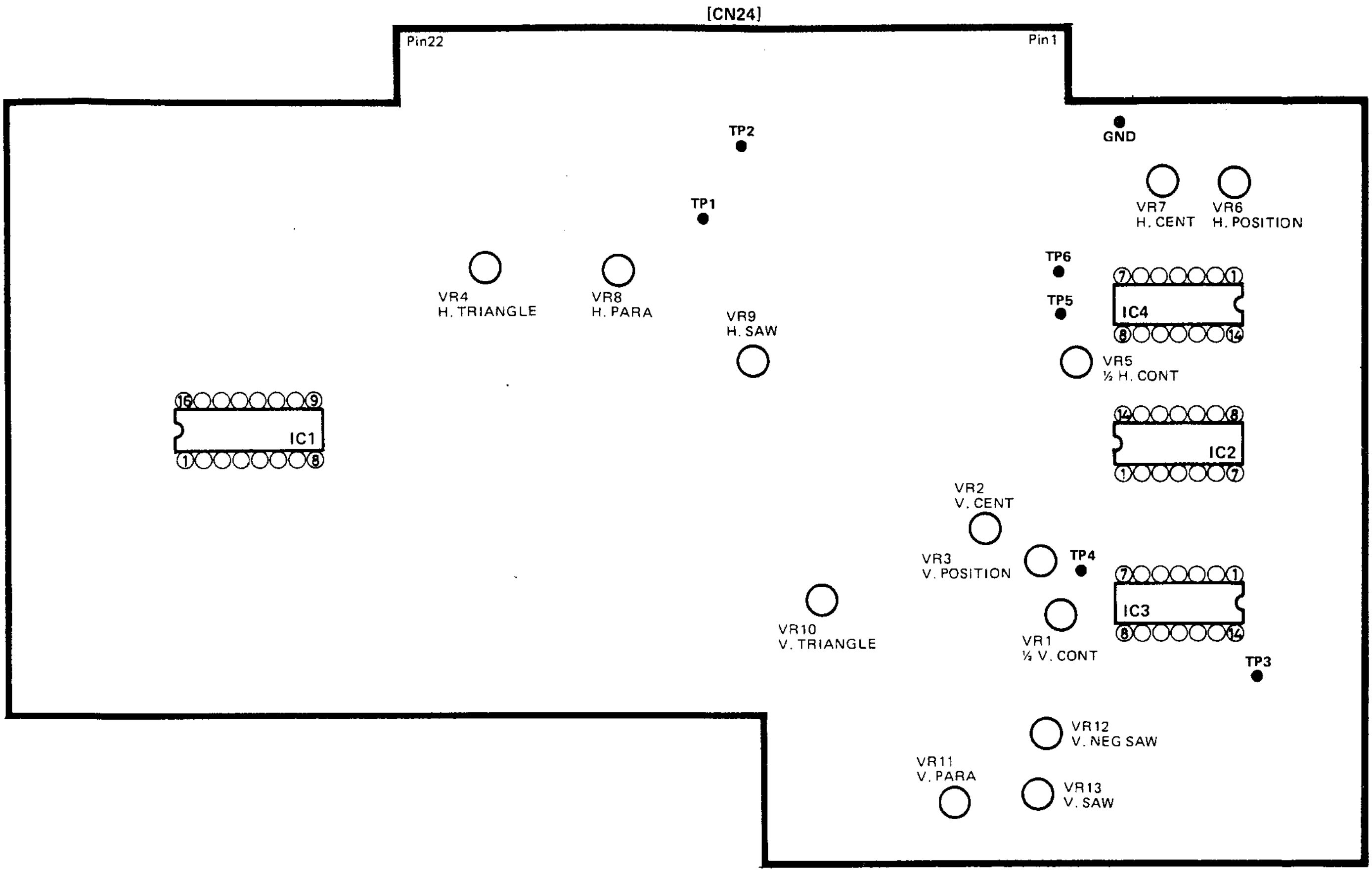

[CN17]
Pin 22
Pin 1
VR30 CH. C GAIN
VR22 CH. C CHROMA PHASE
VR29 CH. A CHROMA PHASE
VR23 EFFECT DG. DP–1
VR25 WIPE DC BIAS
VR28 CH. B SETUP
VR21 MIX DG. DP
IC5
IC6
VR27 CH. B GAIN
VR26 WIPE EDGE SPIKE COMP.
VR24 SC DUTY
VR13 EFFECT GAIN--3
VR14 EFFECT SETUP
VR16 EFFECT GAIN--2
VR17 BORDER WIPE DC BIAS
VR20 BORDER SETUP
IC7
IC8
IC3
VR12 MIX DC BIAS–2
VR11 MIX DC BIAS–1
VR15 EFFECT DG. DP–2
IC4
VR19 BORDER GAIN–1
VR18 BORDER EDGE SPIKE COMP.
CT1 HUE PRESET–1
VR6 SC PHASE
VR5 LUMINANCE PRESET
VR7 MAT/BORDER DG. DP
VR10 MAT COLOR PHASE
IC9
IC10
IC1
VR8 BORDER GAIN–2
VR1 MAT KEY LEVEL
CT2 HUE PRESET--2
VR2 HUE
VR3 SATURATION
VR4 LUMINANCE
VR9 BL KILLER DC BIAS

WIPE PROCESS BOARD —Component Side —

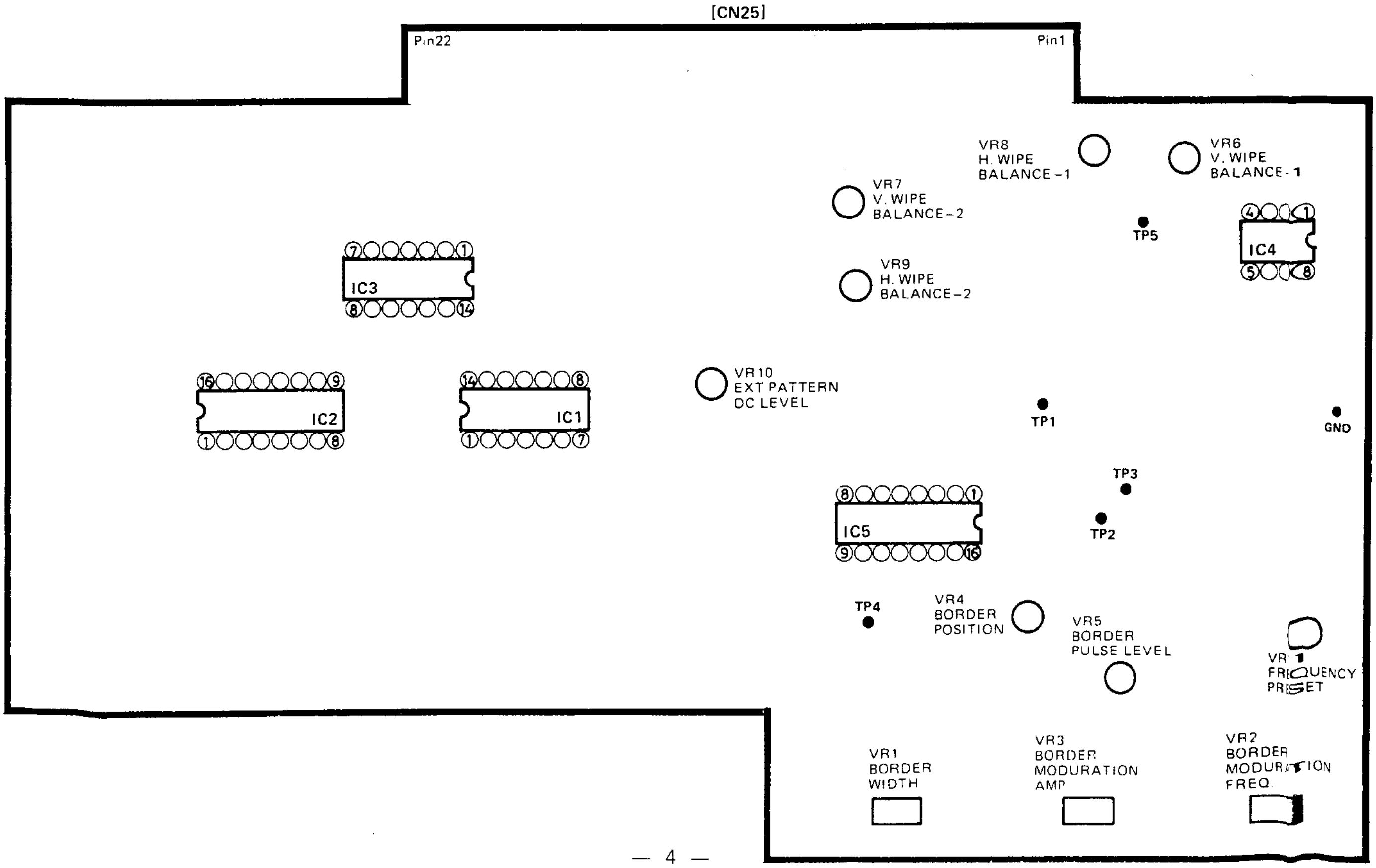
*Asterisk marked of contols are subjected to delete in future production.


[CN23]
Pin22
Pin1
GND
TP3
TP2
GND
VR4 H. TRIANGLE BORDER WIDTH
VR3 H. SAW–PARA BORDER WIDTH
TP1
IC5
IC2
IC1
VR1 V. SAW–PARA BORDER WIDTH
*VR2 V. TRIANGLE BORDER WIDTH
IC3
IC4

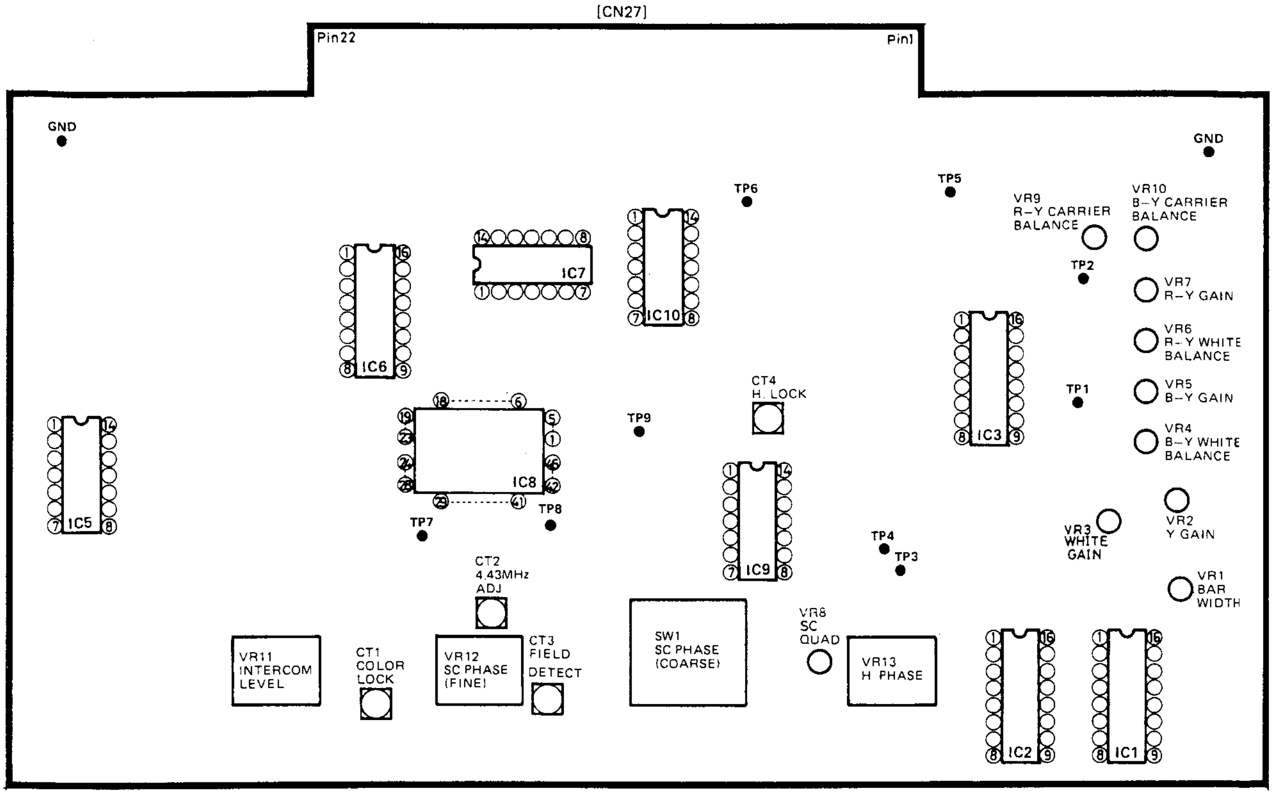
WAVEFORM GEN, BOARD —Component Side —


[CN24]
Pin22
Pin1
TP2
TP1
GND
VR7
H. CENT
VR6
H. POSITION
TP6
TP5
IC4
VR4
H. TRIANGLE
VR8
H. PARA
VR9
H. SAW
VR5
½ H. CONT
IC1
IC2
VR2
V. CENT
VR3
V. POSITION
TP4
IC3
VR10
V. TRIANGLE
VR1
½ V. CONT
TP3
VR12
V. NEG SAW
VR11
V. PARA
VR13
V. SAW

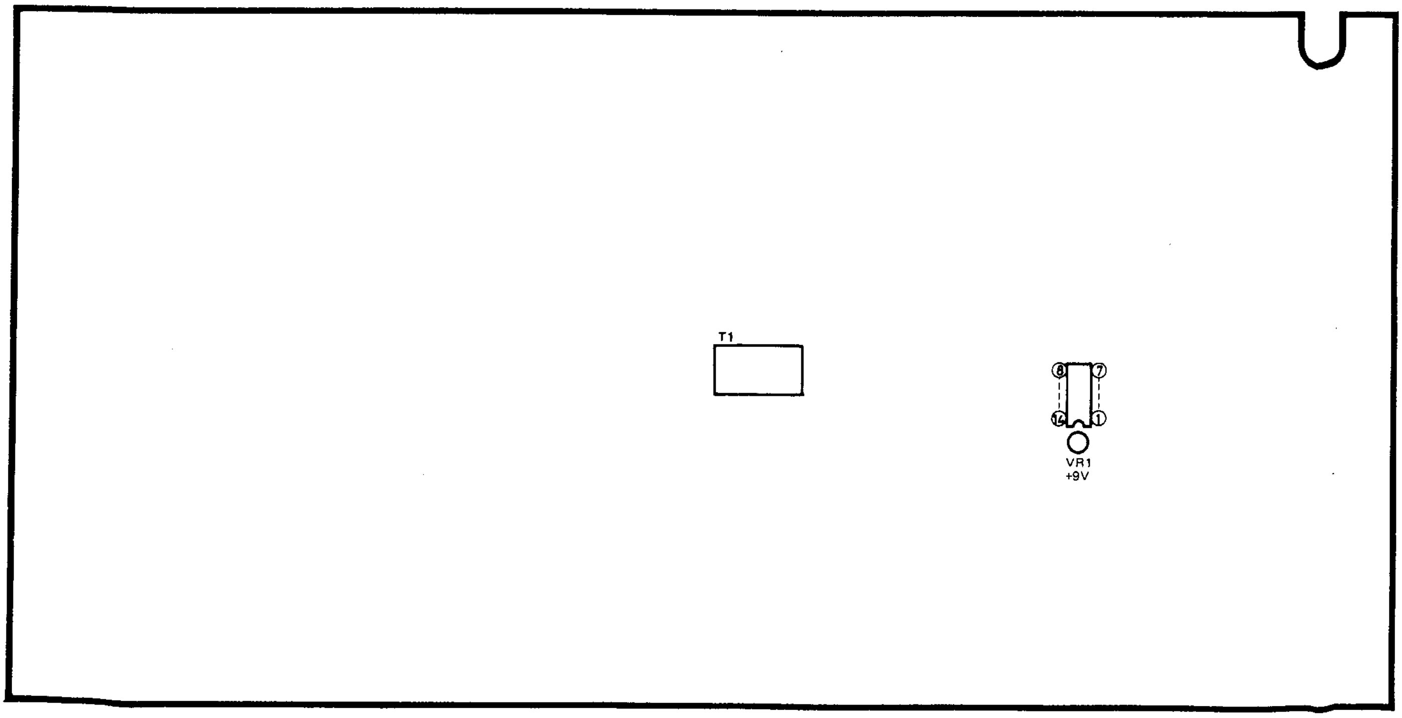
MODURATION BOARD —Component Side —


[CN25]
Pin22
Pin1
VR8
H. WIPE
BALANCE -1
VR6
V. WIPE
BALANCE -1
VR7
V. WIPE
BALANCE-2
TP5
IC4
IC3
VR9
H. WIPE
BALANCE-2
IC2
IC1
VR10
EXT PATTERN
DC LEVEL
TP1
GND
TP3
IC5
TP2
TP4
VR4
BORDER
POSITION
VR5
BORDER
PULSE LEVEL
VR
FREQUENCY
PRESET
VR1
BORDER
WIDTH
VR3
BORDER
MODURATION
AMP
VR2
BORDER
MODURATION
FREQ

SYNC, C/BAR BOARD — Component Side —


[CN27]
Pin22
Pin1
GND
GND
TP6
TP5
VR9
R–Y CARRIER
BALANCE
VR10
B–Y CARRIER
BALANCE
IC7
IC6
IC10
TP2
VR7
R–Y GAIN
VR6
R–Y WHITE
BALANCE
IC3
TP1
VR5
B–Y GAIN
CT4
H. LOCK
TP9
IC8
VR4
B–Y WHITE
BALANCE
IC5
TP7
TP8
IC9
VR3
WHITE
GAIN
VR2
Y GAIN
TP4
TP3
CT2
4.43MHz
ADJ
VR1
BAR
WIDTH
VR11
INTERCOM
LEVEL
CT1
COLOR
LOCK
VR12
SC PHASE
(FINE)
CT3
FIELD
DETECT
SW1
SC PHASE
(COARSE)
VR8
SC
QUAD
VR13
H PHASE
IC2
IC1

MOTHER BOARD — Component Side —

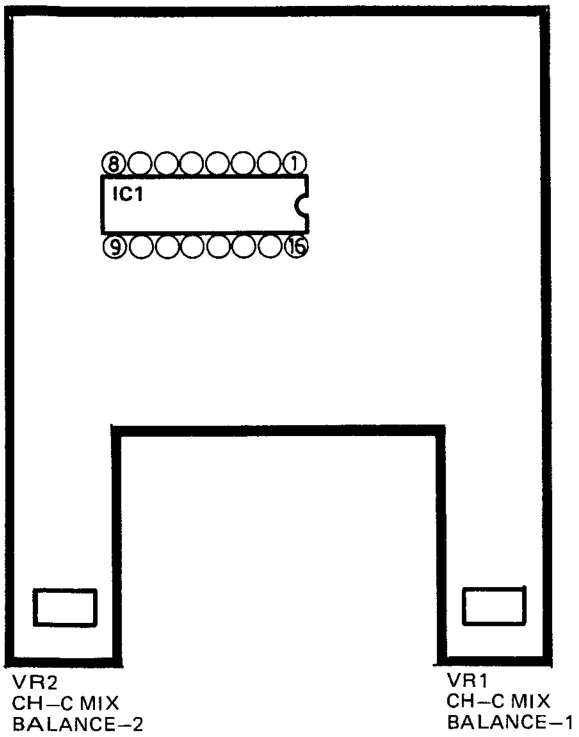


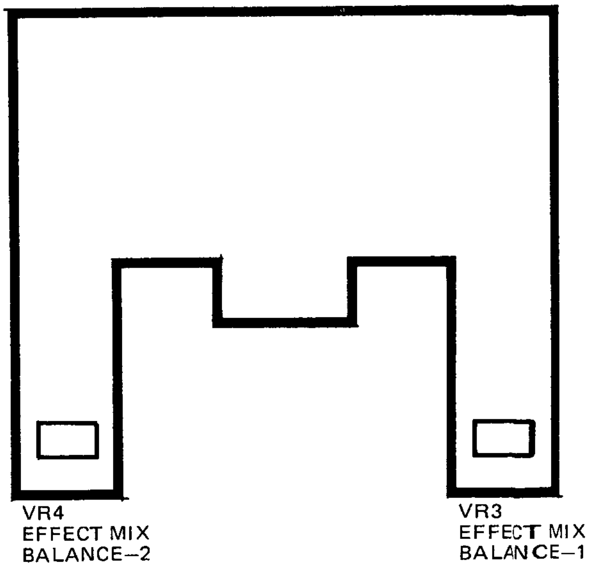
POSITION-1 BOARD

POSITION-2 BOARD

— Component Side —

(These circuit board a assembled with Lever Unit)


⑧
①
IC1
⑨
⑯
VR2
CH–C MIX
BALANCE–2
VR1
CH–C MIX
BALANCE–1


VR4
EFFECT MIX
BALANCE–2
VR3
EFFECT MIX
BALANCE–1

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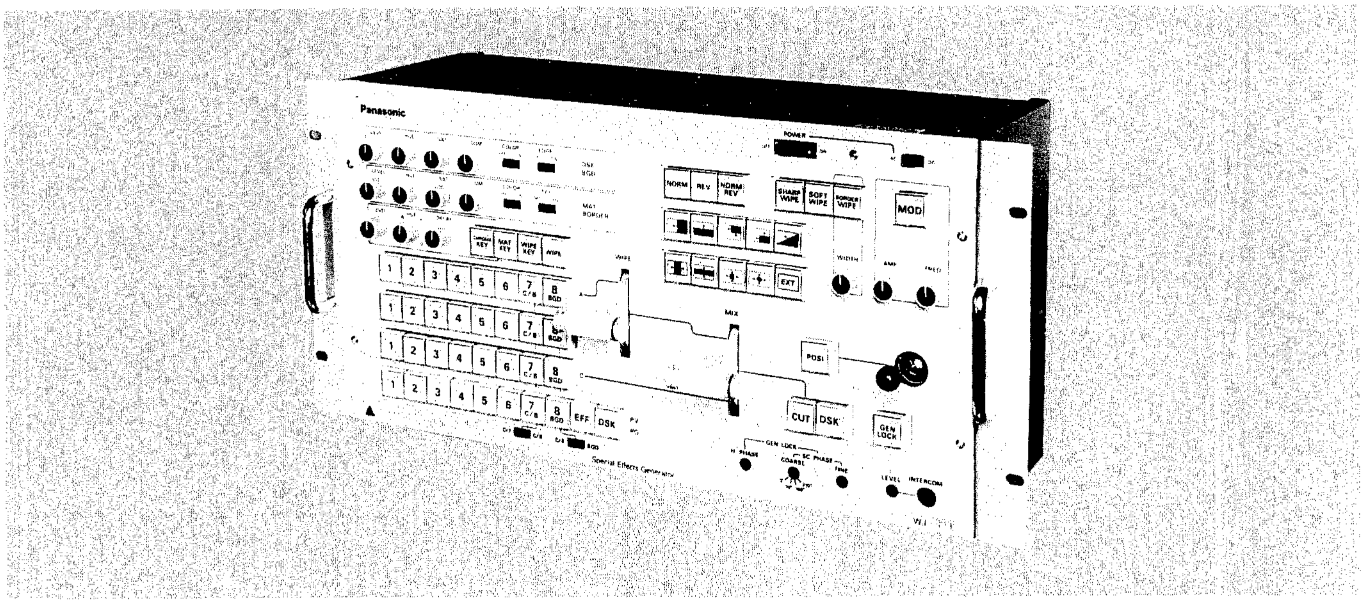
Service Manual

Vol. 3

Block Diagrams
Schematic Diagrams
Conductor Views

Special Effects Generator
WJ-5600


Panasonic
NORM
REV
NORM REV
SHARP WIPE
SOFT WIPE
BORDER WIPE
MOD
EXT
POSI
CUT
DSK
GEN LOCK
EFF
LEVEL
INTERCOM
Special Effects Generator

CONTENTS

BLOCK DIAGRAM

Block Diagram of WJ-5600 . . . . 1, 2
Output Board 3, 4
DSK, BGD Board 5, 6
Effect, Mix Board 7, 8
Chroma Key Board 9, 10
Wipe Process Board 11, 12
Waveform Gen. Board 13, 14
Modulation Board 15, 16
Sync, C/Bar Board 17, 18

SCHEMATIC DIAGRAM

Output Board 19, 20
DSK, BGD Board 23, 24
Effect, Mix Board 27, 28
Chroma Key/Delay/Level Board 31, 32
Input A/B/C Board 35, 36
Input PV-PG Board 39, 40
Wipe Process Board 43, 44
Waveform Gen. Board 47, 48
Modulation Board 51, 52
Lever/Position-1/Position-2 Board. 55, 56
Sync, C/Bar Board 59, 60
Mother Board 63, 64
Connector Board and Termination Board. 71, 72

CONDUCTOR VIEW

Output Board 21, 22
DSK, BGD Board 25, 26
Effect, Mix Board 29, 30
Chroma Key/Delay/Level Board 33, 34
Input A/B/C Board 37, 38
Input PV-PG Board 41, 42
Wipe Process Board 45, 46
Waveform Gen. Board 49, 50
Modulation Board 53, 54
Lever/Position-1/Position-2 Board. 57, 58
Sync, C/Bar Board 61, 62
Mother Board . . . . 65~67
Connector Board and Termination Board. . . . . . 68~70

Panasonic

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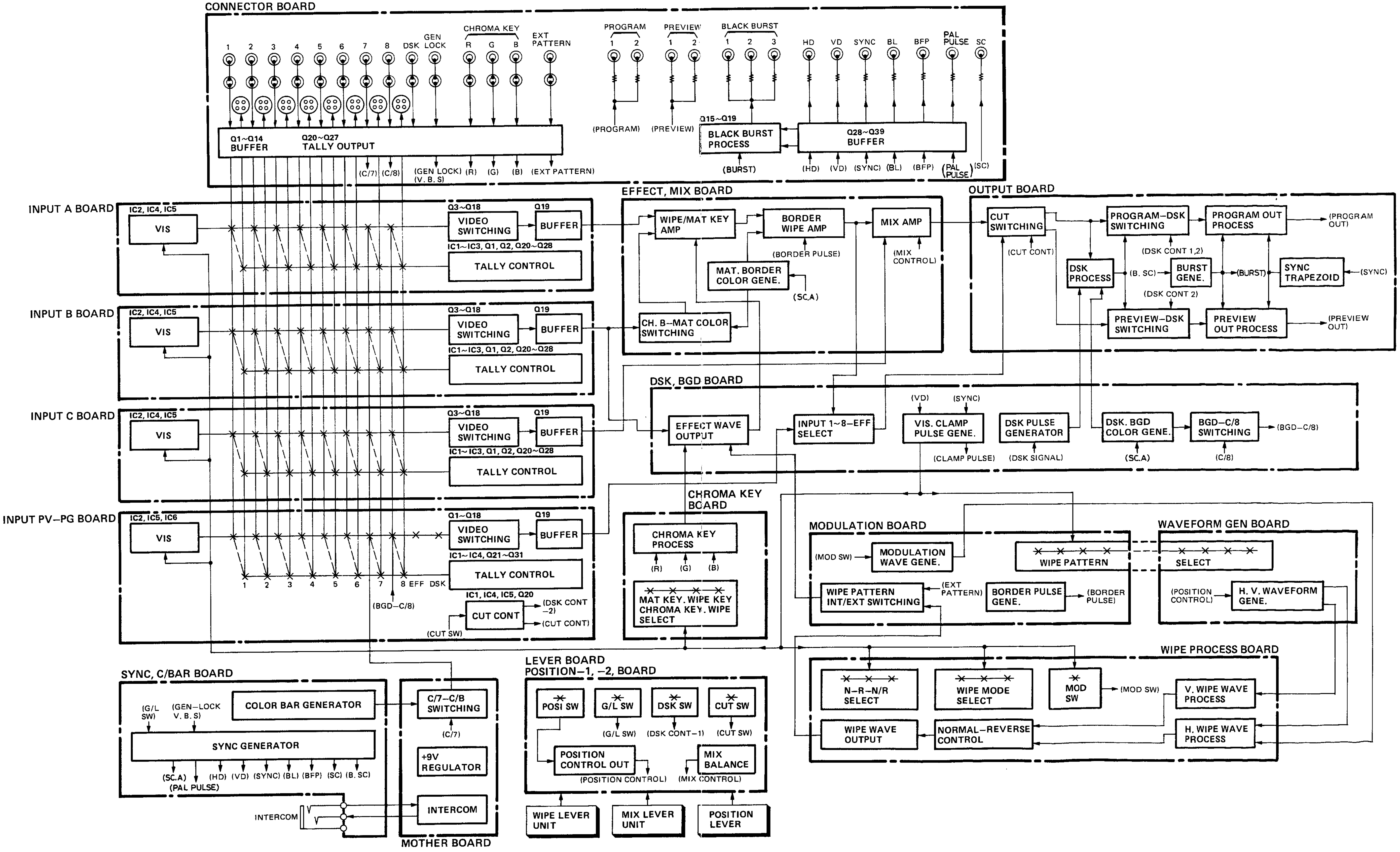
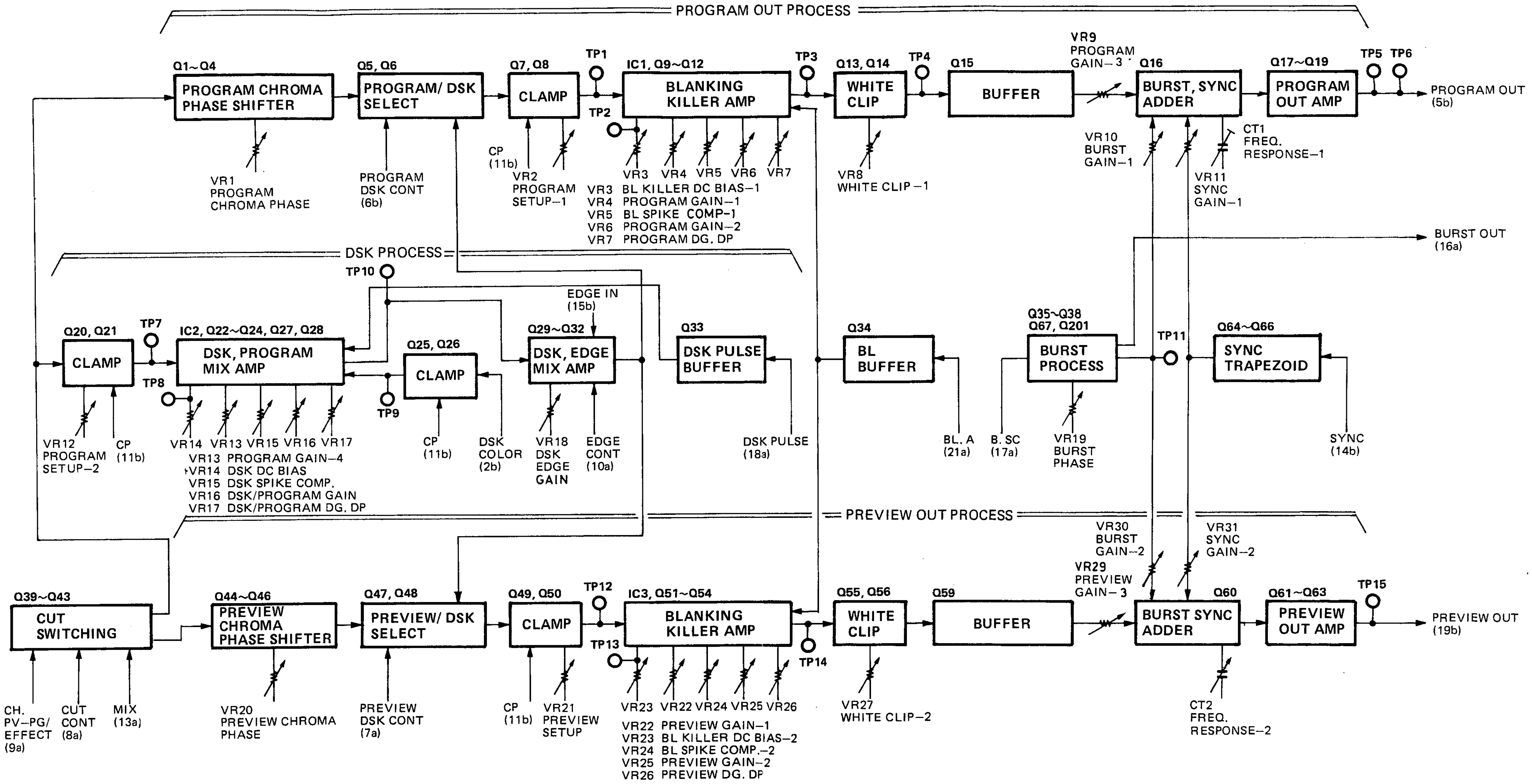
P.O. Box 288, Central Osaka Japan

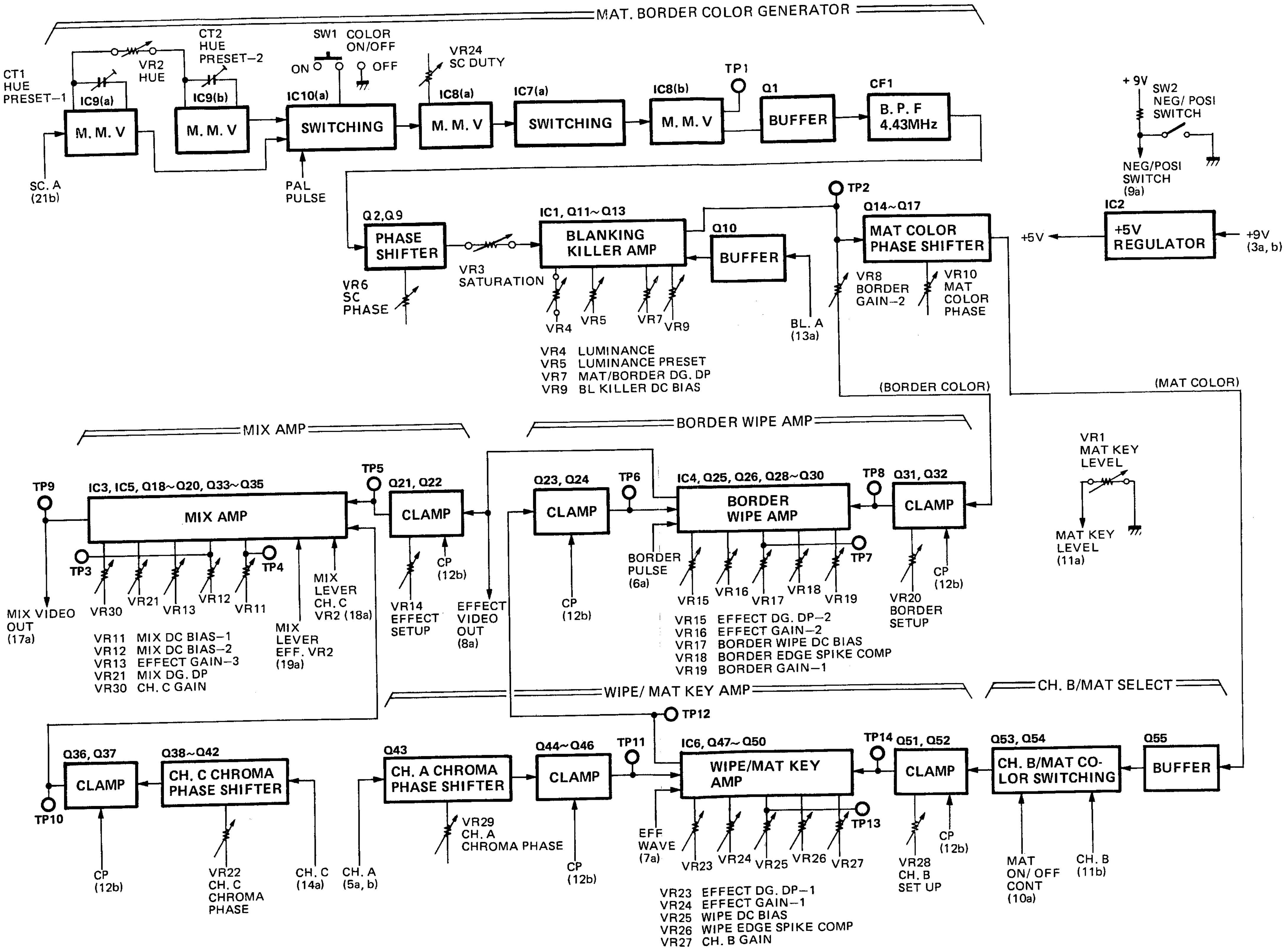
BLOCK DIAGRAM OF WJ-5600


CONNECTOR BOARD
1 2 3 4 5 6 7 8 DSK
GEN LOCK
CHROMA KEY
R G B
EXT PATTERN
PROGRAM 1 2
PREVIEW 1 2
BLACK BURST 1 2 3
HD VD SYNC BL BFP
PAL PULSE
SC
Q1~Q14 BUFFER
Q20~Q27 TALLY OUTPUT
(C/7) (C/8)
(GEN LOCK) (V. B. S)
(R) (G) (B) (EXT PATTERN)
(PROGRAM) (PREVIEW)
Q15~Q19
BLACK BURST PROCESS
(BURST)
Q28~Q39 BUFFER
(HD) (VD) (SYNC) (BL) (BFP) (PAL PULSE) (SC)
INPUT A BOARD
IC2, IC4, IC5
VIS
Q3~Q18 VIDEO SWITCHING
Q19 BUFFER
IC1~IC3, Q1, Q2, Q20~Q28
TALLY CONTROL
INPUT B BOARD
IC2, IC4, IC5
VIS
Q3~Q18 VIDEO SWITCHING
Q19 BUFFER
IC1~IC3, Q1, Q2, Q20~Q28
TALLY CONTROL
INPUT C BOARD
IC2, IC4, IC5
VIS
Q3~Q18 VIDEO SWITCHING
Q19 BUFFER
IC1~IC3, Q1, Q2, Q20~Q28
TALLY CONTROL
INPUT PV–PG BOARD
IC2, IC5, IC6
VIS
Q1~Q18 VIDEO SWITCHING
Q19 BUFFER
IC1~IC4, Q21~Q31
TALLY CONTROL
1 2 3 4 5 6 7 8 EFF DSK
(BGD–C/8)
IC1, IC4, IC5, Q20
CUT CONT
(DSK CONT –2)
(CUT CONT)
(CUT SW)
EFFECT, MIX BOARD
WIPE/MAT KEY AMP
BORDER WIPE AMP
MIX AMP
(BORDER PULSE)
(MIX CONTROL)
MAT. BORDER COLOR GENE.
(SC.A)
CH. B–MAT COLOR SWITCHING
OUTPUT BOARD
CUT SWITCHING
(CUT CONT)
PROGRAM–DSK SWITCHING
PROGRAM OUT PROCESS
(PROGRAM OUT)
(DSK CONT 1,2)
DSK PROCESS
(B. SC)
BURST GENE.
(BURST)
SYNC TRAPEZOID
(SYNC)
(DSK CONT 2)
PREVIEW–DSK SWITCHING
PREVIEW OUT PROCESS
(PREVIEW OUT)
DSK, BGD BOARD
EFFECT WAVE OUTPUT
INPUT 1~8–EFF SELECT
(VD) (SYNC)
VIS. CLAMP PULSE GENE.
(CLAMP PULSE)
DSK PULSE GENERATOR
(DSK SIGNAL)
DSK. BGD COLOR GENE.
(SC.A)
BGD–C/8 SWITCHING
(BGD–C/8)
(C/8)
CHROMA KEY BOARD
CHROMA KEY PROCESS
(R) (G) (B)
MAT KEY. WIPE KEY CHROMA KEY. WIPE SELECT
MODULATION BOARD
(MOD SW)
MODULATION WAVE GENE.
WIPE PATTERN
WIPE PATTERN INT/EXT SWITCHING
(EXT PATTERN)
BORDER PULSE GENE.
(BORDER PULSE)
WAVEFORM GEN BOARD
SELECT
(POSITION CONTROL)
H. V. WAVEFORM GENE.
WIPE PROCESS BOARD
N–R–N/R SELECT
WIPE MODE SELECT
MOD SW
(MOD SW)
V. WIPE WAVE PROCESS
WIPE WAVE OUTPUT
NORMAL–REVERSE CONTROL
H. WIPE WAVE PROCESS
SYNC, C/BAR BOARD
(G/L SW)
(GEN–LOCK V. B. S)
COLOR BAR GENERATOR
SYNC GENERATOR
(SC.A) (HD) (VD) (SYNC) (BL) (BFP) (SC) (B. SC)
(PAL PULSE)
INTERCOM
C/7–C/8 SWITCHING
(C/7)
+9V REGULATOR
INTERCOM
MOTHER BOARD
LEVER BOARD POSITION–1, –2, BOARD
POSI SW
G/L SW
DSK SW
CUT SW
(G/L SW) (DSK CONT–1) (CUT SW)
POSITION CONTROL OUT
MIX BALANCE
(POSITION CONTROL) (MIX CONTROL)
WIPE LEVER UNIT
MIX LEVER UNIT
POSITION LEVER

BLOCK DIAGRAM OF OUTPUT BOARD

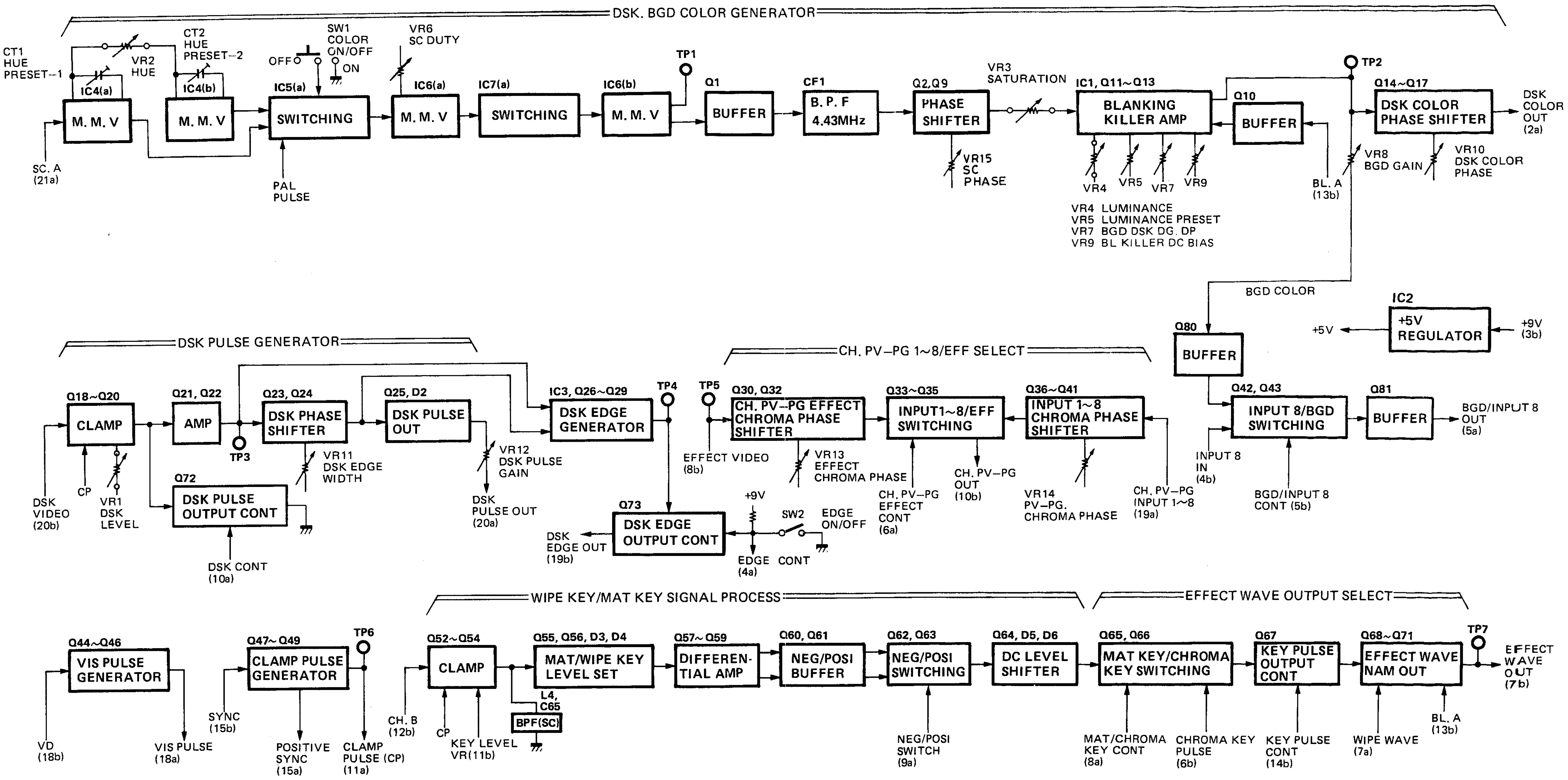

PROGRAM OUT PROCESS
Q1~Q4
PROGRAM CHROMA PHASE SHIFTER
Q5, Q6
PROGRAM/ DSK SELECT
Q7, Q8
CLAMP
TP1
TP2
IC1, Q9~Q12
BLANKING KILLER AMP
TP3
Q13, Q14
WHITE CLIP
TP4
Q15
BUFFER
VR9
PROGRAM
GAIN–3
Q16
BURST, SYNC ADDER
Q17~Q19
PROGRAM OUT AMP
TP5
TP6
PROGRAM OUT
(5b)
VR1
PROGRAM
CHROMA PHASE
PROGRAM
DSK CONT
(6b)
CP
(11b)
VR2
PROGRAM
SETUP–1
VR3 VR4 VR5 VR6 VR7
VR3 BL KILLER DC BIAS–1
VR4 PROGRAM GAIN–1
VR5 BL SPIKE COMP–1
VR6 PROGRAM GAIN–2
VR7 PROGRAM DG. DP
VR8
WHITE CLIP –1
VR10
BURST
GAIN–1
VR11
SYNC
GAIN–1
CT1
FREQ.
RESPONSE–1
BURST OUT
(16a)
DSK PROCESS
TP10
EDGE IN
(15b)
Q20, Q21
CLAMP
TP7
TP8
IC2, Q22~Q24, Q27, Q28
DSK, PROGRAM MIX AMP
Q25, Q26
CLAMP
TP9
Q29~Q32
DSK, EDGE MIX AMP
Q33
DSK PULSE BUFFER
Q34
BL BUFFER
Q35~Q38
Q67, Q201
BURST PROCESS
TP11
Q64~Q66
SYNC TRAPEZOID
VR12
PROGRAM
SETUP–2
CP
(11b)
VR14 VR13 VR15 VR16 VR17
VR13 PROGRAM GAIN–4
VR14 DSK DC BIAS
VR15 DSK SPIKE COMP.
VR16 DSK/PROGRAM GAIN
VR17 DSK/PROGRAM DG. DP
CP
(11b)
DSK
COLOR
(2b)
VR18
DSK
EDGE
GAIN
EDGE
CONT
(10a)
DSK PULSE
(18a)
BL. A
(21a)
B. SC
(17a)
VR19
BURST
PHASE
SYNC
(14b)
PREVIEW OUT PROCESS
VR30
BURST
GAIN–2
VR31
SYNC
GAIN–2
VR29
PREVIEW
GAIN– 3
Q39~Q43
CUT SWITCHING
Q44~Q46
PREVIEW CHROMA PHASE SHIFTER
Q47, Q48
PREVIEW/ DSK SELECT
Q49, Q50
CLAMP
TP12
TP13
IC3, Q51~Q54
BLANKING KILLER AMP
TP14
Q55, Q56
WHITE CLIP
Q59
BUFFER
Q60
BURST SYNC ADDER
Q61~Q63
PREVIEW OUT AMP
TP15
PREVIEW OUT
(19b)
CH.
PV–PG/
EFFECT
(9a)
CUT
CONT
(8a)
MIX
(13a)
VR20
PREVIEW CHROMA
PHASE
PREVIEW
DSK CONT
(7a)
CP
(11b)
VR21
PREVIEW
SETUP
VR23 VR22 VR24 VR25 VR26
VR22 PREVIEW GAIN–1
VR23 BL KILLER DC BIAS–2
VR24 BL SPIKE COMP.–2
VR25 PREVIEW GAIN–2
VR26 PREVIEW DG. DP
VR27
WHITE CLIP–2
CT2
FREQ.
RESPONSE–2

BLOCK DIAGRAM OF EFFECT,MIX BOARD

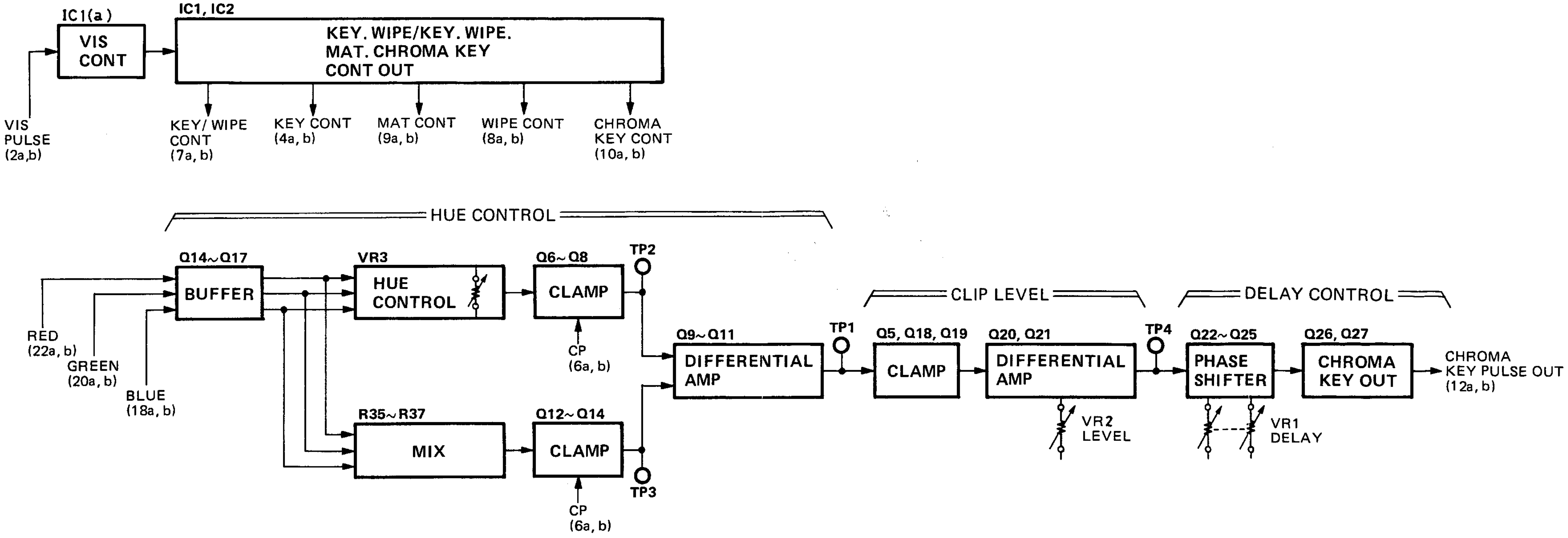


MAT. BORDER COLOR GENERATOR
CT1 HUE PRESET–1
VR2 HUE
CT2 HUE PRESET–2
SW1 COLOR ON/OFF
ON
OFF
VR24 SC DUTY
TP1
IC9(a)
M. M. V
IC9(b)
M. M. V
IC10(a)
SWITCHING
IC8(a)
M. M. V
IC7(a)
SWITCHING
IC8(b)
M. M. V
Q1
BUFFER
CF1
B. P. F 4.43MHz
SC. A (21b)
PAL PULSE
+9V
SW2 NEG/ POSI SWITCH
NEG/POSI SWITCH (9a)
TP2
Q2,Q9
PHASE SHIFTER
VR6 SC PHASE
VR3 SATURATION
IC1, Q11~Q13
BLANKING KILLER AMP
VR4
VR5
VR7
VR9
Q10
BUFFER
BL. A (13a)
Q14~Q17
MAT COLOR PHASE SHIFTER
VR8 BORDER GAIN–2
VR10 MAT COLOR PHASE
IC2
+5V REGULATOR
+5V
+9V (3a, b)
VR4 LUMINANCE
VR5 LUMINANCE PRESET
VR7 MAT/BORDER DG. DP
VR9 BL KILLER DC BIAS
(BORDER COLOR)
(MAT COLOR)
MIX AMP
BORDER WIPE AMP
VR1 MAT KEY LEVEL
MAT KEY LEVEL (11a)
TP9
IC3, IC5, Q18~Q20, Q33~Q35
MIX AMP
TP3
TP4
VR30
VR21
VR13
VR12
VR11
MIX VIDEO OUT (17a)
MIX LEVER CH. C VR2 (18a)
MIX LEVER EFF. VR2 (19a)
VR11 MIX DC BIAS–1
VR12 MIX DC BIAS–2
VR13 EFFECT GAIN–3
VR21 MIX DG. DP
VR30 CH. C GAIN
TP5
Q21, Q22
CLAMP
CP (12b)
VR14 EFFECT SETUP
EFFECT VIDEO OUT (8a)
Q23, Q24
CLAMP
CP (12b)
TP6
IC4, Q25, Q26, Q28~Q30
BORDER WIPE AMP
BORDER PULSE (6a)
VR15
VR16
VR17
VR18
VR19
TP7
TP8
Q31, Q32
CLAMP
CP (12b)
VR20 BORDER SETUP
VR15 EFFECT DG. DP–2
VR16 EFFECT GAIN–2
VR17 BORDER WIPE DC BIAS
VR18 BORDER EDGE SPIKE COMP
VR19 BORDER GAIN–1
WIPE/ MAT KEY AMP
CH. B/MAT SELECT
TP12
Q36, Q37
CLAMP
TP10
CP (12b)
Q38~Q42
CH. C CHROMA PHASE SHIFTER
VR22 CH. C CHROMA PHASE
CH. C (14a)
CH. A (5a, b)
Q43
CH. A CHROMA PHASE SHIFTER
VR29 CH. A CHROMA PHASE
Q44~Q46
CLAMP
CP (12b)
TP11
IC6, Q47~Q50
WIPE/MAT KEY AMP
EFF WAVE (7a)
VR23
VR24
VR25
VR26
VR27
TP13
TP14
Q51, Q52
CLAMP
VR28 CH. B SET UP
CP (12b)
Q53, Q54
CH. B/MAT COLOR SWITCHING
MAT ON/ OFF CONT (10a)
CH. B (11b)
Q55
BUFFER
VR23 EFFECT DG. DP–1
VR24 EFFECT GAIN–1
VR25 WIPE DC BIAS
VR26 WIPE EDGE SPIKE COMP
VR27 CH. B GAIN

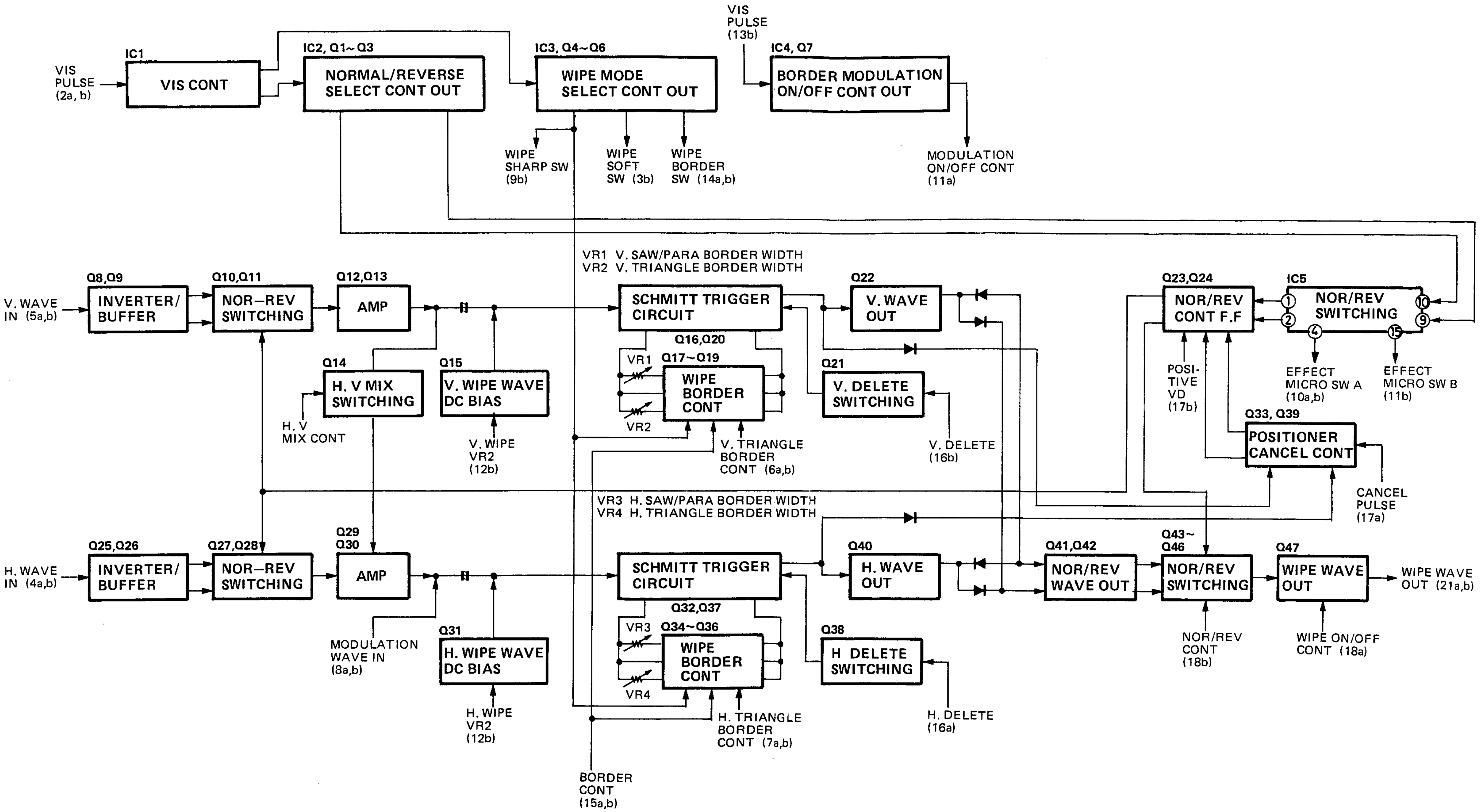
BLOCK DIAGRAM OF DSK,BGD BOARD


DSK. BGD COLOR GENERATOR
CT1 HUE PRESET–1
VR2 HUE
CT2 HUE PRESET–2
IC4(a)
M. M. V
IC4(b)
M. M. V
SC. A (21a)
SW1 COLOR ON/OFF
OFF
ON
IC5(a)
SWITCHING
PAL PULSE
VR6 SC DUTY
IC6(a)
M. M. V
IC7(a)
SWITCHING
IC6(b)
M. M. V
TP1
Q1
BUFFER
CF1
B. P. F 4.43MHz
Q2, Q9
PHASE SHIFTER
VR15 SC PHASE
VR3 SATURATION
IC1, Q11~Q13
BLANKING KILLER AMP
VR4
VR5
VR7
VR9
VR4 LUMINANCE
VR5 LUMINANCE PRESET
VR7 BGD DSK DG. DP
VR9 BL KILLER DC BIAS
Q10
BUFFER
BL. A (13b)
TP2
VR8 BGD GAIN
Q14~Q17
DSK COLOR PHASE SHIFTER
VR10 DSK COLOR PHASE
DSK COLOR OUT (2a)
BGD COLOR
IC2
+5V REGULATOR
+5V
+9V (3b)
Q80
BUFFER
DSK PULSE GENERATOR
Q18~Q20
CLAMP
DSK VIDEO (20b)
CP
VR1 DSK LEVEL
Q21, Q22
AMP
TP3
Q23, Q24
DSK PHASE SHIFTER
VR11 DSK EDGE WIDTH
Q72
DSK PULSE OUTPUT CONT
DSK CONT (10a)
Q25, D2
DSK PULSE OUT
VR12 DSK PULSE GAIN
DSK PULSE OUT (20a)
IC3, Q26~Q29
DSK EDGE GENERATOR
TP4
Q73
DSK EDGE OUTPUT CONT
DSK EDGE OUT (19b)
+9V
SW2 EDGE ON/OFF
EDGE CONT (4a)
CH. PV–PG 1~8/EFF SELECT
TP5
EFFECT VIDEO (8b)
Q30, Q32
CH. PV–PG EFFECT CHROMA PHASE SHIFTER
VR13 EFFECT CHROMA PHASE
Q33~Q35
INPUT1~8/EFF SWITCHING
CH. PV–PG EFFECT CONT (6a)
CH. PV–PG OUT (10b)
Q36~Q41
INPUT 1~8 CHROMA PHASE SHIFTER
VR14 PV–PG. CHROMA PHASE
CH. PV–PG INPUT 1~8 (19a)
Q42, Q43
INPUT 8/BGD SWITCHING
INPUT 8 IN (4b)
BGD/INPUT 8 CONT (5b)
Q81
BUFFER
BGD/INPUT 8 OUT (5a)
WIPE KEY/MAT KEY SIGNAL PROCESS
EFFECT WAVE OUTPUT SELECT
Q44~Q46
VIS PULSE GENERATOR
VD (18b)
VIS PULSE (18a)
Q47~Q49
CLAMP PULSE GENERATOR
SYNC (15b)
POSITIVE SYNC (15a)
TP6
CLAMP PULSE (CP) (11a)
Q52~Q54
CLAMP
CH. B (12b)
CP
KEY LEVEL VR(11b)
L4, C65
BPF(SC)
Q55, Q56, D3, D4
MAT/WIPE KEY LEVEL SET
Q57~Q59
DIFFEREN-TIAL AMP
Q60, Q61
NEG/POSI BUFFER
Q62, Q63
NEG/POSI SWITCHING
NEG/POSI SWITCH (9a)
Q64, D5, D6
DC LEVEL SHIFTER
Q65, Q66
MAT KEY/CHROMA KEY SWITCHING
MAT/CHROMA KEY CONT (8a)
CHROMA KEY PULSE (6b)
Q67
KEY PULSE OUTPUT CONT
KEY PULSE CONT (14b)
Q68~Q71
EFFECT WAVE NAM OUT
WIPE WAVE (7a)
BL. A (13b)
TP7
EFFECT WAVE OUT (7b)

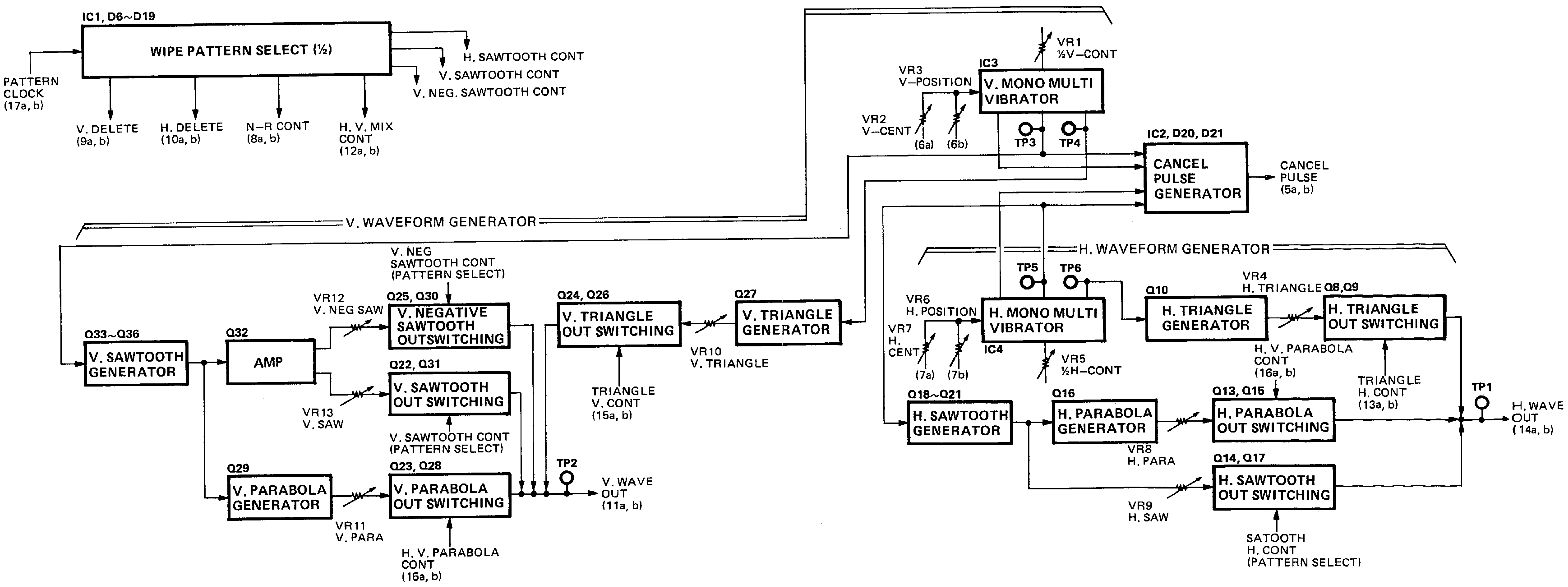
BLOCK DIAGRAM OF CHROMA KEY BOARD


IC1(a)
VIS CONT
IC1, IC2
KEY. WIPE/KEY. WIPE. MAT. CHROMA KEY CONT OUT
VIS PULSE (2a,b)
KEY/ WIPE CONT (7a, b)
KEY CONT (4a, b)
MAT CONT (9a, b)
WIPE CONT (8a, b)
CHROMA KEY CONT (10a, b)
HUE CONTROL
Q14~Q17
BUFFER
RED (22a, b)
GREEN (20a, b)
BLUE (18a, b)
VR3
HUE CONTROL
Q6~Q8
CLAMP
TP2
CP (6a, b)
R35~R37
MIX
Q12~Q14
CLAMP
TP3
CP (6a, b)
Q9~Q11
DIFFERENTIAL AMP
TP1
CLIP LEVEL
Q5, Q18, Q19
CLAMP
Q20, Q21
DIFFERENTIAL AMP
VR2 LEVEL
TP4
DELAY CONTROL
Q22~Q25
PHASE SHIFTER
VR1 DELAY
Q26, Q27
CHROMA KEY OUT
CHROMA KEY PULSE OUT (12a, b)

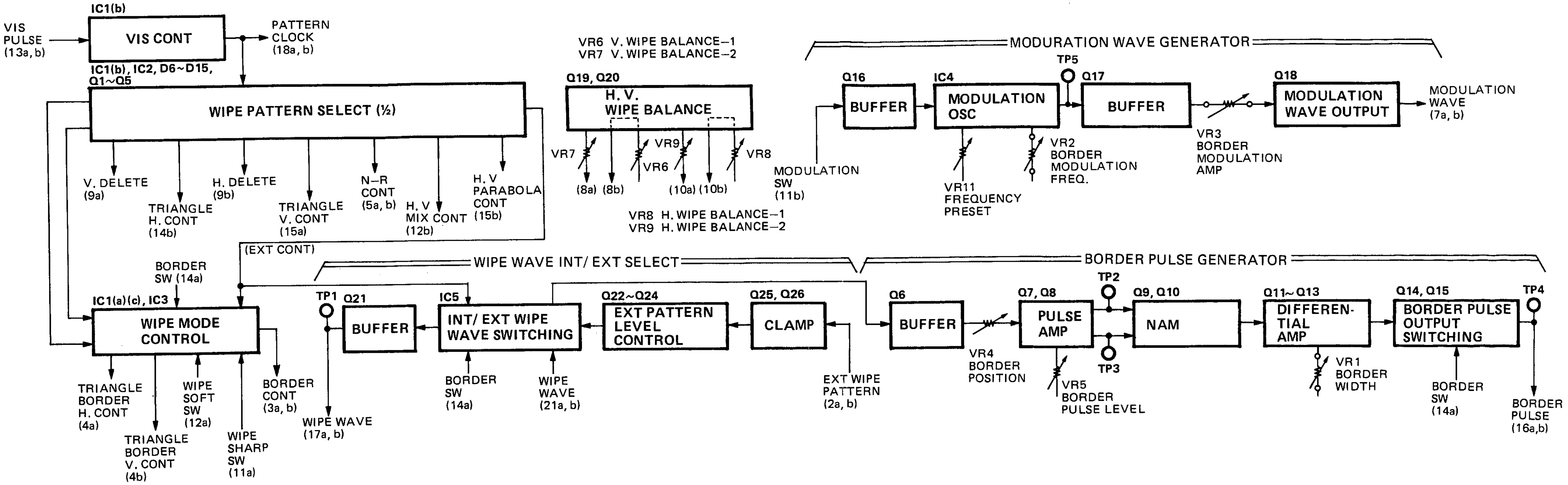
BLOCK DIAGRAM OF WIPE PROCESS BOARD


VIS PULSE (2a, b)
IC1
VIS CONT
IC2, Q1~Q3
NORMAL/REVERSE SELECT CONT OUT
IC3, Q4~Q6
WIPE MODE SELECT CONT OUT
WIPE SHARP SW (9b)
WIPE SOFT SW (3b)
WIPE BORDER SW (14a,b)
VIS PULSE (13b)
IC4, Q7
BORDER MODULATION ON/OFF CONT OUT
MODULATION ON/OFF CONT (11a)
VR1 V. SAW/PARA BORDER WIDTH
VR2 V. TRIANGLE BORDER WIDTH
V. WAVE IN (5a,b)
Q8,Q9
INVERTER/ BUFFER
Q10,Q11
NOR–REV SWITCHING
Q12,Q13
AMP
Q14
H. V MIX SWITCHING
H. V MIX CONT
Q15
V. WIPE WAVE DC BIAS
V. WIPE VR2 (12b)
SCHMITT TRIGGER CIRCUIT
Q16,Q20
VR1
Q17~Q19
WIPE BORDER CONT
VR2
V. TRIANGLE BORDER CONT (6a,b)
Q22
V. WAVE OUT
Q21
V. DELETE SWITCHING
V. DELETE (16b)
Q23,Q24
NOR/REV CONT F.F
IC5
NOR/REV SWITCHING
①
②
⑩
⑨
④
⑮
EFFECT MICRO SW A (10a,b)
EFFECT MICRO SW B (11b)
POSI-TIVE VD (17b)
Q33, Q39
POSITIONER CANCEL CONT
CANCEL PULSE (17a)
VR3 H. SAW/PARA BORDER WIDTH
VR4 H. TRIANGLE BORDER WIDTH
H. WAVE IN (4a,b)
Q25,Q26
INVERTER/ BUFFER
Q27,Q28
NOR–REV SWITCHING
Q29 Q30
AMP
MODULATION WAVE IN (8a,b)
Q31
H. WIPE WAVE DC BIAS
H. WIPE VR2 (12b)
SCHMITT TRIGGER CIRCUIT
Q32,Q37
VR3
Q34~Q36
WIPE BORDER CONT
VR4
H. TRIANGLE BORDER CONT (7a,b)
BORDER CONT (15a,b)
Q40
H. WAVE OUT
Q38
H DELETE SWITCHING
H. DELETE (16a)
Q41,Q42
NOR/REV WAVE OUT
Q43~ Q46
NOR/REV SWITCHING
NOR/REV CONT (18b)
Q47
WIPE WAVE OUT
WIPE ON/OFF CONT (18a)
WIPE WAVE OUT (21a,b)

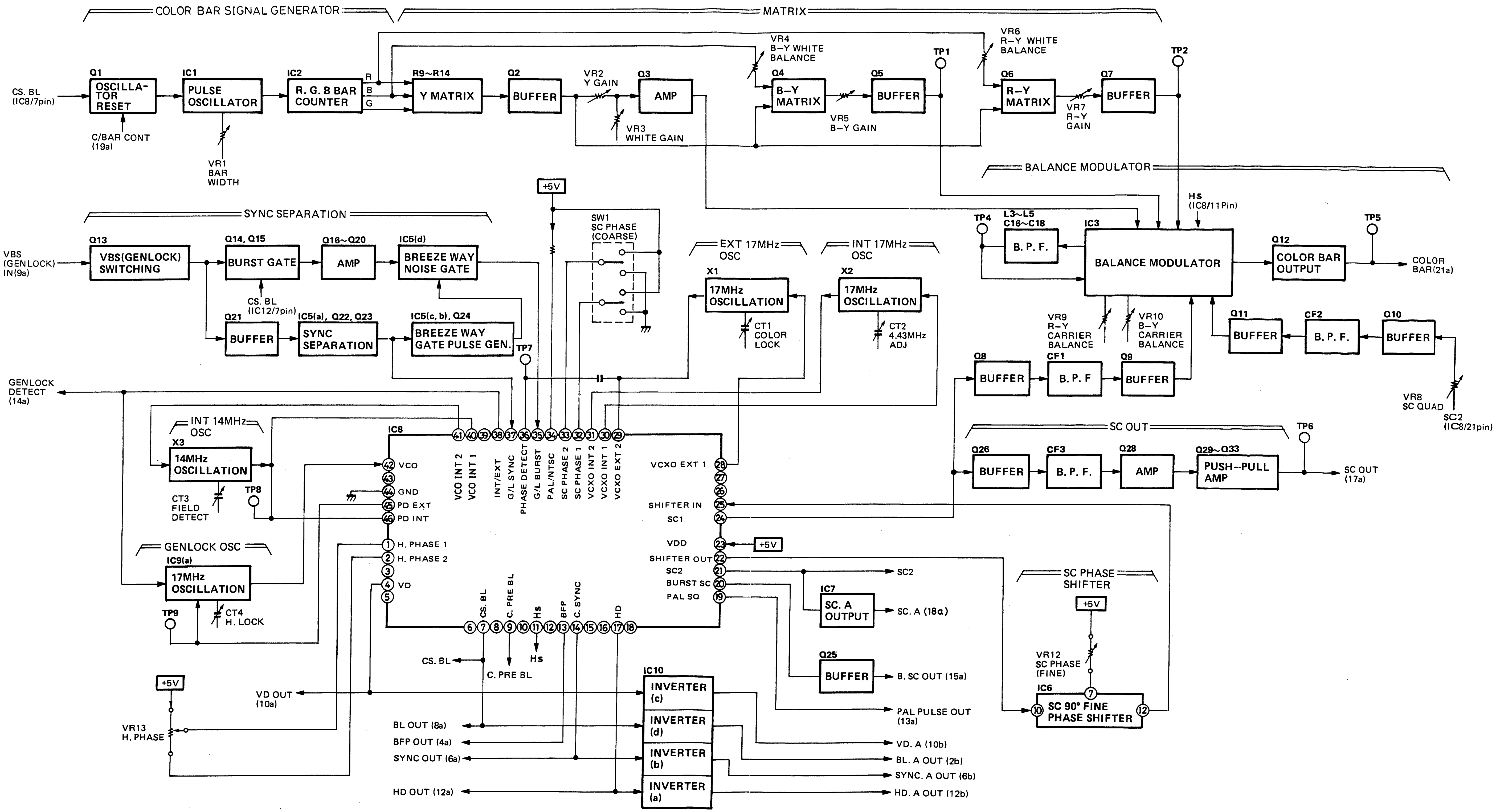
BLOCK DIAGRAM OF WAVEFORM GEN BOARD


IC1, D6~D19
WIPE PATTERN SELECT (½)
PATTERN CLOCK (17a, b)
H. SAWTOOTH CONT
V. SAWTOOTH CONT
V. NEG. SAWTOOTH CONT
V. DELETE (9a, b)
H. DELETE (10a, b)
N–R CONT (8a, b)
H. V. MIX CONT (12a, b)
V. WAVEFORM GENERATOR
Q33~Q36
V. SAWTOOTH GENERATOR
Q32
AMP
V. NEG SAWTOOTH CONT (PATTERN SELECT)
VR12 V. NEG SAW
Q25, Q30
V. NEGATIVE SAWTOOTH OUTSWITCHING
Q22, Q31
V. SAWTOOTH OUT SWITCHING
VR13 V. SAW
V. SAWTOOTH CONT (PATTERN SELECT)
Q29
V. PARABOLA GENERATOR
VR11 V. PARA
Q23, Q28
V. PARABOLA OUT SWITCHING
H. V. PARABOLA CONT (16a, b)
Q24, Q26
V. TRIANGLE OUT SWITCHING
TRIANGLE V. CONT (15a, b)
TP2
V. WAVE OUT (11a, b)
Q27
V. TRIANGLE GENERATOR
VR10 V. TRIANGLE
VR1 ½V–CONT
IC3
V. MONO MULTI VIBRATOR
VR3 V–POSITION
VR2 V–CENT
(6a)
(6b)
TP3
TP4
IC2, D20, D21
CANCEL PULSE GENERATOR
CANCEL PULSE (5a, b)
H. WAVEFORM GENERATOR
TP5
TP6
VR6 H. POSITION
VR7 H. CENT
(7a)
(7b)
H. MONO MULTI VIBRATOR
IC4
VR5 ½H–CONT
Q10
H. TRIANGLE GENERATOR
VR4 H. TRIANGLE
Q8, Q9
H. TRIANGLE OUT SWITCHING
H. V. PARABOLA CONT (16a, b)
TRIANGLE H. CONT (13a, b)
Q18~Q21
H. SAWTOOTH GENERATOR
Q16
H. PARABOLA GENERATOR
VR8 H. PARA
Q13, Q15
H. PARABOLA OUT SWITCHING
Q14, Q17
H. SAWTOOTH OUT SWITCHING
VR9 H. SAW
SATOOTH H. CONT (PATTERN SELECT)
TP1
H. WAVE OUT (14a, b)

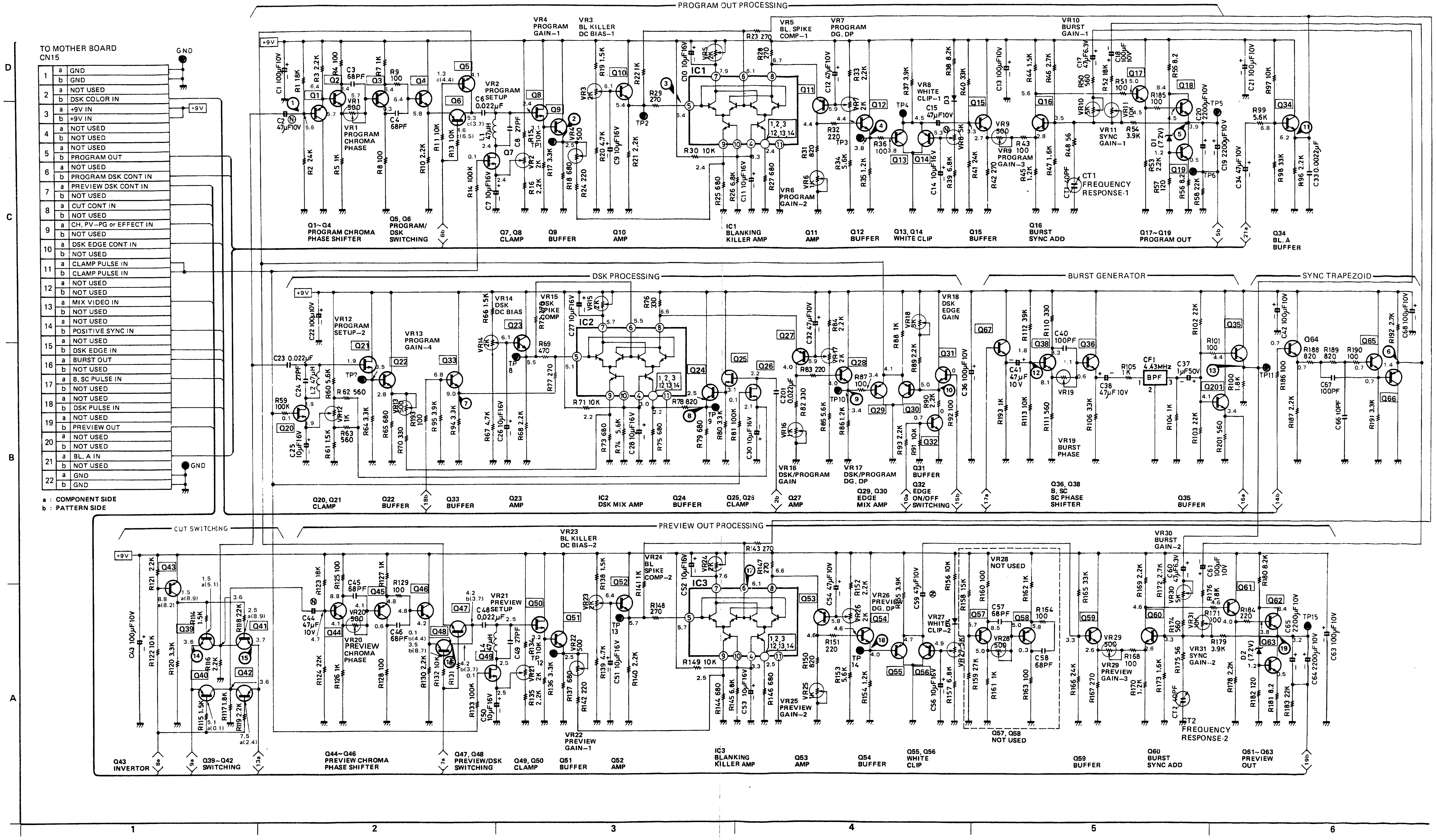
BLOCK DIAGRAM OF MODULATION BOARD


IC1(b)
VIS PULSE (13a, b)
VIS CONT
PATTERN CLOCK (18a, b)
IC1(b), IC2, D6~D15, Q1~Q5
WIPE PATTERN SELECT (½)
V. DELETE (9a)
TRIANGLE H. CONT (14b)
H. DELETE (9b)
TRIANGLE V. CONT (15a)
N–R CONT (5a, b)
H. V MIX CONT (12b)
H. V PARABOLA CONT (15b)
(EXT CONT)
BORDER SW (14a)
IC1(a)(c), IC3
WIPE MODE CONTROL
TRIANGLE BORDER H. CONT (4a)
TRIANGLE BORDER V. CONT (4b)
WIPE SOFT SW (12a)
WIPE SHARP SW (11a)
BORDER CONT (3a, b)
VR6 V. WIPE BALANCE–1
VR7 V. WIPE BALANCE–2
Q19, Q20
H. V. WIPE BALANCE
VR7
VR9
VR6
VR8
(8a) (8b)
(10a) (10b)
VR8 H. WIPE BALANCE–1
VR9 H. WIPE BALANCE–2
MODURATION WAVE GENERATOR
MODULATION SW (11b)
Q16
BUFFER
IC4
MODULATION OSC
TP5
Q17
BUFFER
Q18
MODULATION WAVE OUTPUT
MODULATION WAVE (7a, b)
VR11 FREQUENCY PRESET
VR2 BORDER MODULATION FREQ.
VR3 BORDER MODULATION AMP
WIPE WAVE INT/ EXT SELECT
TP1
Q21
BUFFER
WIPE WAVE (17a, b)
IC5
INT/ EXT WIPE WAVE SWITCHING
BORDER SW (14a)
WIPE WAVE (21a, b)
Q22~Q24
EXT PATTERN LEVEL CONTROL
Q25, Q26
CLAMP
EXT WIPE PATTERN (2a, b)
BORDER PULSE GENERATOR
Q6
BUFFER
VR4 BORDER POSITION
Q7, Q8
PULSE AMP
TP2
TP3
VR5 BORDER PULSE LEVEL
Q9, Q10
NAM
Q11~Q13
DIFFEREN-TIAL AMP
VR1 BORDER WIDTH
Q14, Q15
BORDER PULSE OUTPUT SWITCHING
TP4
BORDER SW (14a)
BORDER PULSE (16a,b)

BLOCK DIAGRAM OF SYNC,C/BAR BOARD


COLOR BAR SIGNAL GENERATOR
MATRIX
CS. BL (IC8/7pin)
Q1
OSCILLA-TOR RESET
C/BAR CONT (19a)
IC1
PULSE OSCILLATOR
VR1 BAR WIDTH
IC2
R. G. B BAR COUNTER
R
B
G
R9~R14
Y MATRIX
Q2
BUFFER
VR2 Y GAIN
Q3
AMP
VR3 WHITE GAIN
VR4 B–Y WHITE BALANCE
Q4
B–Y MATRIX
VR5 B–Y GAIN
Q5
BUFFER
TP1
VR6 R–Y WHITE BALANCE
Q6
R–Y MATRIX
VR7 R–Y GAIN
Q7
BUFFER
TP2
BALANCE MODULATOR
Hs (IC8/11Pin)
TP4
L3~L5 C16~C18
B. P. F.
IC3
BALANCE MODULATOR
Q12
COLOR BAR OUTPUT
TP5
COLOR BAR(21a)
VR9 R–Y CARRIER BALANCE
VR10 B–Y CARRIER BALANCE
Q11
BUFFER
CF2
B. P. F.
Q10
BUFFER
VR8 SC QUAD
SC2 (IC8/21pin)
Q8
BUFFER
CF1
B. P. F
Q9
BUFFER
SYNC SEPARATION
VBS (GENLOCK) IN(9a)
Q13
VBS(GENLOCK) SWITCHING
Q14, Q15
BURST GATE
CS. BL (IC12/7pin)
Q16~Q20
AMP
IC5(d)
BREEZE WAY NOISE GATE
Q21
BUFFER
IC5(a), Q22, Q23
SYNC SEPARATION
IC5(c, b), Q24
BREEZE WAY GATE PULSE GEN.
TP7
+5V
SW1 SC PHASE (COARSE)
EXT 17MHz OSC
X1
17MHz OSCILLATION
CT1 COLOR LOCK
INT 17MHz OSC
X2
17MHz OSCILLATION
CT2 4.43MHz ADJ
GENLOCK DETECT (14a)
INT 14MHz OSC
X3
14MHz OSCILLATION
CT3 FIELD DETECT
TP8
GENLOCK OSC
IC9(a)
17MHz OSCILLATION
TP9
CT4 H. LOCK
+5V
VR13 H. PHASE
IC8
41 40 39 38 37 36 35 34 33 32 31 30 29
VCO INT 2
VCO INT 1
INT/EXT
G/L SYNC
PHASE DETECT
G/L BURST
PAL/NTSC
SC PHASE 2
SC PHASE 1
VCXO INT 2
VCXO INT 1
VCXO EXT 2
42 VCO
43
44 GND
45 PD EXT
46 PD INT
1 H. PHASE 1
2 H. PHASE 2
3
4 VD
5
VCXO EXT 1 28
27
26
SHIFTER IN 25
SC1 24
VDD 23
+5V
SHIFTER OUT 22
SC2 21
BURST SC 20
PAL SQ 19
6 7 8 9 10 11 12 13 14 15 16 17 18
CS. BL
C. PRE BL
Hs
BFP
C. SYNC
HD
CS. BL
C. PRE BL
Hs
SC2
IC7
SC. A OUTPUT
SC. A (18a)
Q25
BUFFER
B. SC OUT (15a)
PAL PULSE OUT (13a)
SC OUT
TP6
Q26
BUFFER
CF3
B. P. F.
Q28
AMP
Q29~Q33
PUSH–PULL AMP
SC OUT (17a)
SC PHASE SHIFTER
+5V
VR12 SC PHASE (FINE)
IC6
7
10
12
SC 90° FINE PHASE SHIFTER
VD OUT (10a)
BL OUT (8a)
BFP OUT (4a)
SYNC OUT (6a)
HD OUT (12a)
IC10
INVERTER (c)
INVERTER (d)
INVERTER (b)
INVERTER (a)
VD. A (10b)
BL. A OUT (2b)
SYNC. A OUT (6b)
HD. A OUT (12b)

SCHEMATIC DIAGRAM OF OUTPUT BOARD


PROGRAM OUT PROCESSING
DSK PROCESSING
BURST GENERATOR
SYNC TRAPEZOID
PREVIEW OUT PROCESSING
CUT SWITCHING
TO MOTHER BOARD CN15
GND
1 a GND
b GND
2 a NOT USED
b DSK COLOR IN
3 a +9V IN
b +9V IN
4 a NOT USED
b NOT USED
5 a NOT USED
b PROGRAM OUT
6 a NOT USED
b PROGRAM DSK CONT IN
7 a PREVIEW DSK CONT IN
b NOT USED
8 a CUT CONT IN
b NOT USED
9 a CH, PV–PG or EFFECT IN
b NOT USED
10 a DSK EDGE CONT IN
b NOT USED
11 a CLAMP PULSE IN
b CLAMP PULSE IN
12 a NOT USED
b NOT USED
13 a MIX VIDEO IN
b NOT USED
14 a NOT USED
b POSITIVE SYNC IN
15 a NOT USED
b DSK EDGE IN
16 a BURST OUT
b NOT USED
17 a B, SC PULSE IN
b NOT USED
18 a NOT USED
b DSK PULSE IN
19 a NOT USED
b PREVIEW OUT
20 a NOT USED
b NOT USED
21 a BL, A IN
b NOT USED
22 a GND
b GND
a : COMPONENT SIDE
b : PATTERN SIDE
Q1~Q4 PROGRAM CHROMA PHASE SHIFTER
Q5, Q6 PROGRAM/DSK SWITCHING
Q7, Q8 CLAMP
Q9 BUFFER
Q10 AMP
IC1 BLANKING KILLER AMP
Q11 AMP
Q12 BUFFER
Q13, Q14 WHITE CLIP
Q15 BUFFER
Q16 BURST SYNC ADD
Q17~Q19 PROGRAM OUT
Q34 BL. A BUFFER
Q20, Q21 CLAMP
Q22 BUFFER
Q33 BUFFER
Q23 AMP
IC2 DSK MIX AMP
Q24 BUFFER
Q25, Q26 CLAMP
Q27 AMP
Q29, Q30 EDGE MIX AMP
Q31 BUFFER
Q32 EDGE ON/OFF SWITCHING
Q36, Q38 B. SC SC PHASE SHIFTER
Q35 BUFFER
Q43 INVERTOR
Q39~Q42 SWITCHING
Q44~Q46 PREVIEW CHROMA PHASE SHIFTER
Q47, Q48 PREVIEW/DSK SWITCHING
Q49, Q50 CLAMP
Q51 BUFFER
Q52 AMP
IC3 BLANKING KILLER AMP
Q53 AMP
Q54 BUFFER
Q55, Q56 WHITE CLIP
Q57, Q58 NOT USED
Q59 BUFFER
Q60 BURST SYNC ADD
Q61~Q63 PREVIEW OUT
VR1 PROGRAM CHROMA PHASE
VR2 PROGRAM SETUP
VR3 BL KILLER DC BIAS–1
VR4 PROGRAM GAIN–1
VR5 BL SPIKE COMP–1
VR6 PROGRAM GAIN–2
VR7 PROGRAM DG. DP
VR8 WHITE CLIP–1
VR9 PROGRAM GAIN–3
VR10 BURST GAIN–1
VR11 SYNC GAIN–1
CT1 FREQUENCY RESPONSE-1
VR12 PROGRAM SETUP–2
VR13 PROGRAM GAIN–4
VR14 DSK DC BIAS
VR15 DSK SPIKE COMP
VR16 DSK/PROGRAM GAIN
VR17 DSK/PROGRAM DG. DP
VR18 DSK EDGE GAIN
VR19 BURST PHASE
VR20 PREVIEW CHROMA PHASE
VR21 PREVIEW SETUP
VR22 PREVIEW GAIN–1
VR23 BL KILLER DC BIAS–2
VR24 BL SPIKE COMP–2
VR25 PREVIEW GAIN–2
VR26 PREVIEW DG. DP
VR27 WHITE CLIP–2
VR28 NOT USED
VR29 PREVIEW GAIN–3
VR30 BURST GAIN–2
VR31 SYNC GAIN–2
CT2 FREQUENCY RESPONSE-2
CF1 4.43MHz BPF
+9V
TP1
TP2
TP5
TP6
TP7
TP8
TP9
TP10
TP11
TP12
TP13
TP14
TP15
A
B
C
D
1
2
3
4
5
6

Voltages are measured by following conditions

a( ) : CUT ——→ ON

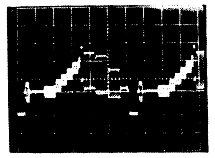
b( ) : DSK PV PG ——→ ON

c( ) : DSK ——→ ON

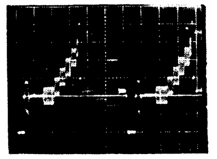
IC1	AN610P	C3, C4
IC2	AN610P	B3
IC3	AN610P	A3, A4
Q1	2SA1254-BC	C2
Q2	2SD636-RS	D2
Q3	2SA1254-BC	D2
Q4	2SD636-RS	D2
Q5	2SC2377CD	D2
Q6	2SA1254-BC	C2
Q7	2SK34-CD	C2, C3
Q8	2SK19-Y	C3
Q9	2SD636-RS	C3
Q10	2SD636-RS	D3
Q11	2SA1254-BC	C4
Q12	2SD636-RS	C4
Q13	2SA1254-BC	C4
Q14	2SA1254-BC	C4
Q15	2SD636-RS	C5
Q16	2SC2377CD	C5
Q17	2SD636-RS	D5
Q18	2SD639RS	C5
Q19	2SD639RS	C5
Q20	2SK34-CD	B2
Q21	2SK19-Y	B2
Q22	2SD636-RS	B2
Q23	2SD636-RS	B3
Q24	2SD636-RS	B3
Q25	2SK19-Y	B3
Q26	2SK34-CD	B4
Q27	2SA1254-BC	B4
Q28	2SD636-RS	B4
Q29	2SA1254-BC	B4
Q30	2SA1254-BC	B4
Q31	2SD636-RS	B4
Q32	2SD636-RS	B4
Q33	2SD636-RS	B2
Q34	2SD636-RS	C6
Q35	2SD636-RS	B6
Q36	2SD636-RS	B5
Q38	2SD636-RS	B5
Q39	2SC2377CD	A1
Q40	2SC2377CD	A1
Q41	2SA1254-BC	A1
Q42	2SA1254-BC	A1
Q43	2SA1254-BC	A1
Q44	2SD636-RS	A2
Q45	2SA1254-BC	A2
Q46	2SD636-RS	A2
Q47	2SC2377CD	A2
Q48	2SA1254-BC	A2
Q49	2SK34-CD	A2
Q50	2SK19-Y	A3
Q51	2SD636-RS	A3
Q52	2SD636-RS	A3
Q53	2SA1254-BC	A4
Q54	2SD636-RS	A4
Q55	2SA1254-BC	A4
Q56	2SA1254-BC	A4
Q57	2SD636-RS	A5
Q58	2SA1254-BC	A5
Q59	2SD636-RS	A5
Q60	2SC2377CD	A5
Q61	2SD636-RS	A6
Q62	2SD639RS	A6
Q63	2SD639RS	A6
Q64	2SD636-RS	B6
Q65	2SD636-RS	B6
Q66	2SA1254-BC	B6
Q67	2SC828-QR	B5
Q201	2SC828-QR	B6
D1	MA4075L	C5
D2	MA4075L	A6
D3	MA27WA	D4
D4	MA27WA	A4

CONDUCTOR VIEW OF OUTPUT BOARD

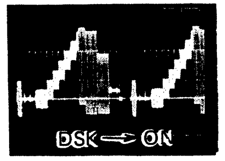
1. 0.2V/DIV 10μs/DIV



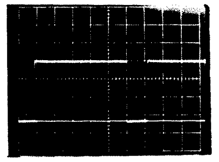
2. 0.1V/DIV 10μs/DIV



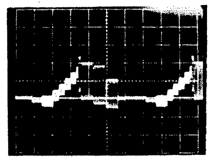
2. 0.1V/DIV 10μs/DIV



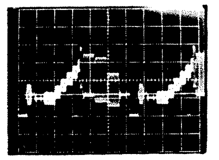
3. 0.5V/DIV 10μs/DIV



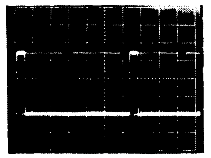
4. 0.2V/DIV 10μs/DIV



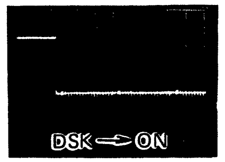
5. 0.5V/DIV 10μs/DIV



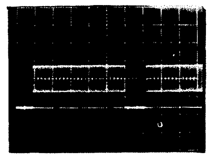
6. 2.0V/DIV 10μs/DIV



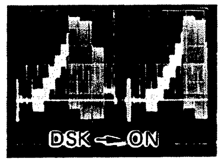
7. 0.5V/DIV 20μs/DIV



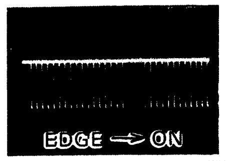
8. 0.2V/DIV 10μs/DIV



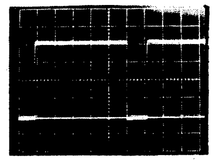
9. 0.1V/DIV 10μs/DIV



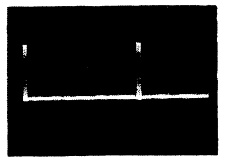
10. 0.2V/DIV 10μs/DIV



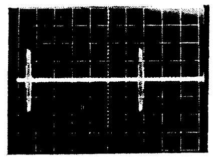
11. 0.5V/DIV 10μs/DIV



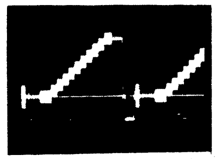
12. 0.5V/DIV 10μs/DIV



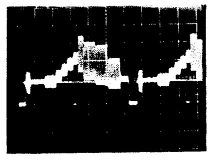
13. 0.2V/DIV 10μs/DIV



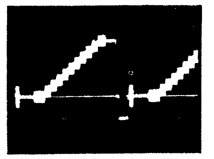
14. 0.2V/DIV 10μs/DIV



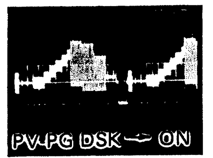
15. 0.2V/DIV 10μs/DIV



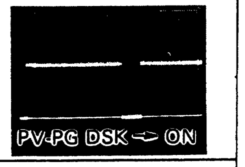
16. 0.2V/DIV 10μs/DIV



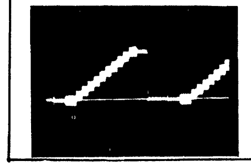
16. 0.5V/DIV 10μs/DIV



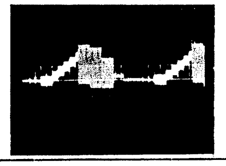
17. 0.2V/DIV 10μs/DIV



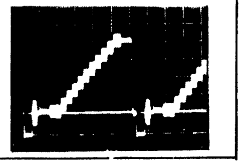
18. 0.2V/DIV 10μs/DIV

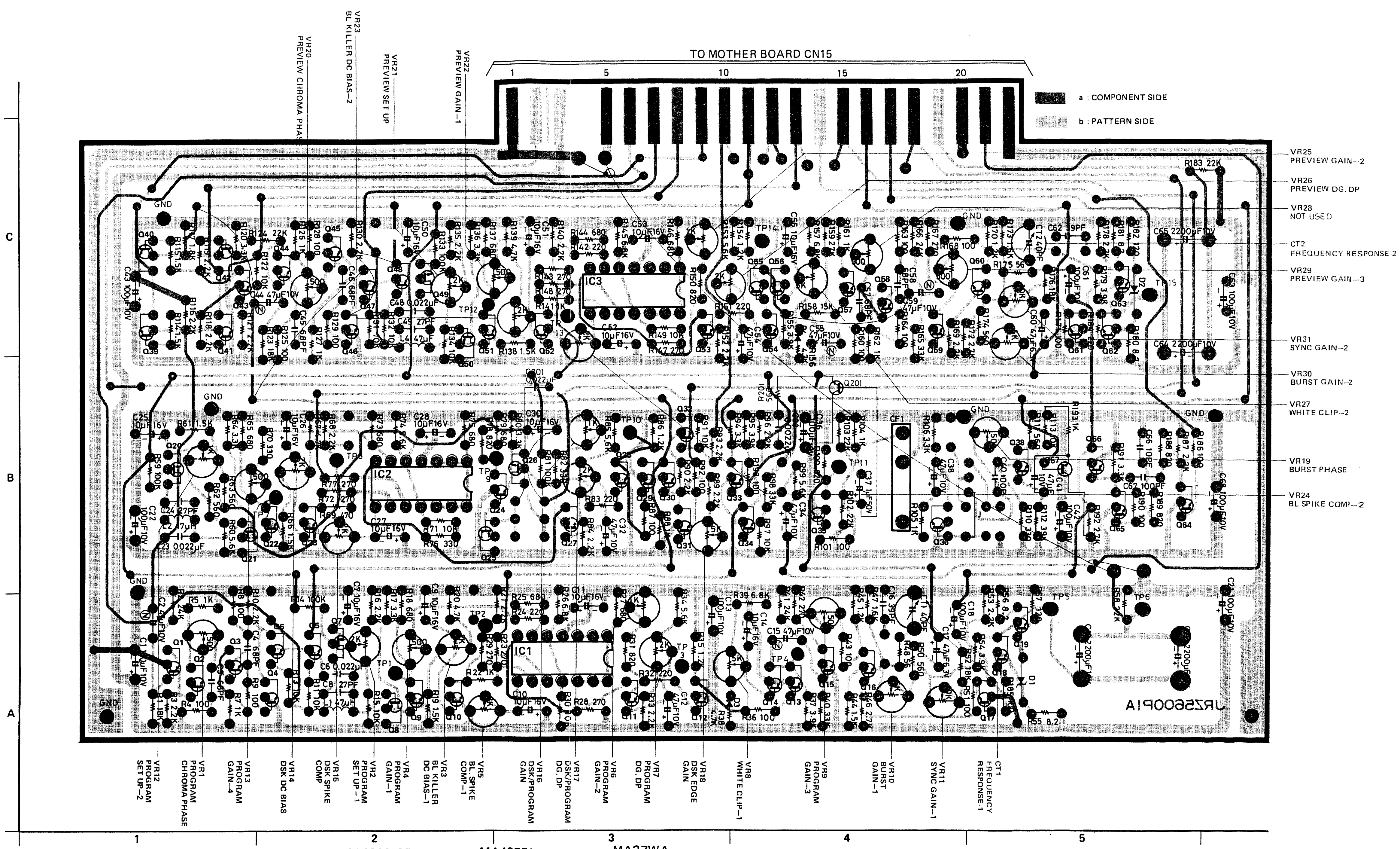


18. 0.2V/DIV 10μs/DIV

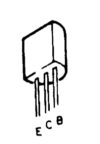


19. 0.5V/DIV 10μs/DIV

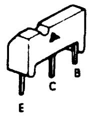



VR20 PREVIEW CHROMA PHASE
VR23 BL KILLER DC BIAS–2
VR21 PREVIEW SET UP
VR22 PREVIEW GAIN–1
TO MOTHER BOARD CN15
1
5
10
15
20
a : COMPONENT SIDE
b : PATTERN SIDE
VR25 PREVIEW GAIN–2
VR26 PREVIEW DG. DP
VR28 NOT USED
CT2 FREQUENCY RESPONSE-2
VR29 PREVIEW GAIN–3
VR31 SYNC GAIN–2
VR30 BURST GAIN–2
VR27 WHITE CLIP–2
VR19 BURST PHASE
VR24 BL SPIKE COMP–2
C
B
A
IC1
IC2
IC3
CF1
GND
VR12 PROGRAM SET UP–2
VR1 PROGRAM CHROMA PHASE
VR13 PROGRAM GAIN–4
VR14 DSK DC BIAS
VR15 DSK SPIKE COMP
VR2 PROGRAM SET UP – 1
VR4 PROGRAM GAIN–1
VR3 BL KILLER DC BIAS–1
VR5 BL. SPIKE COMP–1
VR16 DSK/PROGRAM GAIN
VR17 DSK/PROGRAM DG. DP
VR6 PROGRAM GAIN–2
VR7 PROGRAM DG. DP
VR18 DSK EDGE GAIN
VR8 WHITE CLIP–1
VR9 PROGRAM GAIN–3
VR10 BURST GAIN–1
VR11 SYNC GAIN–1
CT1 FREQUENCY RESPONSE-1
1
2
3
4
5

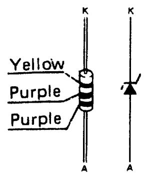
2SC828-QR



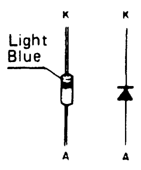
2SA1254-BC
2SB641-RS
2SC2377CD
2SD636-RS
2SD639RS



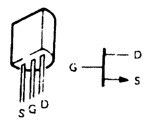
MA4075L


K
K
Yellow
Purple
Purple
A
A

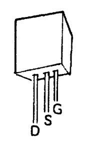
MA27WA


K
K
K
Light Blue
A
A

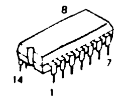
2SK34-CD



2SK19-Y

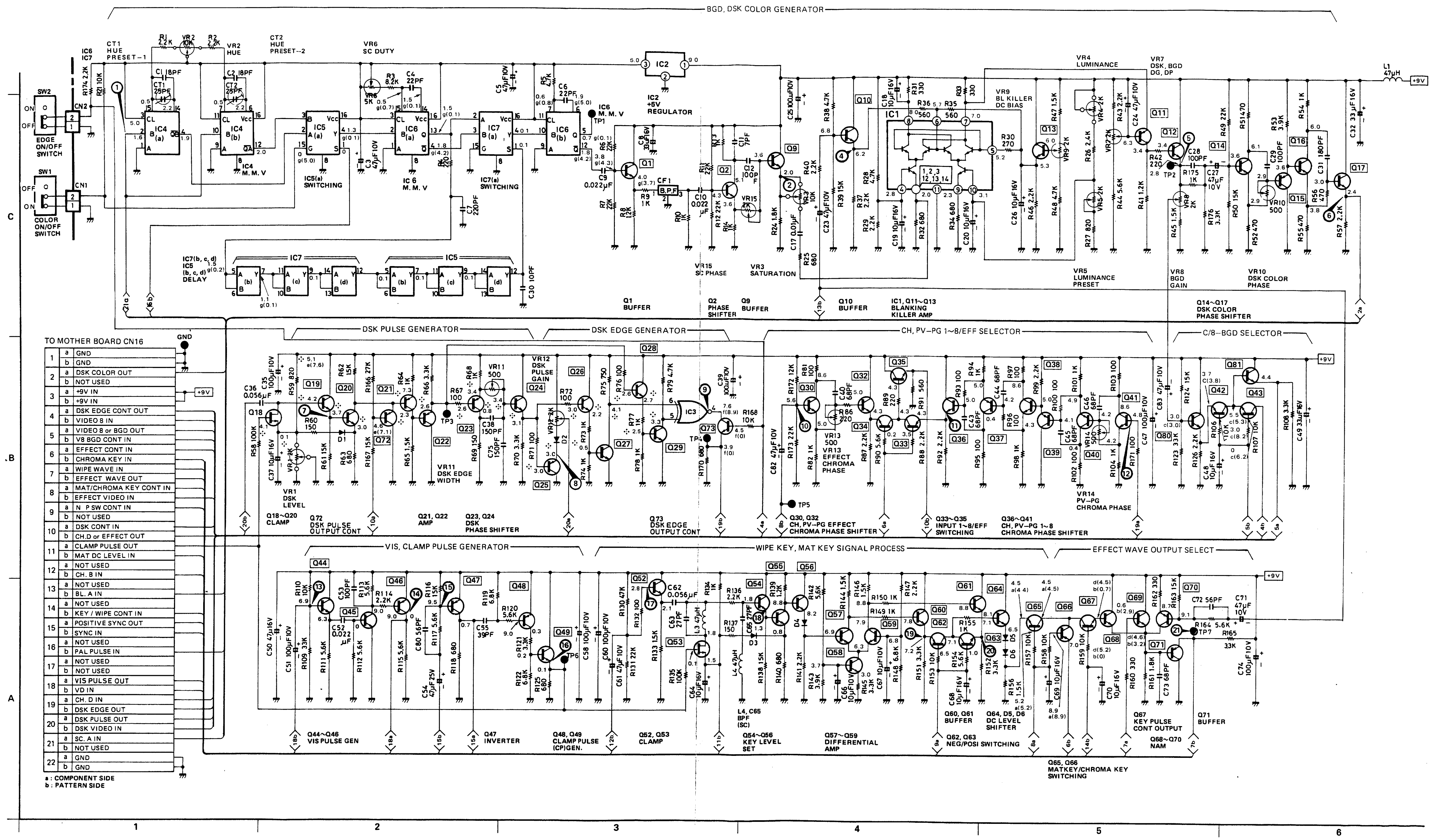


AN610P



IC1	AN610P	A3	Q16	2SC2377CD	A4	Q34	2SD636-RS	B4	Q54	2SD636-RS	C4
IC2	AN610P	B2	Q17	2SD636-RS	A5	Q35	2SD636-RS	B4	Q55	2SA1254-BC	C4
IC3	AN610P	C3	Q18	2SD639RS	A5	Q36	2SD636-RS	B4	Q56	2SA1254-BC	C4
Q1	2SA1254-BC	A1	Q19	2SD639RS	A5	Q38	2SD636-RS	B5	Q57	2SD636-RS	C4
Q2	2SD636-RS	A1	Q20	2SK34-CD	B1	Q39	2SC2377CD	C1	Q58	2SA1254-BC	C4
Q3	2SA1254-BC	A1	Q21	2SK19-Y	B1	Q40	2SC2377CD	C1	Q59	2SD636-RS	C4
Q4	2SD636-RS	A2	Q22	2SD636-RS	B2	Q41	2SA1254-BC	C1	Q60	2SC2377CD	C5
Q5	2SC2377CD	A2	Q23	2SD636-RS	B2	Q42	2SA1254-BC	C1	Q61	2SD636-RS	C5
Q6	2SA1254-BC	A2	Q24	2SD636-RS	B3	Q43	2SA1254-BC	C1	Q62	2SD639RS	C5
Q7	2SK34-CD	A2	Q25	2SK19-Y	B2	Q44	2SD636-RS	C2	Q63	2SD639RS	C5
Q8	2SK19-Y	A2	Q26	2SK34-CD	B3	Q45	2SA1254-BC	C2	Q64	2SD636-RS	B5
Q9	2SD636-RS	A2	Q27	2SA1254-BC	B3	Q46	2SD636-RS	C2	Q65	2SD636-RS	B5
Q10	2SD636-RS	A2	Q28	2SD636-RS	B3	Q47	2SC2377CD	C2	Q66	2SA1254-BC	B5
Q11	2SA1254-BC	A3	Q29	2SA1254-BC	B3	Q48	2SA1254-BC	C2	Q67	2SC828-QR	B5
Q12	2SD636-RS	A3	Q30	2SA1254-BC	B3	Q49	2SK34-CD	C2	Q201	2SC828-QR	B4
Q13	2SA1254-BC	A4	Q31	2SD636-RS	B3	Q50	2SK19-Y	C2	D1	MA4075L	A5
Q14	2SA1254-BC	A4	Q32	2SD636-RS	B3	Q51	2SD636-RS	C2	D2	MA4075L	C5
Q15	2SD636-RS	A4	Q33	2SD636-RS	B4	Q52	2SD636-RS	C3	D3	MA27WA	A3
						Q53	2SA1254-BC	C3	D4	MA27WA	C4

SCHEMATIC DIAGRAM OF DSK,BGD BOARD


BGD, DSK COLOR GENERATOR
DSK PULSE GENERATOR
DSK EDGE GENERATOR
CH, PV–PG 1~8/EFF SELECTOR
C/8–BGD SELECTOR
VIS, CLAMP PULSE GENERATOR
WIPE KEY, MAT KEY SIGNAL PROCESS
EFFECT WAVE OUTPUT SELECT
SW2 EDGE ON/OFF SWITCH
SW1 COLOR ON/OFF SWITCH
IC2 +5V REGULATOR
VR6 SC DUTY
VR4 LUMINANCE
VR7 DSK, BGD DC, DP
VR9 BL KILLER DC BIAS
VR5 LUMINANCE PRESET
VR8 BGD GAIN
VR10 DSK COLOR PHASE
VR15 SC PHASE
VR3 SATURATION
Q1 BUFFER
Q2 PHASE SHIFTER
Q9 BUFFER
Q10 BUFFER
IC1, Q11~Q13 BLANKING KILLER AMP
Q14~Q17 DSK COLOR PHASE SHIFTER
TO MOTHER BOARD CN16
1 a GND
1 b GND
2 a DSK COLOR OUT
2 b NOT USED
3 a +9V IN
3 b +9V IN
4 a DSK EDGE CONT OUT
4 b VIDEO 8 IN
5 a VIDEO 8 or BGD OUT
5 b V8 BGD CONT IN
6 a EFFECT CONT IN
6 b CHROMA KEY IN
7 a WIPE WAVE IN
7 b EFFECT WAVE OUT
8 a MAT/CHROMA KEY CONT IN
8 b EFFECT VIDEO IN
9 a N P SW CONT IN
9 b NOT USED
10 a DSK CONT IN
10 b CH.D or EFFECT OUT
11 a CLAMP PULSE OUT
11 b MAT DC LEVEL IN
12 a NOT USED
12 b CH. B IN
13 a NOT USED
13 b BL. A IN
14 a NOT USED
14 b KEY / WIPE CONT IN
15 a POSITIVE SYNC OUT
15 b SYNC IN
16 a NOT USED
16 b PAL PULSE IN
17 a NOT USED
17 b NOT USED
18 a VIS PULSE OUT
18 b VD IN
19 a CH. D IN
19 b DSK EDGE OUT
20 a DSK PULSE OUT
20 b DSK VIDEO IN
21 a SC. A IN
21 b NOT USED
22 a GND
22 b GND
a : COMPONENT SIDE
b : PATTERN SIDE
Q18~Q20 CLAMP
Q72 DSK PULSE OUTPUT CONT
Q21, Q22 AMP
Q23, Q24 DSK PHASE SHIFTER
VR1 DSK LEVEL
VR11 DSK EDGE WIDTH
VR12 DSK PULSE GAIN
Q73 DSK EDGE OUTPUT CONT
Q30, Q32 CH, PV–PG EFFECT CHROMA PHASE SHIFTER
VR13 EFFECT CHROMA PHASE
Q33~Q35 INPUT 1~8/EFF SWITCHING
Q36~Q41 CH, PV–PG 1~8 CHROMA PHASE SHIFTER
VR14 PV–PG CHROMA PHASE
Q44~Q46 VIS PULSE GEN
Q47 INVERTER
Q48, Q49 CLAMP PULSE (CP)GEN.
Q52, Q53 CLAMP
L4, C65 BPF (SC)
Q54~Q56 KEY LEVEL SET
Q57~Q59 DIFFERENTIAL AMP
Q60, Q61 BUFFER
Q62, Q63 NEG/POSI SWITCHING
Q64, D5, D6 DC LEVEL SHIFTER
Q65, Q66 MATKEY/CHROMA KEY SWITCHING
Q67 KEY PULSE CONT OUTPUT
Q68~Q70 NAM
Q71 BUFFER
L1 47μH
+9V
C
B
A
1
2
3
4
5
6

Voltages are measured by following conditions

a ( ) : MAT KEY → OFF

b ( ) : WIPE → ON

c ( ) : C/8, BGD SELECTOT → C/8

d ( ) : CHROMA KEY, MAT KEY or WIPE KEY → ON

e ( ) : DSK → ON

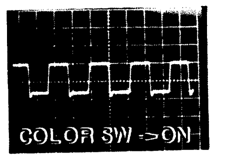
f ( ) : DSK EDGE SW → OFF

g ( ) : COLOR SW → OFF

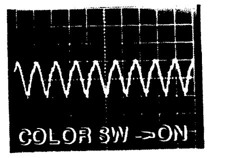
※ : This voltage is changed by VR 1

IC1	AN610P	C4
IC2	AN78N05	D3
IC3	MC14077BP	B3
IC4	YWHD74LS221P	C1
IC5	YWHD74LS157P	C2
IC6	YWHD74LS221P	C2, C3
IC7	YWHD74LS157P	C2
Q1	2SD636-RS	C3
Q2	2SD636-RS	C3
Q9	2SD636-RS	C4
Q10	2SD636-RS	C4
Q11	2SA1254-BC	C5
Q12	2SD636-RS	C5
Q13	2SD636-RS	C5
Q14	2SD636-RS	C6
Q15	2SA1254-BC	C6
Q16	2SD636-RS	C6
Q17	2SD636-RS	C6
Q18	2SK34-CD	B2
Q19	2SD636-RS	B2
Q20	2SC2377CD	B2
Q21	2SA1254-BC	B2
Q22	2SA1254-BC	B2
Q23	2SA1254-BC	B2
Q24	2SC2377CD	B3
Q25	2SA1254-BC	B3
Q26	2SC2377CD	B3
Q27	2SC1216F	B3
Q28	2SC2377CD	B3
Q29	2SC1216F	B3
Q30	2SD636-RS	B4
Q32	2SD636-RS	B4
Q33	2SA1254-BC	B4
Q34	2SC2377CD	B4
Q35	2SC2377CD	B4
Q36	2SD636-RS	B4
Q37	2SA1254-BC	B5
Q38	2SD636-RS	B5
Q39	2SA1254-BC	B5
Q40	2SA1254-BC	B5
Q41	2SD636-RS	B5
Q42	2SA1254-BC	B5
Q43	2SC2377CD	B6
Q44	2SD636-RS	A2
Q45	2SD636-RS	A2
Q46	2SA1254-BC	A2
Q47	2SA1254-BC	A2
Q48	2SA1254-BC	A3
Q49	2SD636-RS	A3
Q52	2SD636-RS	A3
Q53	2SK34-CD	A3
Q54	2SD636-RS	A4
Q55	2SD636-RS	A4
Q56	2SD636-RS	A4
Q57	2SC2377CD	A4
Q58	2SD636-RS	A4
Q59	2SC2377CD	A4
Q60	2SD636-RS	A4
Q61	2SD636-RS	A4
Q62	2SA1254-BC	A4
Q63	2SC2377CD	A4
Q64	2SD636-RS	A5
Q65	2SC2377CD	A5
Q66	2SA1254-BC	A5
Q67	2SC2377CD	A5
Q68	2SD636-RS	A5
Q69	2SD636-RS	A5
Q70	2SA1254-BC	A5
Q71	2SA1254-BC	A5
Q72	2SA1254-BC	B2
Q73	2SD636-RS	B3
Q80	2SD636-RS	B5
Q81	2SC2377CD	B6
D1	MA165	B2
D2	MA27TA	B3
D3	MA165	A4
D4	MA27A	A4
D5	MA26TA	A5
D6	MA26A	A5

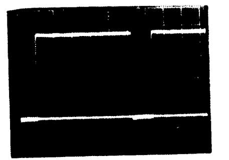
1. 2.0V/DIV 0.2μs/DIV



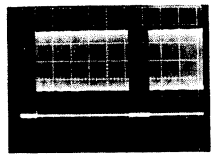
2. 0.5V/DIV 0.2μs/DIV



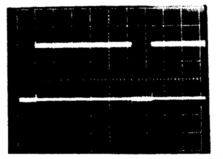
4. 0.5V/DIV 10μs/DIV



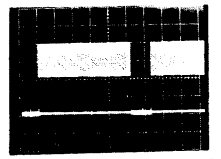
5. 0.2V/DIV 10μs/DIV



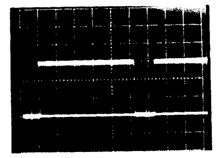
5. 0.2V/DIV 10μs/DIV



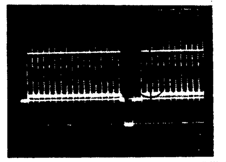
6. 0.2V/DIV 10μs/DIV



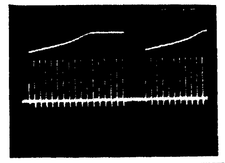
6. 0.2V/DIV 10μs/DIV



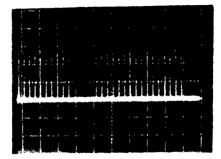
7. 0.2V/DIV 10μs/DIV



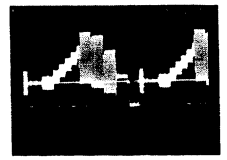
8. 0.1V/DIV 10μs/DIV



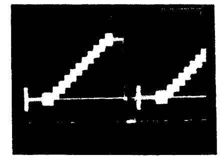
9. 2.0V/DIV 10μs/DIV



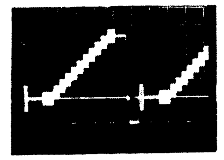
10. 0.2V/DIV 10μs/DIV



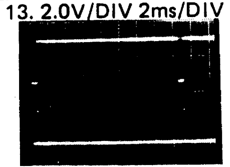
11. 0.2V/DIV 10μs/DIV



12. 0.2V/DIV 10μs/DIV

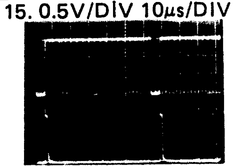


13. 2.0V/DIV 2ms/DIV



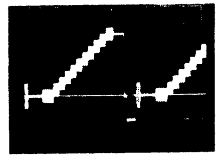
14. 5.0V/DIV 2ms/DIV

15. 0.5V/DIV 10μs/DIV

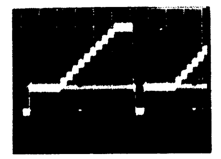


16. 2.0V/DIV 10μs/DIV

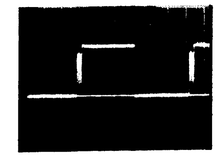
17. 0.2V/DIV 10μs/DIV



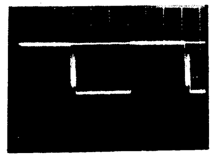
18. 0.2V/DIV 10μs/DIV



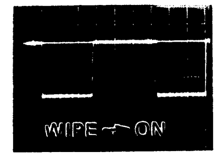
19. 0.5V/DIV 10μs/DIV



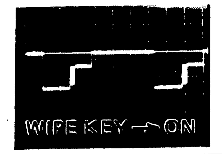
20. 0.5V/DIV 10μs/DIV



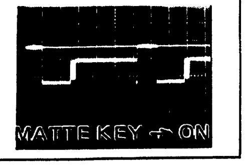
21. 1.0V/DIV 10μs/DIV



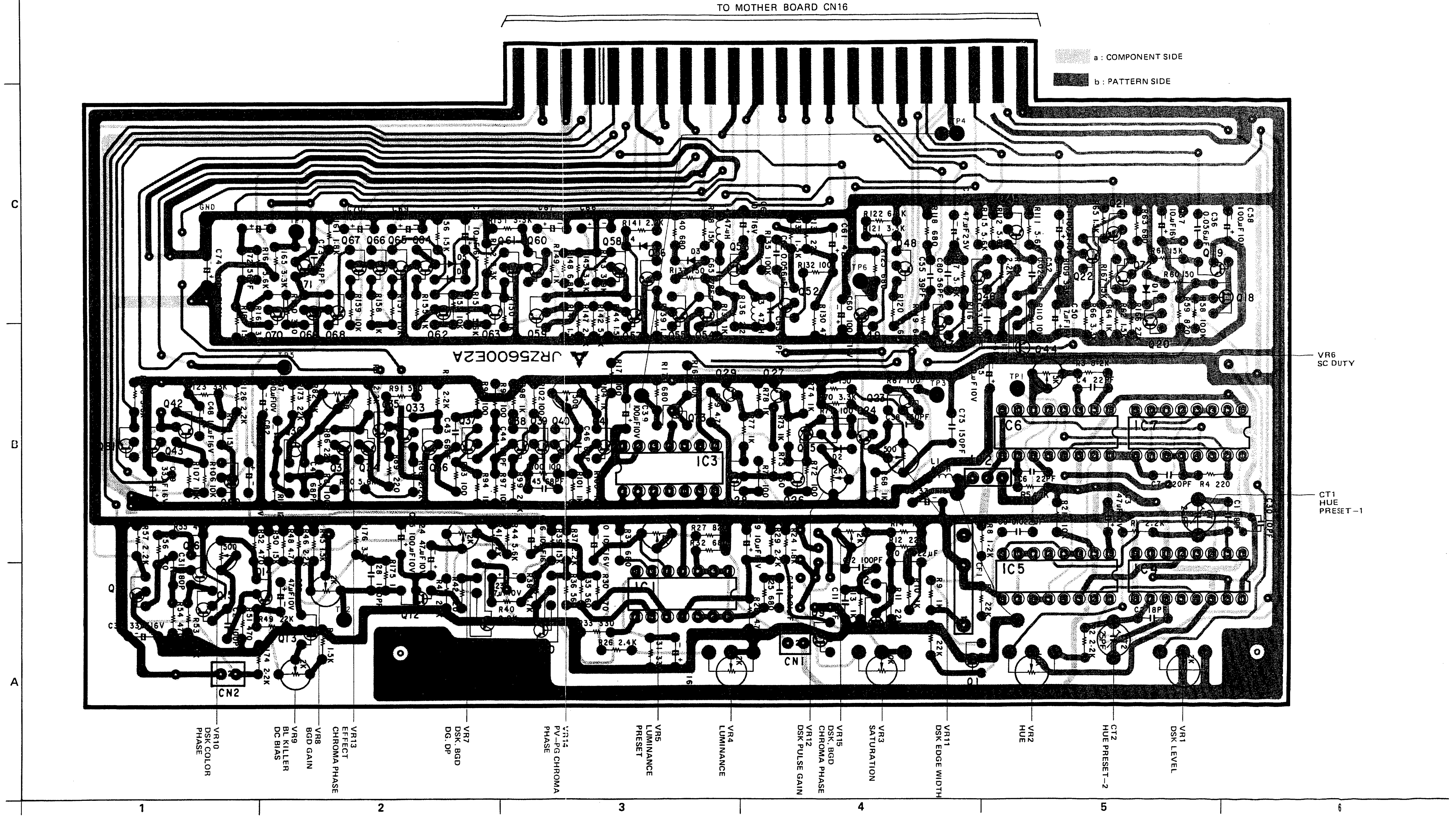
21. 1.0V/DIV 10μs/DIV



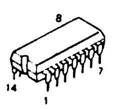
21. 1.0V/DIV 10μs/DIV



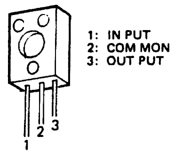
CONDUCTOR VIEW OF DSK,BGD BOARD


TO MOTHER BOARD CN16
a : COMPONENT SIDE
b : PATTERN SIDE
JR25600E2A
IC1
IC3
IC5
IC6
IC7
CN1
CN2
VR6
SC DUTY
CT1
HUE
PRESET−1
VR10
DSK COLOR
PHASE
VR9
BL KILLER
DC BIAS
VR8
BGD GAIN
VR13
EFFECT
CHROMA PHASE
VR7
DSK, BGD
DG, DP
VR14
PV−PG CHROMA
PHASE
VR5
LUMINANCE
PRESET
VR4
LUMINANCE
VR12
DSK PULSE GAIN
VR15
DSK, BGD
CHROMA PHASE
VR3
SATURATION
VR11
DSK EDGE WIDTH
VR2
HUE
CT2
HUE PRESET−2
VR1
DSK LEVEL
C
B
A
1
2
3
4
5
6

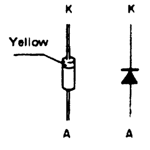
YWHD74LS157P
YWHD74LS221P
AN610P
MC14077BP



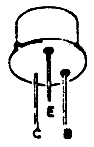
AN78N05


1: IN PUT
2: COM MON
3: OUT PUT
1
2
3

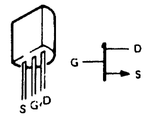
MA27A


Yellow
K
K
A
A

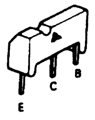
2SC1216F



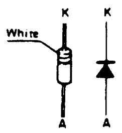
2SK34-CD



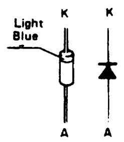
2SA1254-BC
2SC2377CD
2SD636-RS



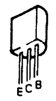
MA165



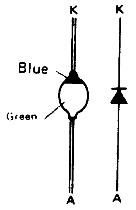
MA27WA


Light Blue
K
K
A
A

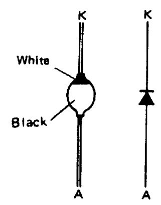
2SA564-QRS
2SC1047



MA27TA
MA26TA

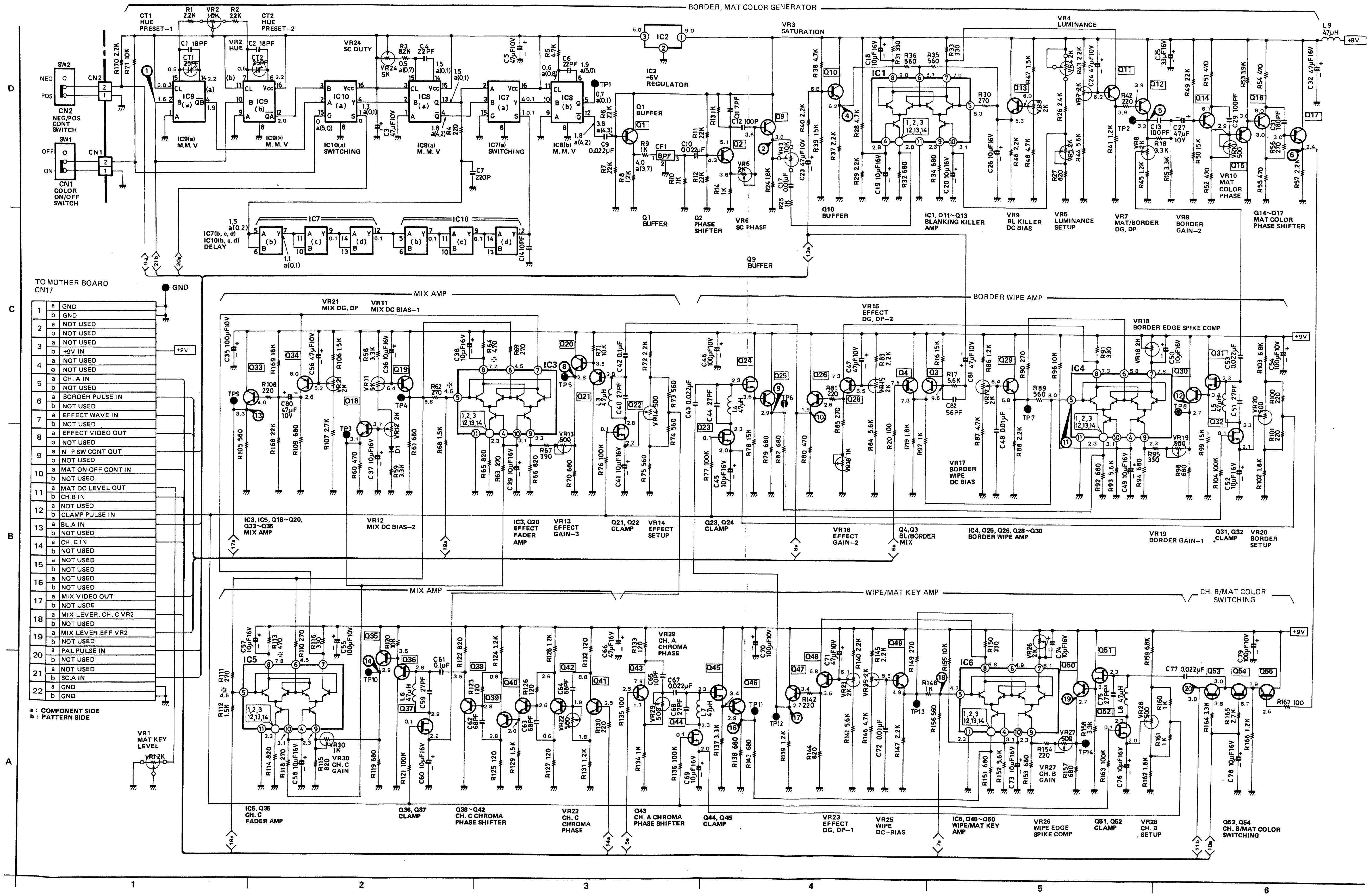

Blue
Green
K
K
A
A

MA26A


White
Black
K
K
A
A

IC1	AN610P	A3	Q20	2SC2377CD	C5	Q40	2SA1254-BC	B3	Q62	2SA1254-BC	C2
IC2	AN78N05	B5	Q21	2SA1254-BC	C5	Q41	2SD636-RS	B3	Q63	2SC2377CD	C2
IC3	MC14077BP	B3	Q22	2SA1254-BC	C5	Q42	2SA1254-BC	B1	Q64	2SD636-RS	C2
IC4	YWHD74LS221P	A5	Q23	2SA1254-BC	B4	Q43	2SC2377CD	B1	Q65	2SC2377CD	C2
IC5	YWHD74LS157P	A5	Q24	2SC2377CD	B4	Q44	2SD636-RS	B5	Q66	2SA1254-BC	C2
IC6	YWHD74LS221P	B5	Q25	2SA1254-BC	B4	Q45	2SD636-RS	C5	Q67	2SC2377CD	C2
IC7	YWHD74LS157P	B5	Q26	2SC2377CD	B4	Q46	2SA1254-BC	C4	Q68	2SD636-RS	C2
Q1	2SD636-RS	A4	Q27	2SC1216F	B4	Q47	2SA1254-BC	C4	Q69	2SD636-RS	C2
Q2	2SD636-RS	A4	Q28	2SC2377CD	B3	Q48	2SA1254-BC	C4	Q70	2SA1254-BC	C2
Q9	2SD636-RS	A4	Q29	2SC1216F	B3	Q49	2SD636-RS	C4	Q71	2SA1254-BC	C2
Q10	2SD636-RS	A3	Q30	2SD636-RS	B2	Q52	2SD636-RS	C4	Q72	2SA1254-BC	C5
Q11	2SA1254-BC	A2	Q32	2SD636-RS	B2	Q53	2SK34-CD	C3	Q73	2SD636-RS	B3
Q12	2SD636-RS	A2	Q33	2SA1254-BC	B2	Q54	2SD636-RS	C3	Q80	2SD636-RS	B1
Q13	2SD636-RS	A2	Q34	2SC2377CD	B2	Q55	2SD636-RS	C3	Q81	2SC2377CD	B1
Q14	2SD636-RS	A2	Q35	2SC2377CD	B2	Q56	2SD636-RS	C3	D1	MA165	C5
Q15	2SA1254-BC	A1	Q36	2SD636-RS	B2	Q57	2SC2377CD	C3	D2	MA27TA	B4
Q16	2SD636-RS	A1	Q37	2SA1254-BC	B2	Q58	2SD636-RS	C3	D3	MA165	C3
Q17	2SD636-RS	A1	Q38	2SD636-RS	B3	Q59	2SC2377CD	C3	D4	MA27A	C3
Q18	2SK34-CD	C6	Q39	2SA1254-BC	B3	Q60	2SD636-RS	C3	D5	MA26TA	C2
Q19	2SD636-RS	C5				Q61	2SD636-RS	C3	D6	MA26A	C2

SCHEMATIC DIAGRAM OF EFFECT,MIX BOARD

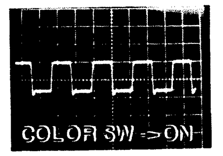

BORDER, MAT COLOR GENERATOR
CT1 HUE PRESET-1
CT2 HUE PRESET-2
VR2 HUE
SW2 NEG/POS CONT SWITCH
SW1 COLOR ON/OFF SWITCH
CN2
CN1
IC9(a) M.M. V
IC9(b) M.M. V
VR24 SC DUTY
IC10(a) SWITCHING
IC8(a) M.M. V
IC7(a) SWITCHING
IC8(b) M.M. V
IC2 +5V REGULATOR
Q1 BUFFER
Q2 PHASE SHIFTER
VR6 SC PHASE
Q9 BUFFER
VR3 SATURATION
Q10 BUFFER
IC1, Q11~Q13 BLANKING KILLER AMP
VR9 BL KILLER DC BIAS
VR4 LUMINANCE
VR5 LUMINANCE SETUP
VR7 MAT/BORDER DG, DP
VR8 BORDER GAIN-2
VR10 MAT COLOR PHASE
Q14~Q17 MAT COLOR PHASE SHIFTER
L9 47µH
+9V
IC7(b, c, d) IC10(b, c, d) DELAY
TO MOTHER BOARD CN17
GND
1 a GND
1 b GND
2 a NOT USED
2 b NOT USED
3 a NOT USED
3 b +9V IN
4 a NOT USED
4 b NOT USED
5 a CH. A IN
5 b NOT USED
6 a BORDER PULSE IN
6 b NOT USED
7 a EFFECT WAVE IN
7 b NOT USED
8 a EFFECT VIDEO OUT
8 b NOT USED
9 a N P SW CONT OUT
9 b NOT USED
10 a MAT ON-OFF CONT IN
10 b NOT USED
11 a MAT DC LEVEL OUT
11 b CH.B IN
12 a NOT USED
12 b CLAMP PULSE IN
13 a BL.A IN
13 b NOT USED
14 a CH. C IN
14 b NOT USED
15 a NOT USED
15 b NOT USED
16 a NOT USED
16 b NOT USED
17 a MIX VIDEO OUT
17 b NOT USDE
18 a MIX LEVER. CH. C VR2
18 b NOT USED
19 a MIX LEVER.EFF VR2
19 b NOT USED
20 a PAL PULSE IN
20 b NOT USED
21 a NOT USED
21 b SC.A IN
22 a GND
22 b GND
a : COMPONENT SIDE
b : PATTERN SIDE
VR1 MAT KEY LEVEL
MIX AMP
VR21 MIX DG, DP
VR11 MIX DC BIAS-1
IC3, IC5, Q18~Q20, Q33~Q35 MIX AMP
VR12 MIX DC BIAS-2
IC3, Q20 EFFECT FADER AMP
VR13 EFFECT GAIN-3
Q21, Q22 CLAMP
VR14 EFFECT SETUP
Q23, Q24 CLAMP
BORDER WIPE AMP
VR15 EFFECT DG, DP-2
VR16 EFFECT GAIN-2
VR17 BORDER WIPE DC BIAS
Q4,Q3 BL/BORDER MIX
IC4, Q25, Q26, Q28~Q30 BORDER WIPE AMP
VR18 BORDER EDGE SPIKE COMP
VR19 BORDER GAIN-1
Q31, Q32 CLAMP
VR20 BORDER SETUP
WIPE/MAT KEY AMP
CH. B/MAT COLOR SWITCHING
VR29 CH. A CHROMA PHASE
VR30 CH. C GAIN
IC5, Q36 CH. C FADER AMP
Q36, Q37 CLAMP
Q38~Q42 CH. C CHROMA PHASE SHIFTER
VR22 CH. C CHROMA PHASE
Q43 CH. A CHROMA PHASE SHIFTER
Q44, Q45 CLAMP
VR23 EFFECT DG, DP-1
VR25 WIPE DC-BIAS
IC6, Q46~Q50 WIPE/MAT KEY AMP
VR26 WIPE EDGE SPIKE COMP
VR27 CH. B GAIN
Q51, Q52 CLAMP
VR28 CH. B SETUP
Q53, Q54 CH. B/MAT COLOR SWITCHING
D
C
B
A
1
2
3
4
5
6

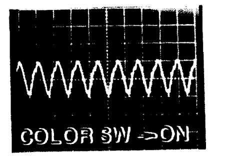
IC1	AN610	D4, D5
IC2	AN78N05	D3
IC3	AN610P	C3
IC4	AN610P	C5
IC5	AN610P	A2
IC6	AN610P	A5
IC7	YWHD74LS157P	C2, D3
IC8	YWHD74LS221P	D2, D3
IC9	YWHD74LS221P	D1, D2
IC10	YWHD74LS157P	C2, C3, D2
Q1	2SD636-RS	D3
Q2	2SD636-RS	D4
Q3	2SA1254-BC	C4
Q4	2SD636-RS	C4
Q9	2SD636-RS	D4
Q10	2SD636-RS	D4
Q11	2SA1254-BC	D5
Q12	2SD636-RS	D5
Q13	2SD636-RS	D5
Q14	2SC2377CD	D6
Q15	2SA1254-BC	D6
Q16	2SC2377CD	D6
Q17	2SD636-RS	D6
Q18	2SD636-RS	C2
Q19	2SD636-RS	C2
Q20	2SD636-RS	C3
Q21	2SA721TU	C3
Q22	2SK34-CD	C3
Q23	2SK34-CD	B4
Q24	2SK19-Y	C4
Q25	2SC2377CD	C4
Q26	2SC2377CD	C4
Q28	2SA1254-BC	C4
Q29	2SD636-RS	C5
Q30	2SC2377CD	C6
Q31	2SK19-Y	C6
Q32	2SK34-CD	C6
Q33	2SC2377CD	C2
Q34	2SA1254-BC	C2
Q35	2SD636-RS	A2
Q36	2SA721TU	A2
Q37	2SK34-CD	A2
Q38	2SA1254-BC	A2
Q39	2SA1254-BC	A3
Q40	2SD636-RS	A3
Q41	2SD636-RS	A3
Q42	2SA1254-BC	A3
Q43	2SC2377CD	A3
Q44	2SK34-CD	A3
Q45	2SK19-Y	A4
Q46	2SC2377CD	A4
Q47	2SD636-RS	A4
Q48	2SA1254-BC	A4
Q49	2SD636-RS	A4
Q50	2SC2377CD	A5
Q51	2SK19-Y	A5
Q52	2SK34-CD	A5
Q53	2SC2377CD	A6
Q54	2SA1254-BC	A6
Q55	2SD636-RS	A6
D1	MA27A	B2

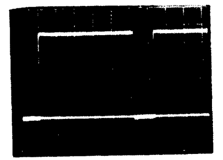
Voltages are measured by following conditions

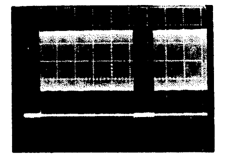
a ( ) : COLOR SW ——————→ OFF

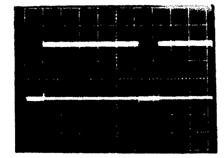
※ : MIX LEVER ——————→ CENTER

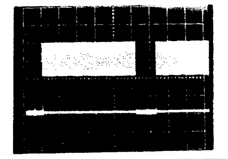

1. 2.0V/DIV 0.2μs/DIV

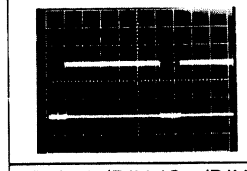

2. 0.5V/DIV 0.2μs/DIV

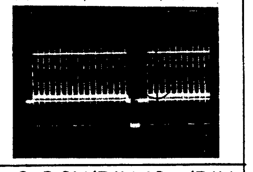

4. 0.5V/DIV 10μs/DIV

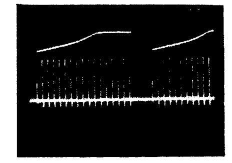

5. 0.2V/DIV 10μs/DIV

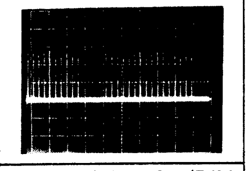

5. 0.2V/DIV 10μs/DIV

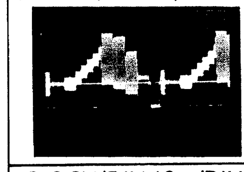

6. 0.2V/DIV 10μs/DIV

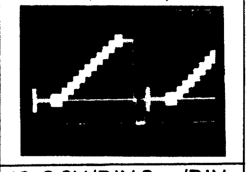

6. 0.2V/DIV 10μs/DIV

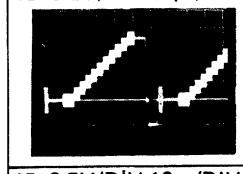

7. 0.2V/DIV 10μs/DIV

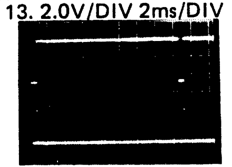

8. 0.1V/DIV 10μs/DIV


9. 2.0V/DIV 10μs/DIV

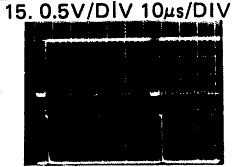

10. 0.2V/DIV 10μs/DIV


11. 0.2V/DIV 10μs/DIV

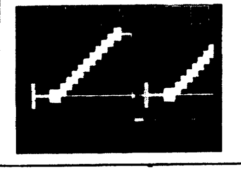

12. 0.2V/DIV 10μs/DIV

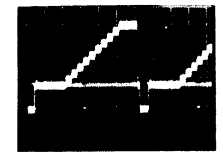

13. 2.0V/DIV 2ms/DIV

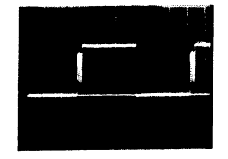
14. 5.0V/DIV 2ms/DIV

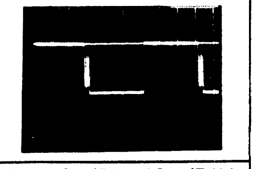

15. 0.5V/DIV 10μs/DIV

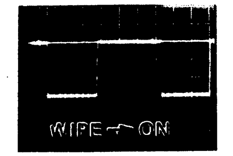
16. 2.0V/DIV 10μs/DIV

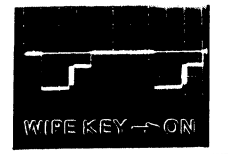

17. 0.2V/DIV 10μs/DIV

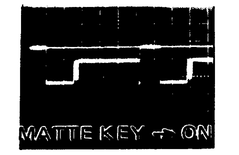

18. 0.2V/DIV 10μs/DIV


19. 0.5V/DIV 10μs/DIV

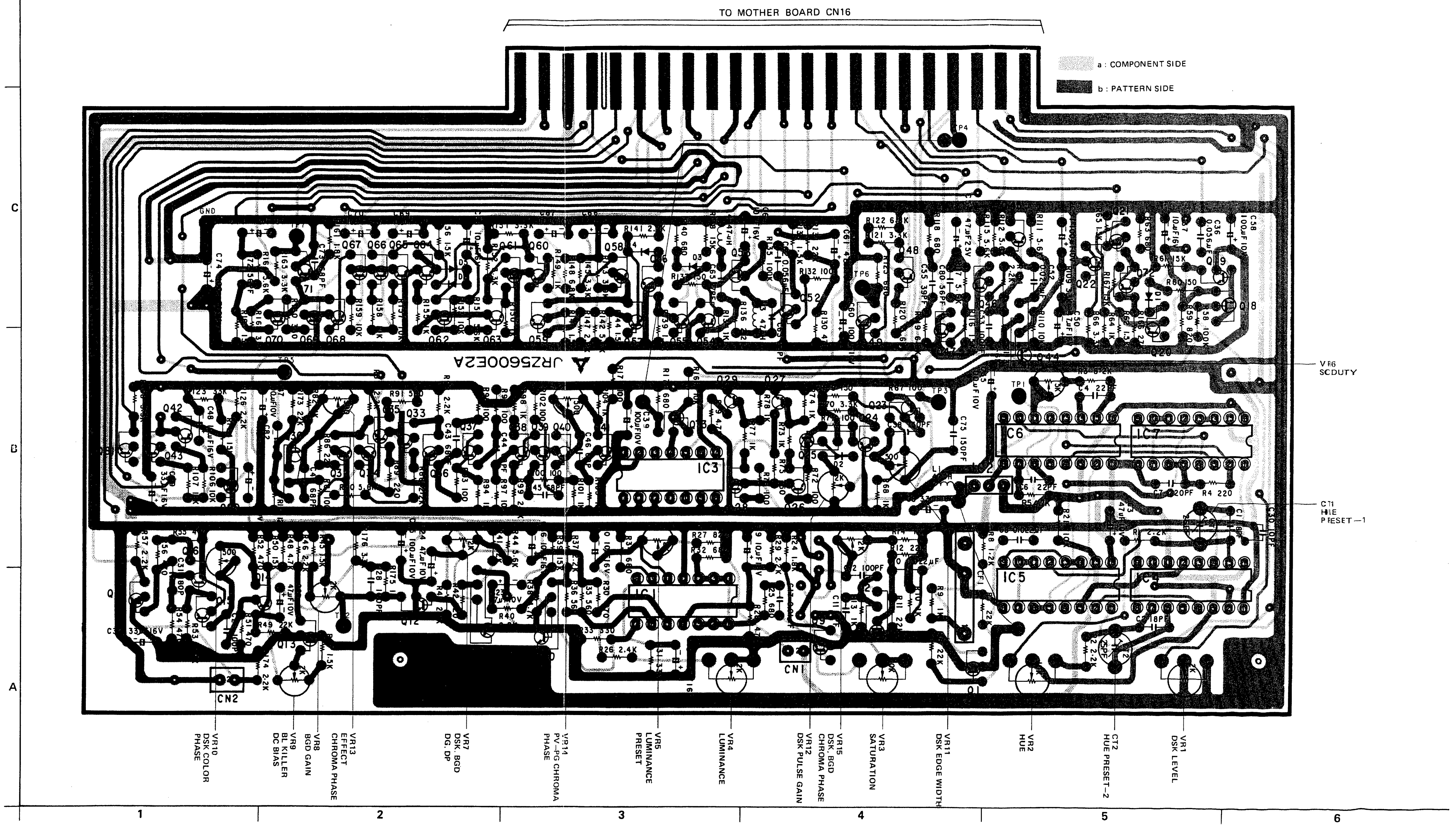

20. 0.5V/DIV 10μs/DIV


21. 1.0V/DIV 10μs/DIV

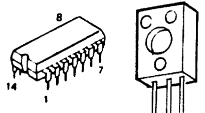

21. 1.0V/DIV 10μs/DIV


21. 1.0V/DIV 10μs/DIV

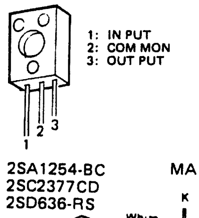
CONDUCTOR VIEW OF DSK,BGD BOARD


TO MOTHER BOARD CN16
a : COMPONENT SIDE
b : PATTERN SIDE
C
B
A
GND
IC1
IC3
IC5
IC6
IC7
CN1
CN2
TP1
VR6
SCDUTY
CT1
HUE
PRESET—1
VR10
DSK COLOR
PHASE
VR9
BL KILLER
DC BIAS
VR8
BGD GAIN
VR13
EFFECT
CHROMA PHASE
VR7
DSK. BGD
DG. DP
VR14
PV—PG CHROMA
PHASE
VR5
LUMINANCE
PRESET
VR4
LUMINANCE
VR12
DSK PULSE GAIN
VR15
DSK. BGD
CHROMA PHASE
VR3
SATURATION
VR11
DSK EDGE WIDTH
VR2
HUE
CT2
HUE PRESET—2
VR1
DSK LEVEL
1
2
3
4
5
6

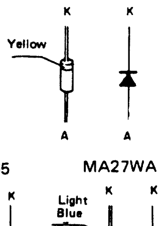
YWHD74LS157P
YWHD74LS221P
AN610P
MC14077BP



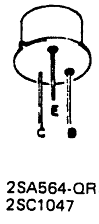
AN78N05


1: IN PUT
2: COM MON
3: OUT PUT
1
2
3

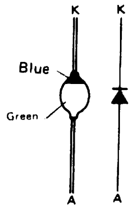
MA27A


Yellow
K
K
A
A

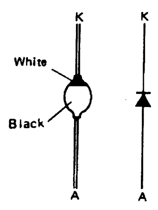
2SC1216F



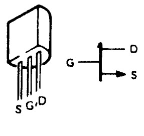
MA27TA
MA26TA


K
K
Blue
Green
A
A

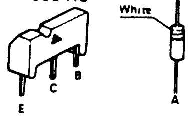
MA26A


K
K
White
Black
A
A

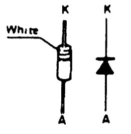
2SK34-CD



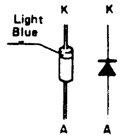
2SA1254-BC
2SC2377CD
2SD636-RS



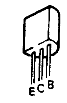
MA165



MA27WA

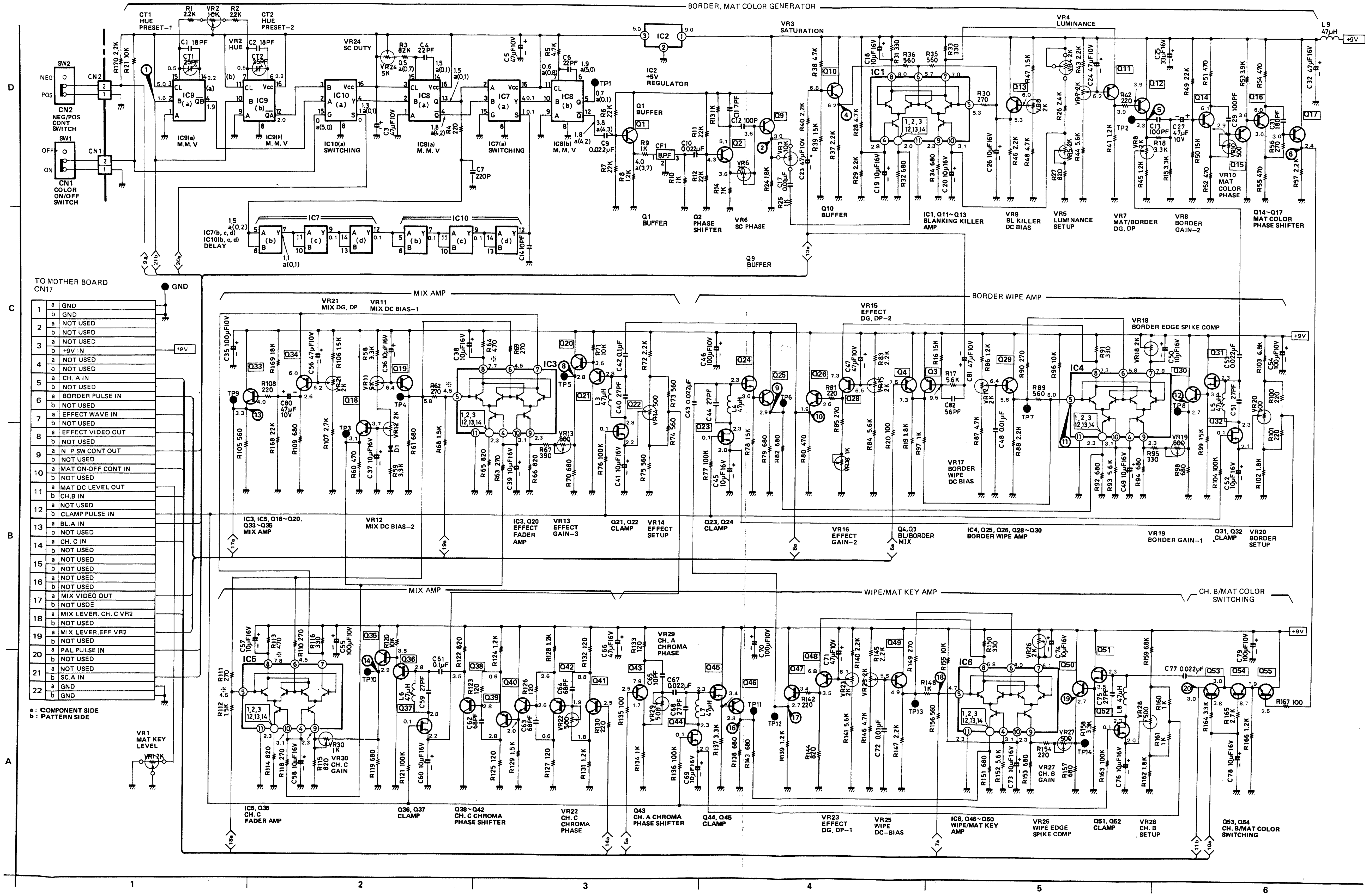

Light
Blue
K
K
A
A

2SA564-QRS
2SC1047



IC1	AN610P	A3	Q20	2SC2377CD	C5	Q40	2SA1254-BC	B3	Q62	2SA1254-BC	C2
IC2	AN78N05	B5	Q21	2SA1254-BC	C5	Q41	2SD636-RS	B3	Q63	2SC2377CD	C2
IC3	MC14077BP	B3	Q22	2SA1254-BC	C5	Q42	2SA1254-BC	B1	Q64	2SD636-RS	C2
IC4	YWHD74LS221P	A5	Q23	2SA1254-BC	B4	Q43	2SC2377CD	B1	Q65	2SC2377CD	C2
IC5	YWHD74LS157P	A5	Q24	2SC2377CD	B4	Q44	2SD636-RS	B5	Q66	2SA1254-BC	C2
IC6	YWHD74LS221P	B5	Q25	2SA1254-BC	B4	Q45	2SD636-RS	C5	Q67	2SC2377CD	C2
IC7	YWHD74LS157P	B5	Q26	2SC2377CD	B4	Q46	2SA1254-BC	C4	Q68	2SD636-RS	C2
Q1	2SD636-RS	A4	Q27	2SC1216F	B4	Q47	2SA1254-BC	C4	Q69	2SD636-RS	C2
Q2	2SD636-RS	A4	Q28	2SC2377CD	B3	Q48	2SA1254-BC	C4	Q70	2SA1254-BC	C2
Q9	2SD636-RS	A4	Q29	2SC1216F	B3	Q49	2SD636-RS	C4	Q71	2SA1254-BC	C2
Q10	2SD636-RS	A3	Q30	2SD636-RS	B2	Q52	2SD636-RS	C4	Q72	2SA1254-BC	C5
Q11	2SA1254-BC	A2	Q32	2SD636-RS	B2	Q53	2SK34-CD	C3	Q73	2SD636-RS	B3
Q12	2SD636-RS	A2	Q33	2SA1254-BC	B2	Q54	2SD636-RS	C3	Q80	2SD636-RS	B1
Q13	2SD636-RS	A2	Q34	2SC2377CD	B2	Q55	2SD636-RS	C3	Q81	2SC2377CD	B1
Q14	2SD636-RS	A2	Q35	2SC2377CD	B2	Q56	2SD636-RS	C3	D1	MA165	C5
Q15	2SA1254-BC	A1	Q36	2SD636-RS	B2	Q57	2SC2377CD	C3	D2	MA27TA	B4
Q16	2SD636-RS	A1	Q37	2SA1254-BC	B2	Q58	2SD636-RS	C3	D3	MA165	C3
Q17	2SD636-RS	A1	Q38	2SD636-RS	B3	Q59	2SC2377CD	C3	D4	MA27A	C3
Q18	2SK34-CD	C6	Q39	2SA1254-BC	B3	Q60	2SD636-RS	C3	D5	MA26TA	C2
Q19	2SD636-RS	C5				Q61	2SD636-RS	C3	D6	MA26A	C2

SCHEMATIC DIAGRAM OF EFFECT, MIX BOARD

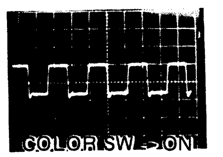

BORDER, MAT COLOR GENERATOR
CT1 HUE PRESET-1
CT2 HUE PRESET-2
VR2 HUE
VR24 SC DUTY
IC2 +5V REGULATOR
VR3 SATURATION
VR4 LUMINANCE
L9 47μH
+9V
SW2 NEG POS
CN2
CN2 NEG/POS CONT SWITCH
SW1 OFF ON
CN1
CN1 COLOR ON/OFF SWITCH
IC9(a) M.M.V
IC9(b) M.M.V
IC10(a) SWITCHING
IC8(a) M.M.V
IC7(a) SWITCHING
IC8(b) M.M.V
Q1 BUFFER
Q2 PHASE SHIFTER
VR6 SC PHASE
Q9 BUFFER
Q10 BUFFER
IC1, Q11~Q13 BLANKING KILLER AMP
VR9 BL KILLER DC BIAS
VR5 LUMINANCE SETUP
VR7 MAT/BORDER DG, DP
VR8 BORDER GAIN-2
VR10 MAT COLOR PHASE
Q14~Q17 MAT COLOR PHASE SHIFTER
IC7(b, c, d) IC10(b, c, d) DELAY
TO MOTHER BOARD CN17
GND
1 a GND
1 b GND
2 a NOT USED
2 b NOT USED
3 a NOT USED
3 b +9V IN
4 a NOT USED
4 b NOT USED
5 a CH. A IN
5 b NOT USED
6 a BORDER PULSE IN
6 b NOT USED
7 a EFFECT WAVE IN
7 b NOT USED
8 a EFFECT VIDEO OUT
8 b NOT USED
9 a N P SW CONT OUT
9 b NOT USED
10 a MAT ON-OFF CONT IN
10 b NOT USED
11 a MAT DC LEVEL OUT
11 b CH.B IN
12 a NOT USED
12 b CLAMP PULSE IN
13 a BL.A IN
13 b NOT USED
14 a CH. C IN
14 b NOT USED
15 a NOT USED
15 b NOT USED
16 a NOT USED
16 b NOT USED
17 a MIX VIDEO OUT
17 b NOT USDE
18 a MIX LEVER. CH. C VR2
18 b NOT USED
19 a MIX LEVER.EFF VR2
19 b NOT USED
20 a PAL PULSE IN
20 b NOT USED
21 a NOT USED
21 b SC.A IN
22 a GND
22 b GND
a : COMPONENT SIDE
b : PATTERN SIDE
VR1 MAT KEY LEVEL
MIX AMP
VR21 MIX DG, DP
VR11 MIX DC BIAS-1
BORDER WIPE AMP
VR15 EFFECT DG, DP-2
VR18 BORDER EDGE SPIKE COMP
IC3, IC5, Q18~Q20, Q33~Q35 MIX AMP
VR12 MIX DC BIAS-2
IC3, Q20 EFFECT FADER AMP
VR13 EFFECT GAIN-3
Q21, Q22 CLAMP
VR14 EFFECT SETUP
Q23, Q24 CLAMP
VR16 EFFECT GAIN-2
Q4, Q3 BL/BORDER MIX
VR17 BORDER WIPE DC BIAS
IC4, Q25, Q26, Q28~Q30 BORDER WIPE AMP
VR19 BORDER GAIN-1
Q31, Q32 CLAMP
VR20 BORDER SETUP
MIX AMP
WIPE/MAT KEY AMP
CH. B/MAT COLOR SWITCHING
VR30 CH. C GAIN
VR29 CH. A CHROMA PHASE
IC5, Q36 CH. C FADER AMP
Q36, Q37 CLAMP
Q38~Q42 CH. C CHROMA PHASE SHIFTER
VR22 CH. C CHROMA PHASE
Q43 CH. A CHROMA PHASE SHIFTER
Q44, Q45 CLAMP
VR23 EFFECT DG, DP-1
VR25 WIPE DC-BIAS
IC6, Q46~Q50 WIPE/MAT KEY AMP
VR26 WIPE EDGE SPIKE COMP
Q51, Q52 CLAMP
VR27 CH. B GAIN
VR28 CH. B SETUP
Q53, Q54 CH. B/MAT COLOR SWITCHING
A
B
C
D
1
2
3
4
5
6

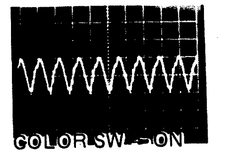
IC1	AN610	D4, D5
IC2	AN78N05	D3
IC3	AN610P	C3
IC4	AN610P	C5
IC5	AN610P	A2
IC6	AN610P	A5
IC7	YWHD74LS157P	C2, D3
IC8	YWHD74LS221P	D2, D3
IC9	YWHD74LS221P	D1, D2
IC10	YWHD74LS157P	C2, C3, D2
Q1	2SD636-RS	D3
Q2	2SD636-RS	D4
Q3	2SA1254-BC	C4
Q4	2SD636-RS	C4
Q9	2SD636-RS	D4
Q10	2SD636-RS	D4
Q11	2SA1254-BC	D5
Q12	2SD636-RS	D5
Q13	2SD636-RS	D5
Q14	2SC2377CD	D6
Q15	2SA1254-BC	D6
Q16	2SC2377CD	D6
Q17	2SD636-RS	D6
Q18	2SD636-RS	C2
Q19	2SD636-RS	C2
Q20	2SD636-RS	C3
Q21	2SA721TU	C3
Q22	2SK34-CD	C3
Q23	2SK34-CD	B4
Q24	2SK19-Y	C4
Q25	2SC2377CD	C4
Q26	2SC2377CD	C4
Q28	2SA1254-BC	C4
Q29	2SD636-RS	C5
Q30	2SC2377CD	C6
Q31	2SK19-Y	C6
Q32	2SK34-CD	C6
Q33	2SC2377CD	C2
Q34	2SA1254-BC	C2
Q35	2SD636-RS	A2
Q36	2SA721TU	A2
Q37	2SK34-CD	A2
Q38	2SA1254-BC	A2
Q39	2SA1254-BC	A3
Q40	2SD636-RS	A3
Q41	2SD636-RS	A3
Q42	2SA1254-BC	A3
Q43	2SC2377CD	A3
Q44	2SK34-CD	A3
Q45	2SK19-Y	A4
Q46	2SC2377CD	A4
Q47	2SD636-RS	A4
Q48	2SA1254-BC	A4
Q49	2SD636-RS	A4
Q50	2SC2377CD	A5
Q51	2SK19-Y	A5
Q52	2SK34-CD	A5
Q53	2SC2377CD	A6
Q54	2SA1254-BC	A6
Q55	2SD636-RS	A6
D1	MA27A	B2

Voltages are measured by following conditions

a ( ) : COLOR SW ————→ OFF

※ : MIX LEVER ————→ CENTER

1. 2.0V/DIV 0.2μs/DIV


2. 0.5V/DIV 0.2μs/DIV


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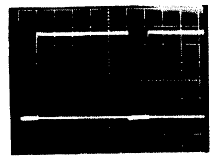

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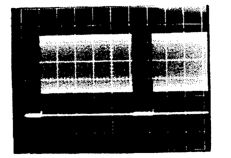

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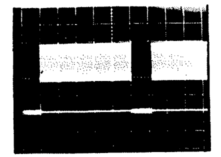
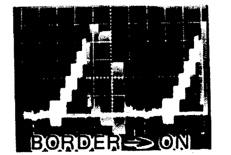
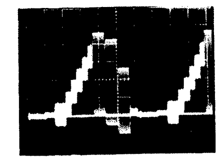


8. 0.1V/DIV 10μs/DIV


9. 0.1V/DIV 10μs/DIV


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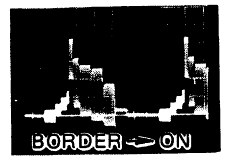
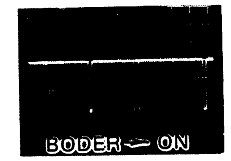
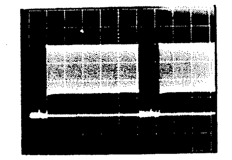
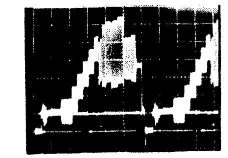


11. 0.1V/DIV 10μs/DIV


12. 0.1V/DIV 10μs/DIV


13. 0.1V/DIV 10μs/DIV


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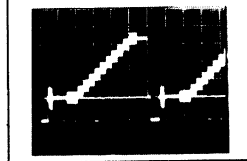

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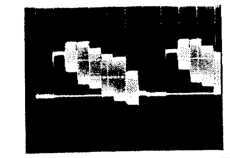
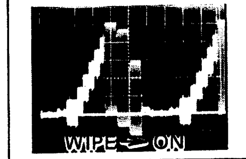
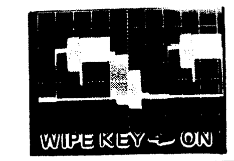


17. 0.1V/DIV 10μs/DIV


17. 0.2V/DIV 10μs/DIV


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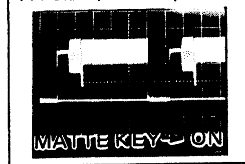
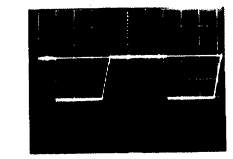


18. 1.0V/DIV 10μs/DIV


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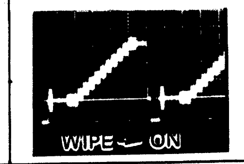

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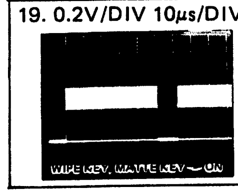

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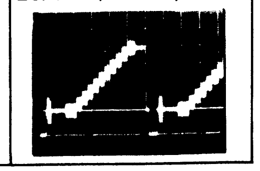
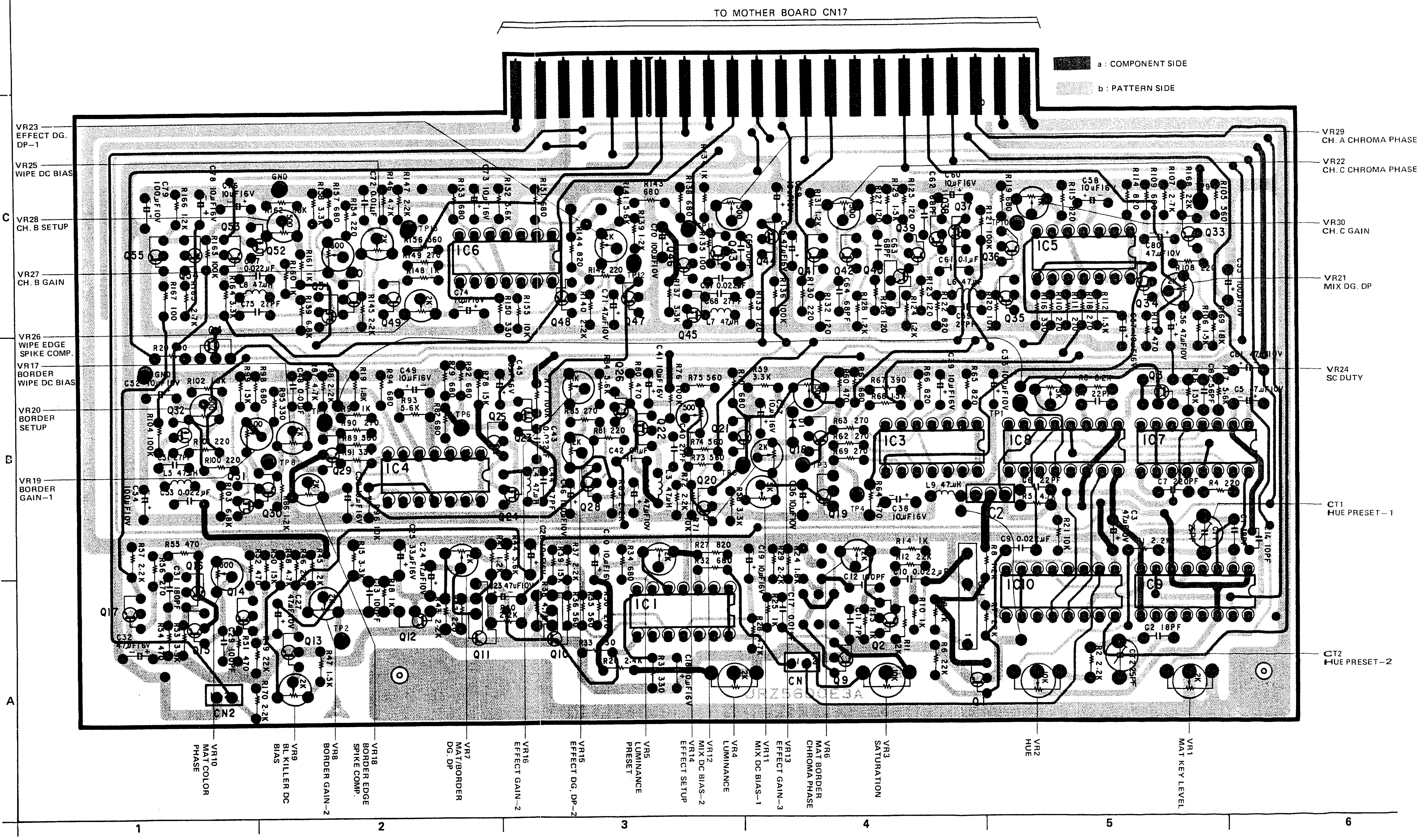


CONDUCTOR VIEW OF EFFECT,MIX BOARD


TO MOTHER BOARD CN17
a : COMPONENT SIDE
b : PATTERN SIDE
C
B
A
VR23 EFFECT DG. DP-1
VR25 WIPE DC BIAS
VR28 CH. B SETUP
VR27 CH. B GAIN
VR26 WIPE EDGE SPIKE COMP.
VR17 BORDER WIPE DC BIAS
VR20 BORDER SETUP
VR19 BORDER GAIN-1
VR29 CH. A CHROMA PHASE
VR22 CH. C CHROMA PHASE
VR30 CH. C GAIN
VR21 MIX DG. DP
VR24 SC DUTY
CT1 HUE PRESET-1
CT2 HUE PRESET-2
VR10 MAT COLOR PHASE
VR9 BL KILLER DC BIAS
VR8 BORDER GAIN-2
VR18 BORDER EDGE SPIKE COMP.
VR7 MAT/BORDER DG. DP
VR16 EFFECT GAIN-2
VR15 EFFECT DG, DP-2
VR5 LUMINANCE PRESET
VR12 MIX DC BIAS-2
VR14 EFFECT SETUP
VR4 LUMINANCE
VR11 MIX DC BIAS-1
VR13 EFFECT GAIN-3
VR6 MAT BORDER CHROMA PHASE
VR3 SATURATION
VR2 HUE
VR1 MAT KEY LEVEL
IC1
IC3
IC4
IC5
IC6
IC7
IC8
IC9
IC10
CN
CN2
GND
TP1
TP2
TP6
TP8
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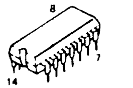
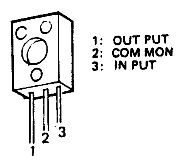
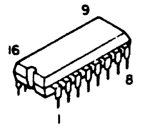
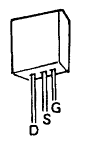
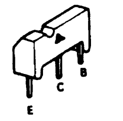
3
4
5
6

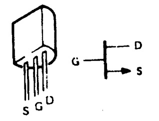
AN610P


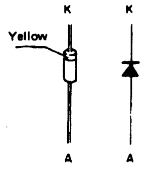
AN78N05

1: OUT PUT
2: COM MON
3: IN PUT
1 2 3

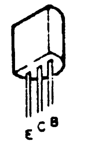
YWHD74LS157P
YWHD74LS221P


2SK19-Y


2SA1254-BC
2SC2377CD
2SD636-RS


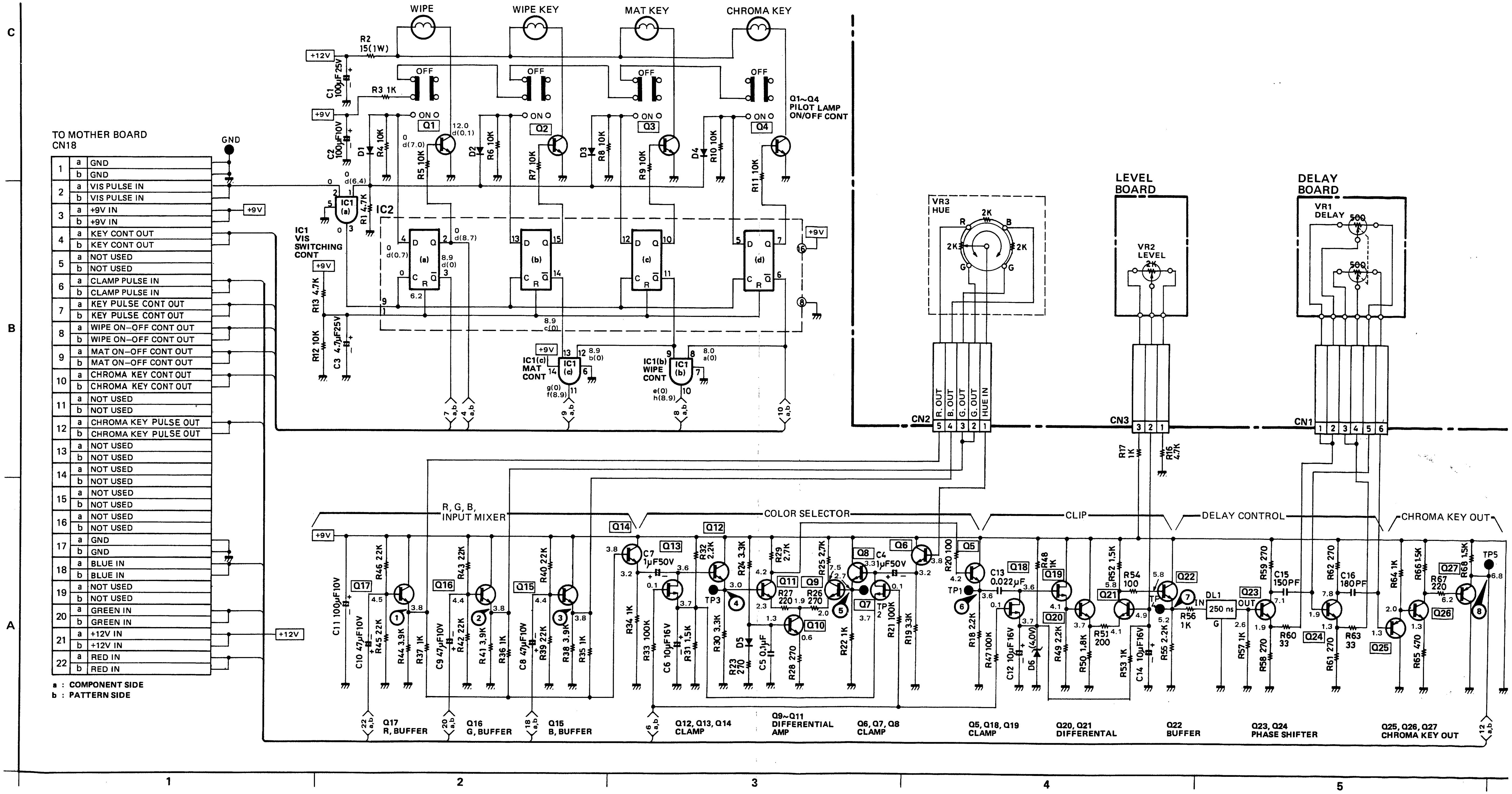
2SK34-CD


MA27A

K
K
Yellow
A
A

2SA721TU


IC1	AN610	A3	Q10	2SD636-RS	A3	Q25	2SC2377CD	B2	Q41	2SD636-RS	C4
IC2	AN78N05	B5	Q11	2SA1254-BC	A2	Q26	2SC2377CD	B3	Q42	2SA1254-BC	C4
IC3	AN610P	B4	Q12	2SD636-RS	A2	Q28	2SA1254-BC	B3	Q43	2SC2377CD	C3
IC4	AN610P	B2	Q13	2SD636-RS	A2	Q29	2SD636-RS	B2	Q44	2SK34-CD	C4
IC5	AN610P	C5	Q14	2SC2377CD	A1	Q30	2SC2377CD	B2	Q45	2SK19-Y	C3
IC6	AN610P	C2, C3	Q15	2SA1254-BC	A1	Q31	2SK19-Y	B1	Q46	2SC2377CD	C3
IC7	YWHD74LS157P	B5	Q16	2SC2377CD	A1	Q32	2SK34-CD	B1	Q47	2SD636-RS	C3
IC8	YWHD74LS221P	B5	Q17	2SD636-RS	A1	Q33	2SC2377CD	C5	Q48	2SA1254-BC	C3
IC9	YWHD74LS221P	A5	Q18	2SD636-RS	B4	Q34	2SA1254-BC	C5	Q49	2SD636-RS	C2
IC10	YWHD74LS157P	A5	Q19	2SD636-RS	B4	Q35	2SD636-RS	C5	Q50	2SC2377CD	C2
Q1	2SD636-RS	A4	Q20	2SD636-RS	B3	Q36	2SA721TU	C5	Q51	2SK19-Y	C2
Q2	2SD636-RS	A4	Q21	2SA721TU	B3	Q37	2SK34-CD	C4	Q52	2SK34-CD	C2
Q3	2SA1254-BC	B5	Q22	2SK34-CD	B3	Q38	2SA1254-BC	C4	Q53	2SC2377CD	C1
Q4	2SD636-RS	B1	Q23	2SK34-CD	B3	Q39	2SA1254-BC	C4	Q54	2SA1254-BC	C1
Q9	2SD636-RS	A4	Q24	2SK19-Y	B3	Q40	2SD636-RS	C4	Q55	2SD636-RS	C1
									D1	MA27A	B4

SCHEMATIC DIAGRAM OF CHROMA KEY BOARD/DELAY BOARD/LEVEL BOARD



WIPE
WIPE KEY
MAT KEY
CHROMA KEY
+12V
R2 15(1W)
C1 100μF25V
R3 1K
OFF
ON
+9V
C2 100μF10V
Q1~Q4 PILOT LAMP ON/OFF CONT
Q1
Q2
Q3
Q4
D1
R4 10K
R5 10K
D2
R6 10K
R7 10K
D3
R8 10K
R9 10K
D4
R10 10K
R11 10K
TO MOTHER BOARD CN18
GND
1 a GND
b GND
2 a VIS PULSE IN
b VIS PULSE IN
3 a +9V IN
b +9V IN
4 a KEY CONT OUT
b KEY CONT OUT
5 a NOT USED
b NOT USED
6 a CLAMP PULSE IN
b CLAMP PULSE IN
7 a KEY PULSE CONT OUT
b KEY PULSE CONT OUT
8 a WIPE ON–OFF CONT OUT
b WIPE ON–OFF CONT OUT
9 a MAT ON–OFF CONT OUT
b MAT ON–OFF CONT OUT
10 a CHROMA KEY CONT OUT
b CHROMA KEY CONT OUT
11 a NOT USED
b NOT USED
12 a CHROMA KEY PULSE OUT
b CHROMA KEY PULSE OUT
13 a NOT USED
b NOT USED
14 a NOT USED
b NOT USED
15 a NOT USED
b NOT USED
16 a NOT USED
b NOT USED
17 a GND
b GND
18 a BLUE IN
b BLUE IN
19 a NOT USED
b NOT USED
20 a GREEN IN
b GREEN IN
21 a +12V IN
b +12V IN
22 a RED IN
b RED IN
a : COMPONENT SIDE
b : PATTERN SIDE
IC1 VIS SWITCHING CONT
IC2
R1 4.7K
R13 4.7K
R12 10K
C3 4.7μF25V
IC1(c) MAT CONT
IC1(b) WIPE CONT
(a)
(b)
(c)
(d)
VR3 HUE
VR2 LEVEL
VR1 DELAY
LEVEL BOARD
DELAY BOARD
CN1
CN2
CN3
R. OUT
B. OUT
G. OUT
G. OUT
HUE IN
R17 1K
R16 4.7K
R, G, B, INPUT MIXER
COLOR SELECTOR
CLIP
DELAY CONTROL
CHROMA KEY OUT
DL1 250 ns
IN
OUT
TP1
TP2
TP3
TP5
Q5 – Q27
C7 1μF50V
C4 3.3 1μF50V
C13 0.022μF
C15 150PF
C16 180PF
Q17 R, BUFFER
Q16 G, BUFFER
Q15 B, BUFFER
Q12, Q13, Q14 CLAMP
Q9~Q11 DIFFERENTIAL AMP
Q6, Q7, Q8 CLAMP
Q5, Q18, Q19 CLAMP
Q20, Q21 DIFFERENTAL
Q22 BUFFER
Q23, Q24 PHASE SHIFTER
Q25, Q26, Q27 CHROMA KEY OUT
C
B
A
1
2
3
4
5

Voltages are measured by following conditions

a( ) : [illegible] ——→ ON

b( ) : MAT KEY ——→ ON

c( ) : WIPE KEY ——→ ON

d( ) : WIPE ——→ ON

e( ) : MAT KEY or [illegible] ——→ ON

f( ) : [illegible] or WIPE ——→ ON

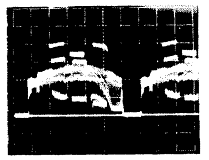
g( ) : MAT KEY or WIPE KEY ——→ ON

h( ) : WIPE KEY or WIPE ——→ ON

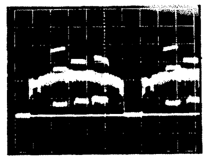
IC1	HD14081BP	B2, B3	Q11	2SC2377CD	A3	Q23	2SD636-RS	A5
IC2	YWHD14175BP	B2, B3	Q12	2SD636-RS	A3	Q24	2SD636-RS	A5
Q1	2SD639RS	C2	Q13	2SK34-CD	A3	Q25	2SB641-RS	A5
Q2	2SD639RS	C2	Q14	2SD636-RS	A3	Q26	2SD636-RS	A5
Q3	2SD639RS	C3	Q15	2SD636-RS	A2	Q27	2SB641-RS	A5
Q4	2SD639RS	C3	Q16	2SD636-RS	A2	D1	MA165	C2
Q5	2SD636-RS	A4	Q17	2SD636-RS	A2	D2	MA165	C2
Q6	2SD636-RS	A4	Q18	2SK34-CD	A4	D3	MA165	C2
Q7	2SK34-CD	A3	Q19	2SK19-Y	A4	D4	MA165	C3
Q8	2SD636-RS	A3	Q20	2SC2377CD	A4	D5	MA165	A3
Q9	2SC2377CD	A3	Q21	2SC2377CD	A4	D6	YUDYZ040B	A4
Q10	2SD636-RS	A3	Q22	2SD636-RS	A4			

CONDUCTOR VIEW OF CHROMA KEY BOARD/DELAY BOARD/LEVEL BOARD

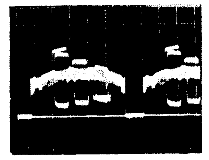
1. 0.2V/DIV 10μs/DIV



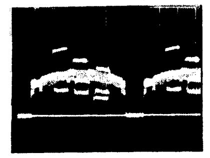
2. 0.2V/DIV 10μs/DIV



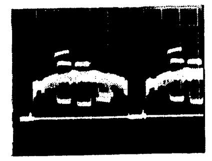
3. 0.2V/DIV 10μs/DIV



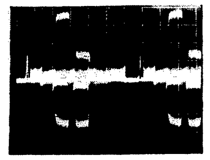
4. 0.2V/DIV 10μs/DIV



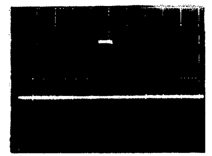
5. 0.2V/DIV 10μs/DIV



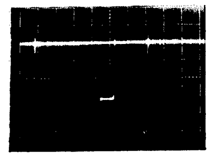
6. 0.2V/DIV 10μs/DIV

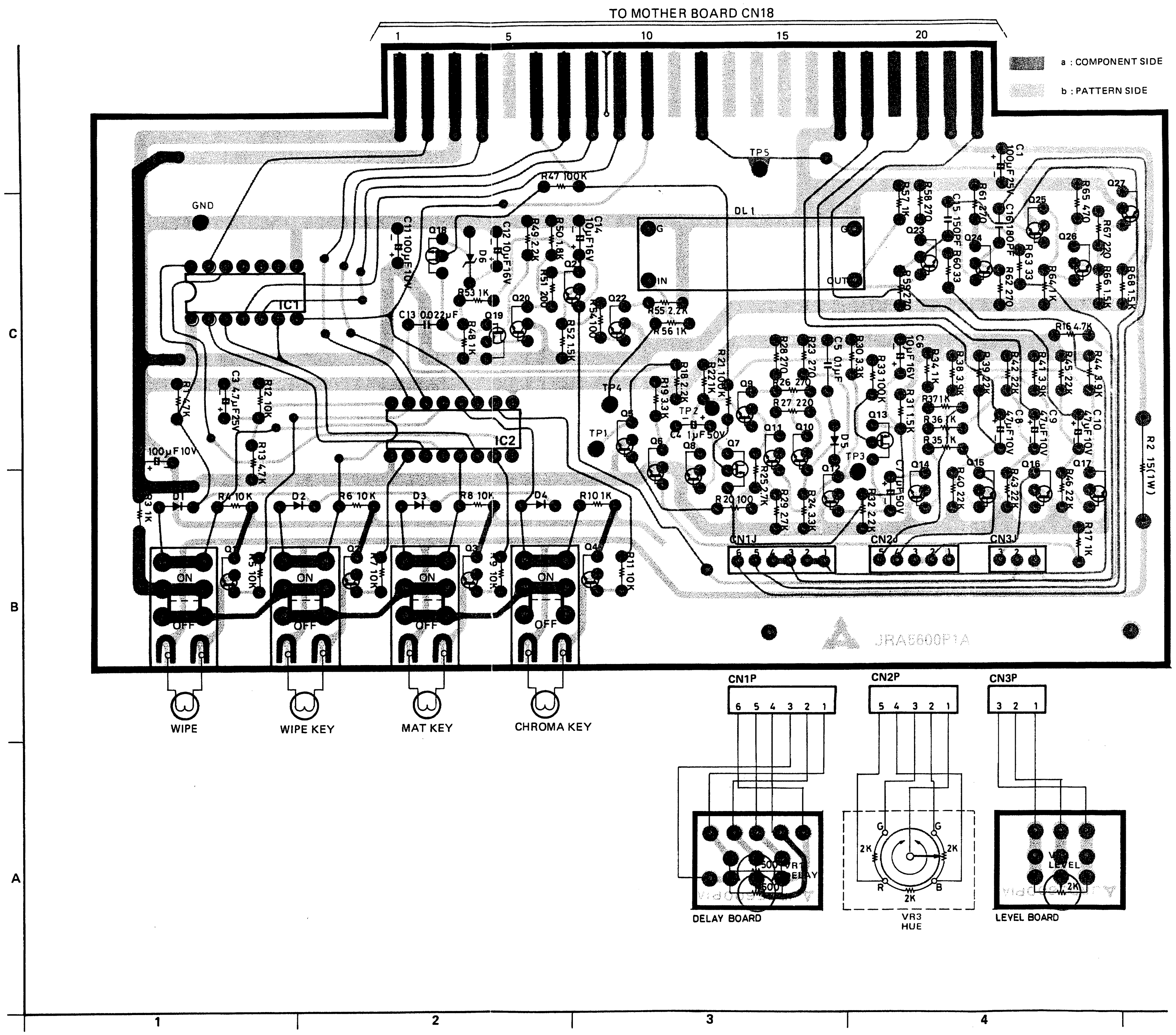


7. 1.0V/DIV 10μs/DIV

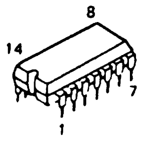


8. 1.0V/DIV 10μs/DIV

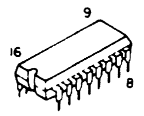




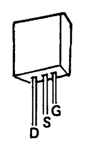
HD14081BP



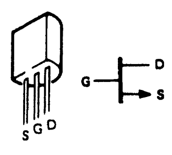
HD14175BP



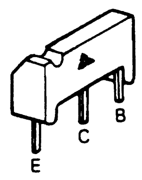
2SK19-Y



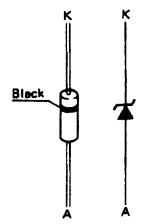
2SK34-CD



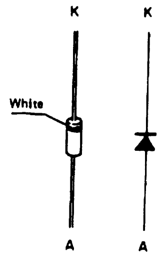
2SB641-RS
2SC2377CD
2SD636-RS
2SD639RS



YUDYZ040B

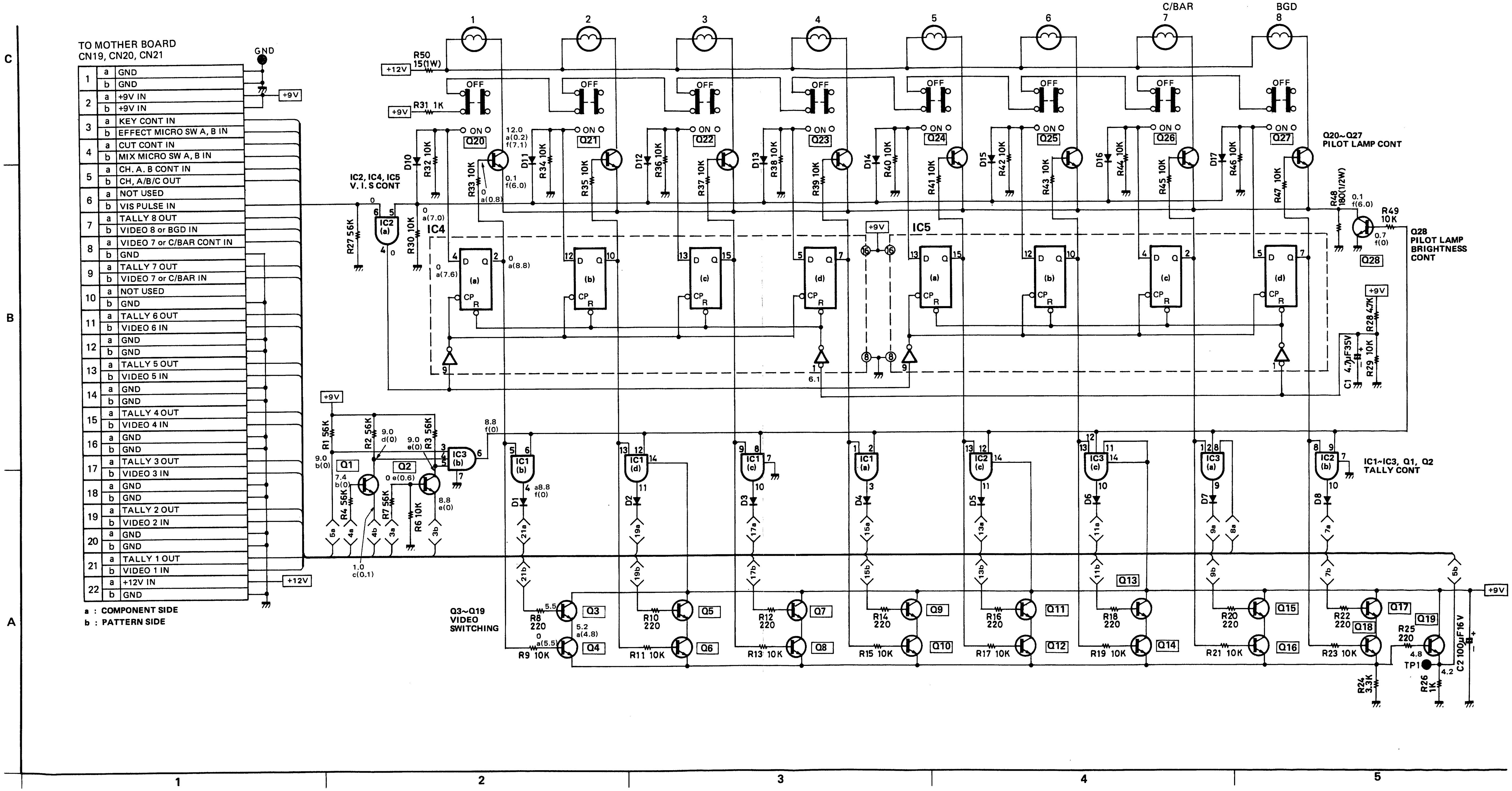


MA165



IC1	HD14081BP	C1	Q11	2SC2377CD	C3	Q23	2SD636-RS	C4
IC2	YWHD14175BP	C2	Q12	2SD636-RS	B3	Q24	2SD636-RS	C4
Q1	2SD639RS	B1	Q13	2SK34-CD	C4	Q25	2SB641-RS	C4
Q2	2SD639RS	B2	Q14	2SD636-RS	B4	Q26	2SD636-RS	C4
Q3	2SD639RS	B2	Q15	2SD636-RS	B4	Q27	2SB641-RS	C4
Q4	2SD639RS	B3	Q16	2SD636-RS	B4	D1	MA165	B1
Q5	2SD636-RS	C3	Q17	2SD636-RS	B4	D2	MA165	B1
Q6	2SD636-RS	B3	Q18	2SK34-CD	C2	D3	MA165	B2
Q7	2SK34-CD	B3	Q19	2SK19-Y	C2	D4	MA165	B2
Q8	2SD636-RS	B3	Q20	2SC2377CD	C2	D5	MA165	C3
Q9	2SC2377CD	C3	Q21	2SC2377CD	C2	D6	YUDYZ040B	C2
Q10	2SD636-RS	C3	Q22	2SD636-RS	C3			

SCHEMATIC DIAGRAM OF INPUT A/B/C BOARD


C
B
A
1
2
3
4
5
TO MOTHER BOARD
CN19, CN20, CN21
GND
1 a GND
b GND
2 a +9V IN
b +9V IN
3 a KEY CONT IN
b EFFECT MICRO SW A, B IN
4 a CUT CONT IN
b MIX MICRO SW A, B IN
5 a CH. A. B CONT IN
b CH, A/B/C OUT
6 a NOT USED
b VIS PULSE IN
7 a TALLY 8 OUT
b VIDEO 8 or BGD IN
8 a VIDEO 7 or C/BAR CONT IN
b GND
9 a TALLY 7 OUT
b VIDEO 7 or C/BAR IN
10 a NOT USED
b GND
11 a TALLY 6 OUT
b VIDEO 6 IN
12 a GND
b GND
13 a TALLY 5 OUT
b VIDEO 5 IN
14 a GND
b GND
15 a TALLY 4 OUT
b VIDEO 4 IN
16 a GND
b GND
17 a TALLY 3 OUT
b VIDEO 3 IN
18 a GND
b GND
19 a TALLY 2 OUT
b VIDEO 2 IN
20 a GND
b GND
21 a TALLY 1 OUT
b VIDEO 1 IN
22 a +12V IN
b GND
a : COMPONENT SIDE
b : PATTERN SIDE
+9V
+12V
R50 15(1W)
R31 1K
1
2
3
4
5
6
C/BAR 7
BGD 8
OFF
ON
Q20
Q21
Q22
Q23
Q24
Q25
Q26
Q27
Q20~Q27 PILOT LAMP CONT
IC2, IC4, IC5 V. I. S CONT
IC2 (a)
IC4
IC5
R27 56K
R30 10K
D10
R32 10K
R33 10K
D11
R34 10K
R35 10K
D12
R36 10K
R37 10K
D13
R38 10K
R39 10K
D14
R40 10K
R41 10K
D15
R42 10K
R43 10K
D16
R44 10K
R45 10K
D17
R46 10K
R47 10K
R48 180(1/2W)
R49 10K
Q28
Q28 PILOT LAMP BRIGHTNESS CONT
R28 4.7K
R29 10K
C1 4.7μF35V
12.0
a(0.2)
f(7.1)
0.1
f(6.0)
a(0.8)
a(7.0)
a(7.6)
a(8.8)
0.7
f(0)
6.1
D Q
CP R
(a)
(b)
(c)
(d)
R1 56K
R2 56K
R3 56K
R4 56K
R5 56K
R7 56K
R6 10K
Q1
Q2
IC3 (b)
9.0 b(0)
7.4 b(0)
9.0 d(0)
9.0 e(0)
0 e(0.6)
8.8 f(0)
8.8 e(0)
1.0 c(0.1)
IC1 (b)
IC1 (d)
IC1 (c)
IC1 (a)
IC2 (c)
IC3 (c)
IC3 (a)
IC2 (b)
IC1~IC3, Q1, Q2 TALLY CONT
D1
D2
D3
D4
D5
D6
D7
D8
Q3~Q19 VIDEO SWITCHING
Q3
Q4
Q5
Q6
Q7
Q8
Q9
Q10
Q11
Q12
Q13
Q14
Q15
Q16
Q17
Q18
Q19
R8 220
R9 10K
R10 220
R11 10K
R12 220
R13 10K
R14 220
R15 10K
R16 220
R17 10K
R18 220
R19 10K
R20 220
R21 10K
R22 220
R23 10K
R25 220
R24 3.3K
R26 1K
C2 100μF16V
TP1
4.8
4.2
5.5
5.2
a(4.8)
a(5.5)

Voltages are measured by following conditions

a( ) : 1 ——→ ON

b( ) : CUT ——→ ON

c( ) : (CUT → ON) or (MIX LEVER → BOTTOM)

d( ) : (CUT → OFF) and (MIX LEVER → BOTTOM)

e( ) : (WIPE → ON) and (WIPE LEVER → BOTTOM)

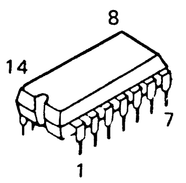
f( ) : (CUT → ON), (CUT → OFF and MIX LEVER → BOTTOM)

or (WIPE → ON and WIPE LEVER → BOTTOM)

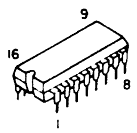
IC1	HD14081BP	B2, B3
IC2	HD14081BP	B4, B5
IC3	HD14073BP	B2, B4
IC4	HD14175BP	B1, B2
IC5	HD14175BP	B4, B5
Q1	2SD636-RS	A2
Q2	2SD636-RS	A2
Q3	2SD636-RS	A2
Q4	2SD636-RS	A2
Q5	2SD636-RS	A3
Q6	2SD636-RS	A3
Q7	2SD636-RS	A3
Q8	2SD636-RS	A3
Q9	2SD636-RS	A3
Q10	2SD636-RS	A3
Q11	2SD636-RS	A4
Q12	2SD636-RS	A4
Q13	2SD636-RS	A4
Q14	2SD636-RS	A4
Q15	2SD636-RS	A5
Q16	2SD636-RS	A5
Q17	2SD636-RS	A5
Q18	2SD636-RS	A5
Q19	2SD636-RS	A5
Q20	2SD639RS	C2
Q21	2SD639RS	C2
Q22	2SD639RS	C3
Q23	2SD639RS	C3
Q24	2SD639RS	C4
Q25	2SD639RS	C4
Q26	2SD639RS	C4
Q27	2SD639RS	C5
Q28	2SD639RS	C5
D1	MA162	A2
D2	MA162	A3
D3	MA162	A3
D4	MA162	A3
D5	MA162	A4
D6	MA162	A4
D7	MA162	A4
D8	MA162	A5
D10	MA162	C2
D11	MA162	C2
D12	MA162	C3
D13	MA162	C3
D14	MA162	C3
D15	MA162	C4
D16	MA162	C4
D17	MA162	C4

CONDUCTOR VIEW OF INPUT A/B/C BOARD

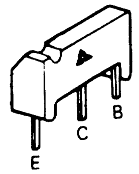
HD14073BP
HD14081BP



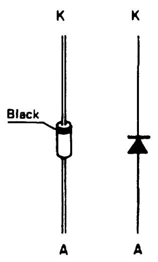
HD14175BP

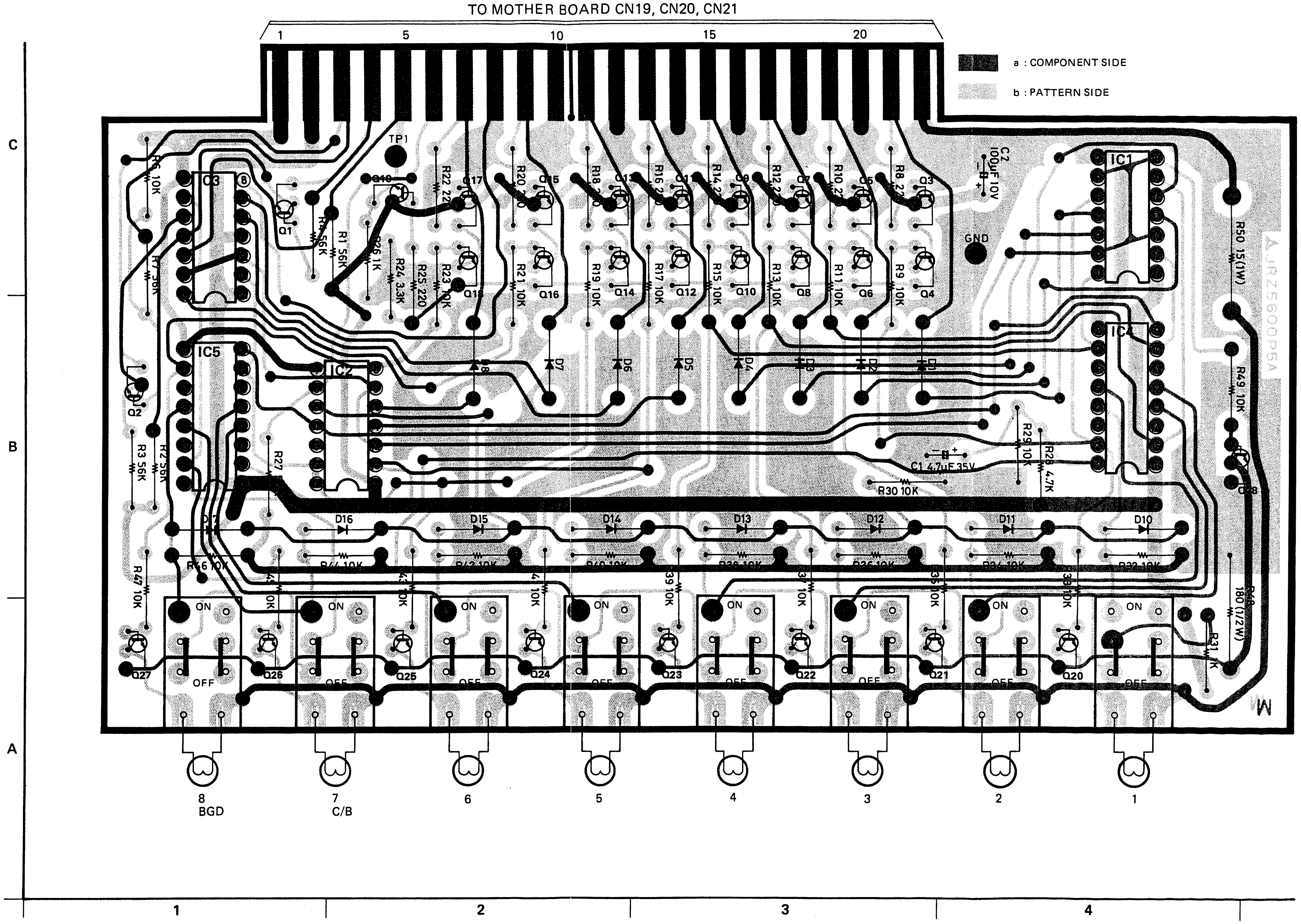


2SD636-RS
2SD639RS



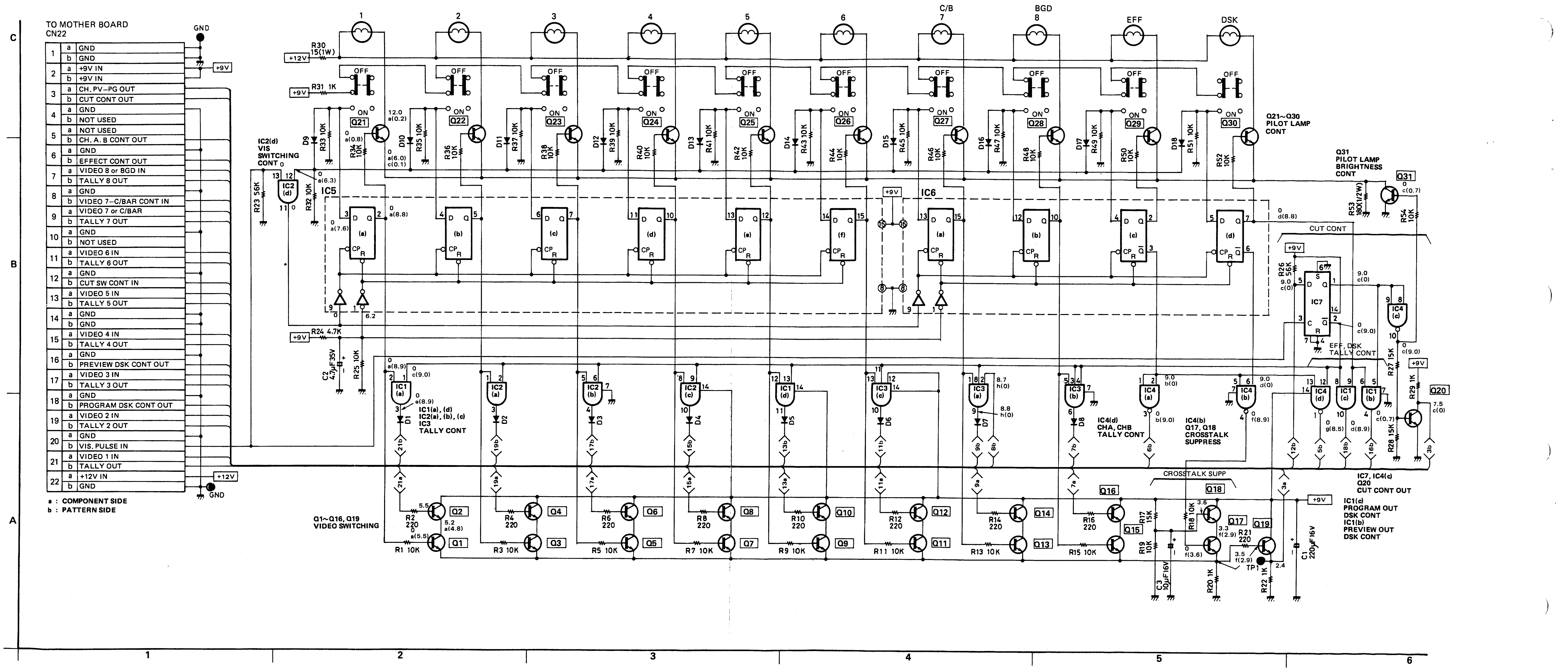
MA162




TO MOTHER BOARD CN19, CN20, CN21
1
5
10
15
20
a : COMPONENT SIDE
b : PATTERN SIDE
C
B
A
1
2
3
4
TP1
GND
IC1
IC2
IC3
IC5
C2 100µF 10V
C1 4.7µF 35V
R50 15(1W)
R49 10K
R48 180 (1/2W)
R31 1K
R29 10K
R28 4.7K
R30 10K
R3 56K
R2 56K
R47 10K
R46 10K
R27
R6 10K
R7 56K
R4 56K
R1 56K
R26 1K
R24 3.3K
R25 220
R23 10K
R22 22
R21 10K
R20 220
R19 10K
R18 220
R17 10K
R16 22
R15 10K
R14 22
R13 10K
R12 22
R11 10K
R10 22
R9 10K
R8 22
R44 10K
R42 10K
R40 10K
R38 10K
R36 10K
R34 10K
R32 10K
R43 10K
R41 10K
R39 10K
R37 10K
R35 10K
R33 10K
Q1
Q2
Q3
Q4
Q5
Q6
Q7
Q8
Q9
Q10
Q11
Q12
Q13
Q14
Q15
Q16
Q17
Q18
Q19
Q20
Q21
Q22
Q23
Q24
Q25
Q26
Q27
Q28
D1
D2
D3
D4
D5
D6
D7
D8
D10
D11
D12
D13
D14
D15
D16
D17
ON
OFF
8
BGD
7
C/B
6
5
4
3
2
1

IC1	HD14081BP	C4
IC2	HD14081BP	B2
IC3	HD14073BP	C1
IC4	HD14175BP	B4
IC5	HD14175BP	B1
Q1	2SD636-RS	C1
Q2	2SD636-RS	B1
Q3	2SD636-RS	C3
Q4	2SD636-RS	C3
Q5	2SD636-RS	C3
Q6	2SD636-RS	C3
Q7	2SD636-RS	C3
Q8	2SD636-RS	C3
Q9	2SD636-RS	C3
Q10	2SD636-RS	C3
Q11	2SD636-RS	C3
Q12	2SD636-RS	C3
Q13	2SD636-RS	C2
Q14	2SD636-RS	C2
Q15	2SD636-RS	C2
Q16	2SD636-RS	C2
Q17	2SD636-RS	C2
Q18	2SD636-RS	C2
Q19	2SD636-RS	C2
Q20	2SD639RS	A4
Q21	2SD639RS	A3, A4
Q22	2SD639RS	A3
Q23	2SD639RS	A3
Q24	2SD639RS	A2
Q25	2SD639RS	A2
Q26	2SD639RS	A1
Q27	2SD639RS	A1
Q28	2SD639RS	B4
D1	MA162	B3
D2	MA162	B3
D3	MA162	B3
D4	MA162	B3
D5	MA162	B3
D6	MA162	B2
D7	MA162	B2
D8	MA162	B2
D10	MA162	B4
D11	MA162	B4
D12	MA162	B3
D13	MA162	B3
D14	MA162	B2
D15	MA162	B2
D16	MA162	B2
D17	MA162	B1

SCHEMATIC DIAGRAM OF INPUT PV–PG BOARD


TO MOTHER BOARD
CN22
GND
1 a GND
b GND
2 a +9V IN
b +9V IN
3 a CH. PV–PG OUT
b CUT CONT OUT
4 a GND
b NOT USED
5 a NOT USED
b CH. A. B CONT OUT
6 a GND
b EFFECT CONT OUT
7 a VIDEO 8 or BGD IN
b TALLY 8 OUT
8 a GND
b VIDEO 7–C/BAR CONT IN
9 a VIDEO 7 or C/BAR
b TALLY 7 OUT
10 a GND
b NOT USED
11 a VIDEO 6 IN
b TALLY 6 OUT
12 a GND
b CUT SW CONT IN
13 a VIDEO 5 IN
b TALLY 5 OUT
14 a GND
b GND
15 a VIDEO 4 IN
b TALLY 4 OUT
16 a GND
b PREVIEW DSK CONT OUT
17 a VIDEO 3 IN
b TALLY 3 OUT
18 a GND
b PROGRAM DSK CONT OUT
19 a VIDEO 2 IN
b TALLY 2 OUT
20 a GND
b VIS. PULSE IN
21 a VIDEO 1 IN
b TALLY OUT
22 a +12V IN
b GND
a : COMPONENT SIDE
b : PATTERN SIDE
1
2
3
4
5
6
C/B 7
BGD 8
EFF
DSK
OFF
ON
R30 15(1W)
R31 1K
+12V
+9V
IC2(d) VIS SWITCHING CONT
IC5
IC6
Q21~Q30 PILOT LAMP CONT
Q31 PILOT LAMP BRIGHTNESS CONT
CUT CONT
IC7
EFF, DSK TALLY CONT
IC1(a), (d) IC2(a), (b), (c) IC3 TALLY CONT
IC4(d) CHA, CHB TALLY CONT
IC4(b) Q17, Q18 CROSSTALK SUPPRESS
CROSSTALK SUPP
Q1~Q16, Q19 VIDEO SWITCHING
IC7, IC4(c) Q20 CUT CONT OUT
IC1(c) PROGRAM OUT DSK CONT
IC1(b) PREVIEW OUT DSK CONT
TP1
C1 220μF16V
C2 4.7μF35V
C3 10μF16V
R53 180(1/2W)
Q20
C
B
A

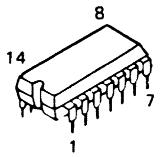
Voltages are measured by following conditions

a( ) : 1 ————→ ON
b( ) : EFF ————→ ON
c( ) : CUT ————→ ON
d( ) : DSK ————→ ON
e( ) : CUT and 1 ————→ ON
f( ) : EFF or DSK ————→ ON
g( ) : CUT and DSK ————→ ON
h( ) : C/7, COLOR BAR SELECTOR → C/B

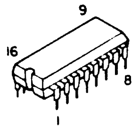
IC1	HD14081BP	B2, B4, B6
IC2	HD14081BP	B2, B3
IC3	HD14073BP	B4, B5
IC4	HD14011BP	B5, B6
IC5	HD14174BP	B2, B3
IC6	YWHD14175BP	B4, B5
IC7	HD14013BP	B6
Q1	2SD636-RS	A2
Q2	2SD636-RS	A2
Q3	2SD636-RS	A3
Q4	2SD636-RS	A3
Q5	2SD636-RS	A3
Q6	2SD636-RS	A3
Q7	2SD636-RS	A7
Q8	2SD636-RS	A8
Q9	2SD636-RS	A4
Q10	2SD636-RS	A4
Q11	2SD636-RS	A4
Q12	2SD636-RS	A4
Q13	2SD636-RS	A4
Q14	2SD636-RS	A4
Q15	2SD636-RS	A5
Q16	2SD636-RS	A5
Q17	2SD636-RS	A5
Q18	2SD636-RS	A5
Q19	2SD636-RS	A5
Q20	2SD636-RS	A6
Q21	2SD639RS	C2
Q22	2SD639RS	C2
Q23	2SD639RS	C3
Q24	2SD639RS	C3
Q25	2SD639RS	C3
Q26	2SD639RS	C4
Q27	2SD639RS	C4
Q28	2SD639RS	C5
Q29	2SD639RS	C5
Q30	2SD639RS	C5
Q31	2SD639RS	B6
D1	MA162	A2
D2	MA162	A2
D3	MA162	A3
D4	MA162	A3
D5	MA162	A4
D6	MA162	A4
D7	MA162	A4
D8	MA162	A5
D9	MA162	B2, C2
D10	MA162	B2, C2
D11	MA162	B2, C2
D12	MA162	B3, C3
D13	MA162	B3, C3
D14	MA162	B4, C4
D15	MA162	B4, C4
D16	MA162	B4, C4
D17	MA162	B5, C5
D18	MA162	B5, C5

CONDUCTOR VIEW OF INPUT PV–PG BOARD

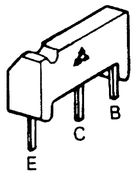
HD14011BP
HD14013BP
HD14073BP
HD14081BP



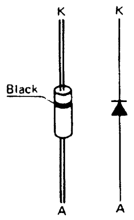
HD14174BP
HD14175BP

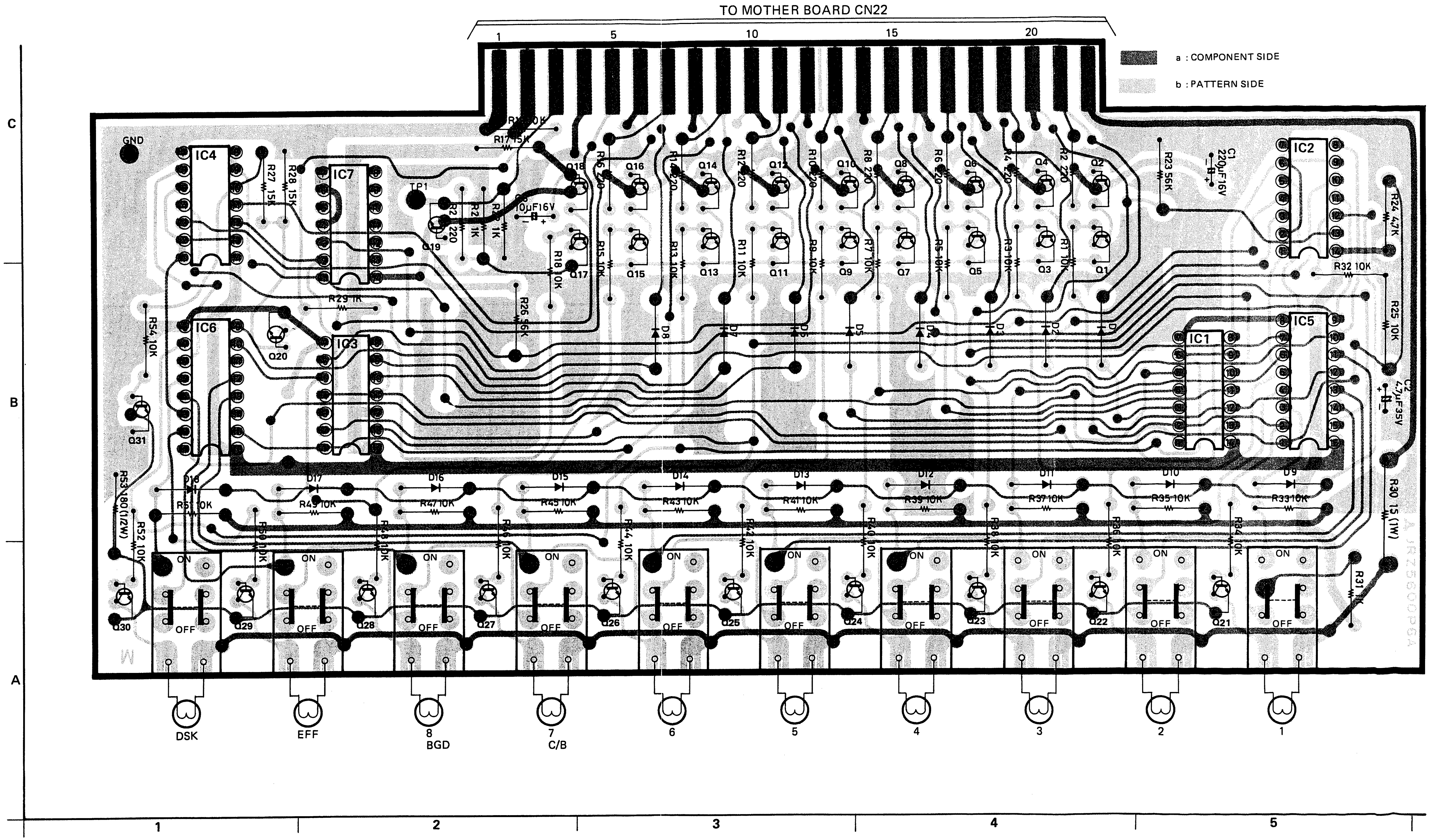


2SD636-RS
2SD639RS



MA162



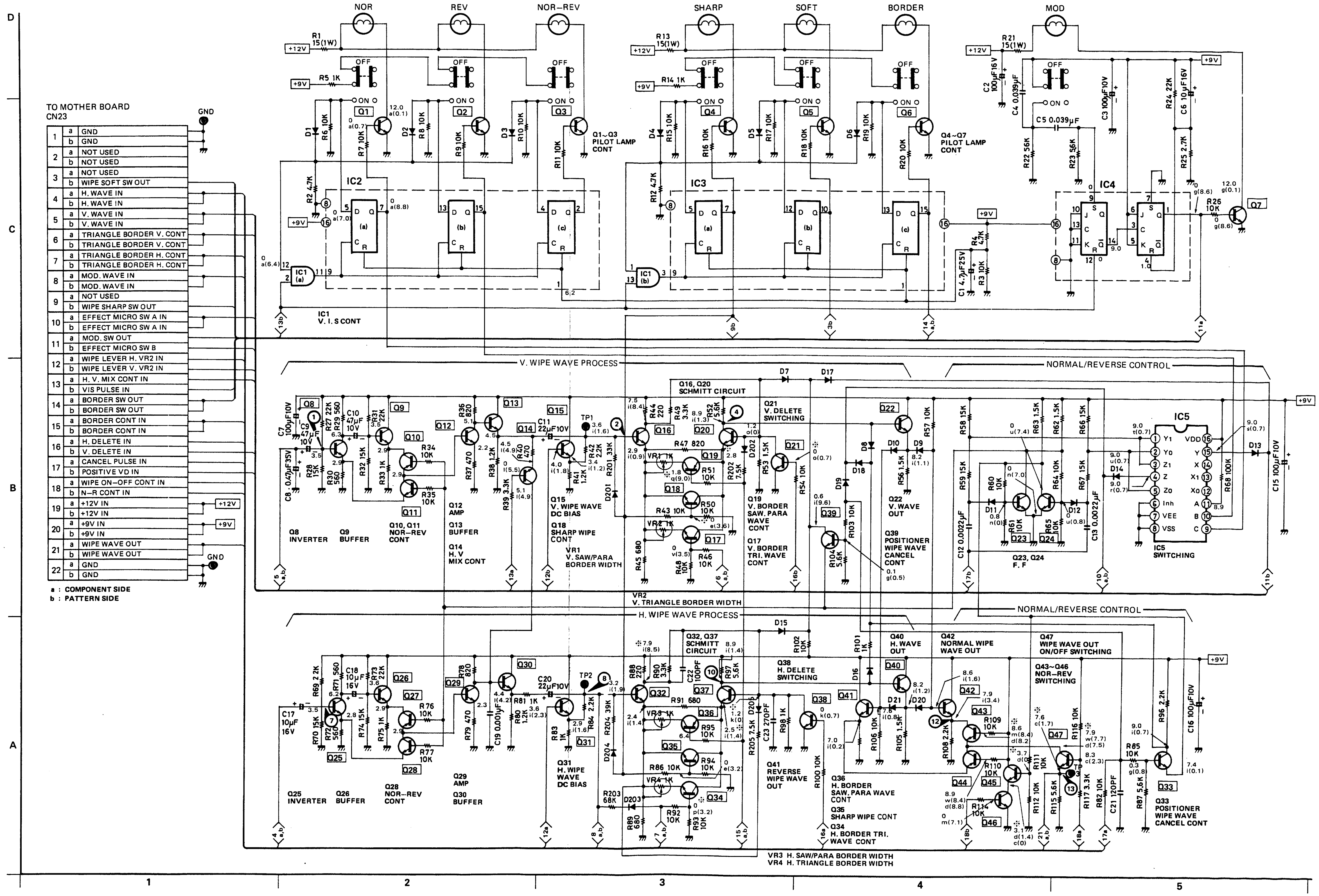

TO MOTHER BOARD CN22
1
5
10
15
20
a : COMPONENT SIDE
b : PATTERN SIDE
C
B
A
1
2
3
4
5
GND
IC1
IC2
IC3
IC4
IC5
IC6
IC7
TP1
C1 220µF16V
C2 4.7µF35V
C3 10µF16V
R23 56K
R24 4.7K
R25 10K
R26 56K
R27 15K
R28 15K
R29 1K
R30 15 (1W)
R31 1K
R32 10K
R53 180 (1/2W)
R54 10K
ON
OFF
DSK
EFF
8
BGD
7
C/B
6
5
4
3
2
1

IC1	HD14081BP	B5	Q2	2SD636-RS	C4	Q10	2SD636-RS	C3	Q18	2SD636-RS	C3	Q26	2SD639RS	A3	D3	MA162	B4
IC2	HD14081BP	C5	Q3	2SD636-RS	C4	Q11	2SD636-RS	C3	Q19	2SD636-RS	C2	Q27	2SD639RS	A2	D4	MA162	B4
IC3	HD14073BP	B2	Q4	2SD636-RS	C4	Q12	2SD636-RS	C3	Q20	2SD636-RS	B1	Q28	2SD639RS	A2	D5	MA162	B3
IC4	HD14011BP	C1	Q5	2SD636-RS	C4	Q13	2SD636-RS	C3	Q21	2SD639RS	A5	Q29	2SD639RS	A1	D6	MA162	B3
IC5	HD14174BP	B5	Q6	2SD636-RS	C4	Q14	2SD636-RS	C3	Q22	2SD639RS	A4	Q30	2SD639RS	A1	D7	MA162	B3
IC6	YWHD14175BP	B1	Q7	2SD636-RS	C4	Q15	2SD636-RS	C3	Q23	2SD639RS	A4	Q31	2SD639RS	B1	D8	MA162	B3
IC7	HD14013BP	C2	Q8	2SD636-RS	C4	Q16	2SD636-RS	C3	Q24	2SD639RS	A3, A4	D1	MA162	B4	D9	MA162	B5
Q1	2SD636-RS	C4	Q9	2SD636-RS	C3	Q17	2SD636-RS	C3	Q25	2SD639RS	A3	D2	MA162	B4	D10	MA162	B5

D11	MA162	B4
D12	MA162	B4
D13	MA162	B3
D14	MA162	B3
D15	MA162	B2
D16	MA162	B2
D17	MA162	B2
D18	MA162	B1

IC1	HD14081BP	C2, C3
IC2	YWHD14175BP	C2, C3
IC3	YWHD14175BP	C3, C4
IC4	HD14027BP	C5
IC5	HD14053BP	B5
Q1	2SD639RS	C2
Q2	2SD639RS	C2
Q3	2SD639RS	C3
Q4	2SD639RS	C3
Q5	2SD639RS	C4
Q6	2SD639RS	C4
Q7	2SD639RS	C5
Q8	2SD636-RS	B2
Q9	2SD636-RS	B2
Q10	2SA1254-BC	B2
Q11	2SC2377CD	B2
Q12	2SD636-RS	B2
Q13	2SD636-RS	B2
Q14	2SD636-RS	B2
Q15	2SD636-RS	B3
Q16	2SC2377CD	B3
Q17	2SC2377CD	B3
Q18	2SC2377CD	B3
Q19	2SA1254-BC	B3
Q20	2SC2377CD	B3
Q21	2SD636-RS	B3
Q22	2SD636-RS	B4
Q23	2SC2377CD	B4
Q24	2SC2377CD	B4
Q25	2SD636-RS	A2
Q26	2SD636-RS	A2
Q27	2SA1254-BC	A2
Q28	2SC2377CD	A2
Q29	2SD636-RS	A2
Q30	2SD636-RS	A2
Q31	2SD636-RS	A3
Q32	2SC1216F	A3
Q33	2SC2377CD	A5
Q34	2SC2377CD	A3
Q35	2SC2377CD	A3
Q36	2SA1254-BC	A3
Q37	2SC1216F	A3
Q38	2SD636-RS	A4
Q39	2SD636-RS	B4
Q40	2SD636-RS	A4
Q41	2SD636-RS	A4
Q42	2SD636-RS	A4
Q43	2SC2377CD	A4
Q44	2SA1254-BC	A4
Q45	2SD636-RS	A4
Q46	2SD636-RS	A4
Q47	2SD636-RS	A5
D1	MA165	C2
D2	MA165	C2
D3	MA165	C2
D4	MA165	C3
D5	MA165	C3
D6	MA165	C4
D7	MA165	B3
D8	MA165	B4
D9	MA165	B4
D10	MA165	B4
D11	MA165	B4
D12	MA165	B5
D13	MA165	B5
D14	MA165	B5
D15	MA165	A3
D16	MA165	A4
D17	MA165	B4
D18	MA165	B4
D19	MA165	B4
D20	MA165	A4
D21	MA165	A4
D201	MA165	B3
D202	MA165	B3
D203	MA165	A3
D204	MA165	A3
D205	MA165	A3

SCHEMATIC DIAGRAM OF WIPE PROCESS BOARD


NOR
REV
NOR-REV
SHARP
SOFT
BORDER
MOD
Q1~Q3 PILOT LAMP CONT
Q4~Q7 PILOT LAMP CONT
IC1 V. I. S CONT
IC2
IC3
IC4
IC5
TO MOTHER BOARD CN23
GND
NOT USED
WIPE SOFT SW OUT
H. WAVE IN
V. WAVE IN
TRIANGLE BORDER V. CONT
TRIANGLE BORDER H. CONT
MOD. WAVE IN
WIPE SHARP SW OUT
EFFECT MICRO SW A IN
MOD. SW OUT
EFFECT MICRO SW B
WIPE LEVER H. VR2 IN
WIPE LEVER V. VR2 IN
H. V. MIX CONT IN
VIS PULSE IN
BORDER SW OUT
BORDER CONT IN
H. DELETE IN
V. DELETE IN
CANCEL PULSE IN
POSITIVE VD IN
WIPE ON-OFF CONT IN
N-R CONT IN
+12V IN
+9V IN
WIPE WAVE OUT
a : COMPONENT SIDE
b : PATTERN SIDE
V. WIPE WAVE PROCESS
NORMAL/REVERSE CONTROL
Q16, Q20 SCHMITT CIRCUIT
Q21 V. DELETE SWITCHING
Q8 INVERTER
Q9 BUFFER
Q10, Q11 NOR-REV CONT
Q12 AMP
Q13 BUFFER
Q14 H. V MIX CONT
Q15 V. WIPE WAVE DC BIAS
Q18 SHARP WIPE CONT
VR1 V. SAW/PARA BORDER WIDTH
Q19 V. BORDER SAW. PARA WAVE CONT
Q17 V. BORDER TRI. WAVE CONT
Q22 V. WAVE OUT
Q39 POSITIONER WIPE WAVE CANCEL CONT
Q23, Q24 F. F
IC5 SWITCHING
VR2 V. TRIANGLE BORDER WIDTH
H. WIPE WAVE PROCESS
Q32, Q37 SCHMITT CIRCUIT
Q38 H. DELETE SWITCHING
Q40 H. WAVE OUT
Q42 NORMAL WIPE WAVE OUT
Q47 WIPE WAVE OUT ON/OFF SWITCHING
Q43~Q46 NOR-REV SWITCHING
Q25 INVERTER
Q26 BUFFER
Q28 NOR-REV CONT
Q29 AMP
Q30 BUFFER
Q31 H. WIPE WAVE DC BIAS
Q41 REVERSE WIPE WAVE OUT
Q36 H. BORDER SAW. PARA WAVE CONT
Q35 SHARP WIPE CONT
Q34 H. BORDER TRI. WAVE CONT
Q33 POSITIONER WIPE WAVE CANCEL CONT
VR3 H. SAW/PARA BORDER WIDTH
VR4 H. TRIANGLE BORDER WIDTH
TP1
TP2
+12V
+9V
A
B
C
D
1
2
3
4
5

Voltages are measured by following conditions

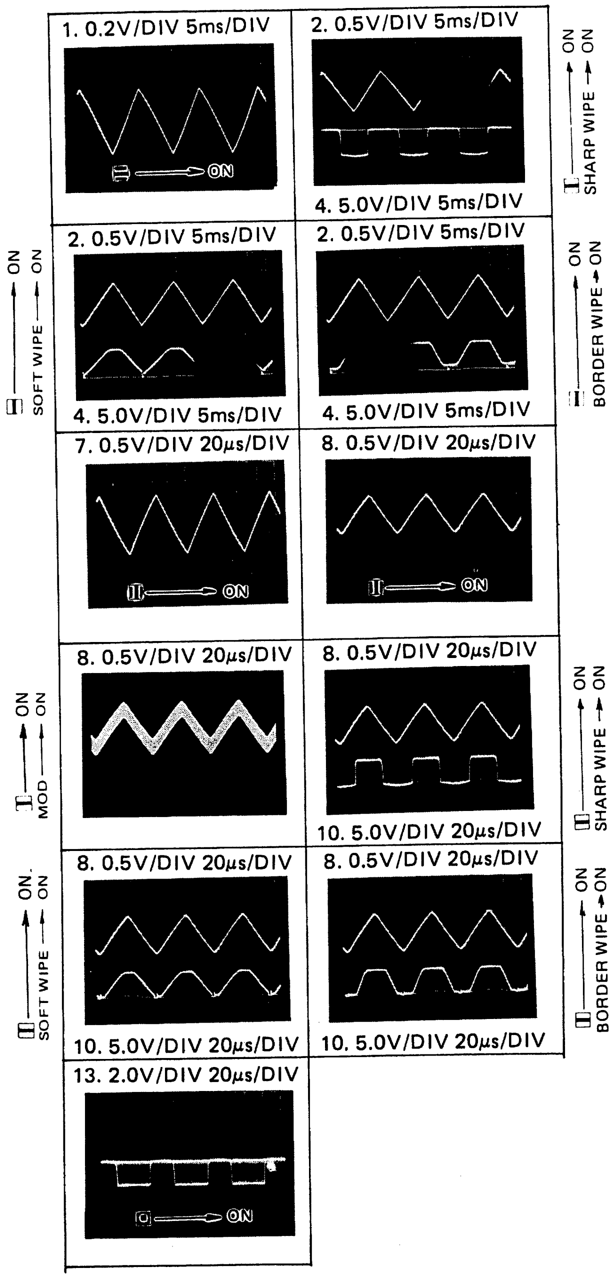
a ( ) : NORM ——→ ON
b ( ) : WIPE ——→ ON
c ( ) : WIPE ——→ OFF
d ( ) : REV ——→ ON
e ( ) : SHARP WIPE ——→ ON
f ( ) : (▜, ▟ or ▣ → ON) and (REV → ON)

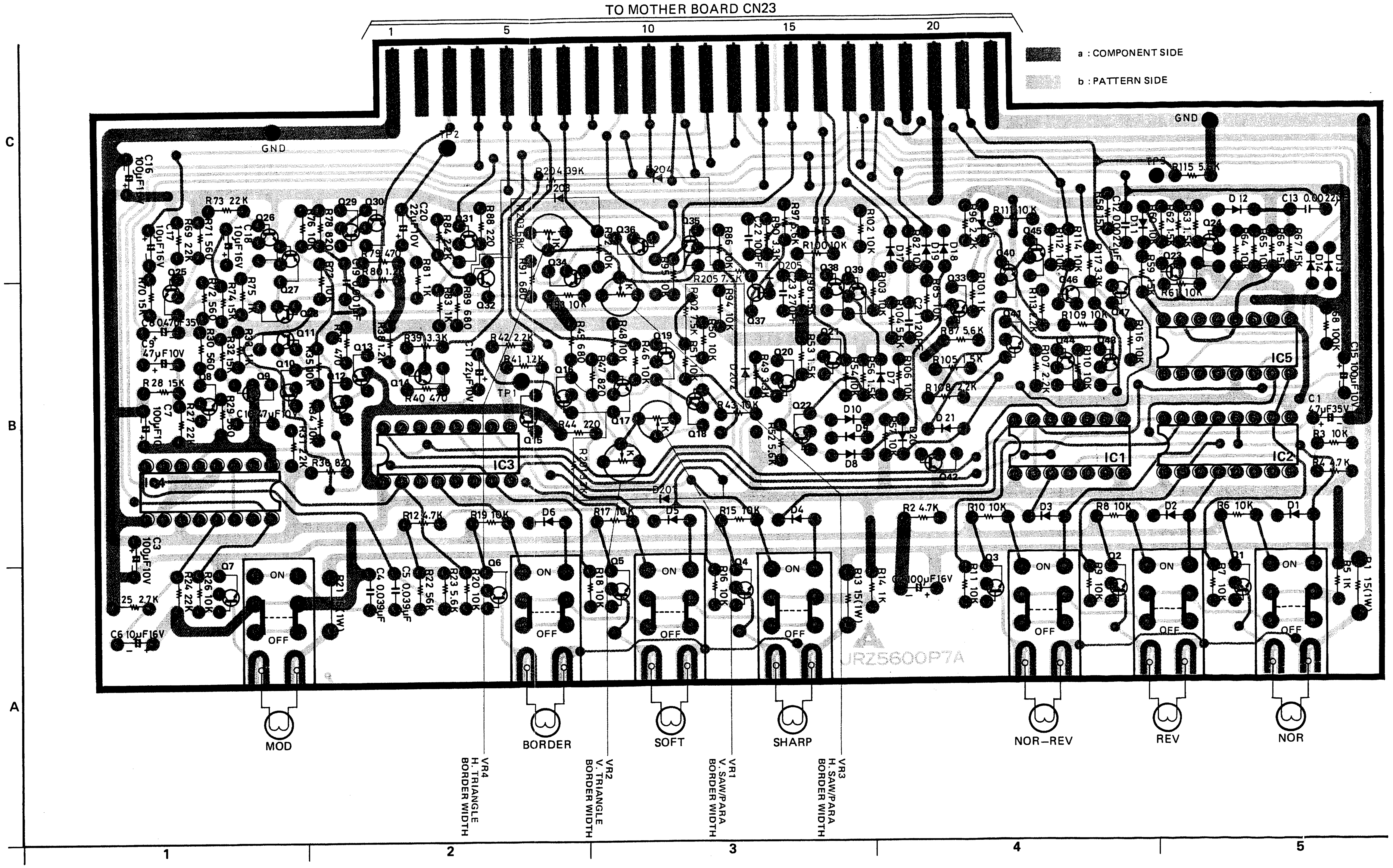
g ( ) : POSI ——→ ON
h ( ) : WIPE LEVER ——→ TOP
i ( ) : WIPE LEVER ——→ BOTTOM
k ( ) : ⬓ or ▤ ——→ ON
l ( ) : ◪ or ⊡ ——→ ON
m ( ) : ▜, ▟ or ▣ ——→ ON

n ( ) : (WIPE LEVER → TOP) and (REV → ON)
o ( ) : ◨, ◪, ◫, ⊡ → ON
p ( ) : (◫ or ▣ → ON) and (BOARD WIPE → ON)
q ( ) : ◫, ▤, ▣ or EXT → ON
r ( ) : (WIPE LEVER → TOP) and (NORM REV → ON)
s ( ) : (WIPE LEVER → BOTTOM) and (NORM REV → ON)

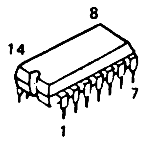
t( ) : (WIPE LEVER → BOTTOM) and (NORM → ON)
u( ) : (WIPE LEVER → BOTTOM) and (REV or NORM REV → ON)
v( ) : (▤ or ▣ → ON) and (BOARD WIPE → ON)
※ : WIPE LEVER → TOP

CONDUCTOR VIEW OF WIPE PROCESS BOARD

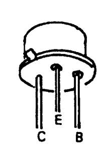



TO MOTHER BOARD CN23
1
5
10
15
20
a : COMPONENT SIDE
b : PATTERN SIDE
GND
TP1
TP2
TP3
IC1
IC2
IC3
IC4
IC5
ON
OFF
URZ5600P7A
MOD
BORDER
SOFT
SHARP
NOR–REV
REV
NOR
VR4 H. TRIANGLE BORDER WIDTH
VR2 V. TRIANGLE BORDER WIDTH
VR1 V. SAW/PARA BORDER WIDTH
VR3 H. SAW/PARA BORDER WIDTH
A
B
C
1
2
3
4
5

HD14027BP
HD14053BP
HD14081BP

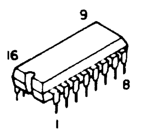


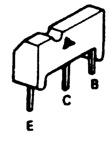
2SC1216F



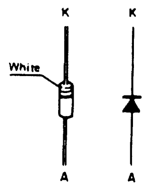
2SA1254-BC
2SC2377CD
2SD636-RS
2SD639RS

HD14175BP



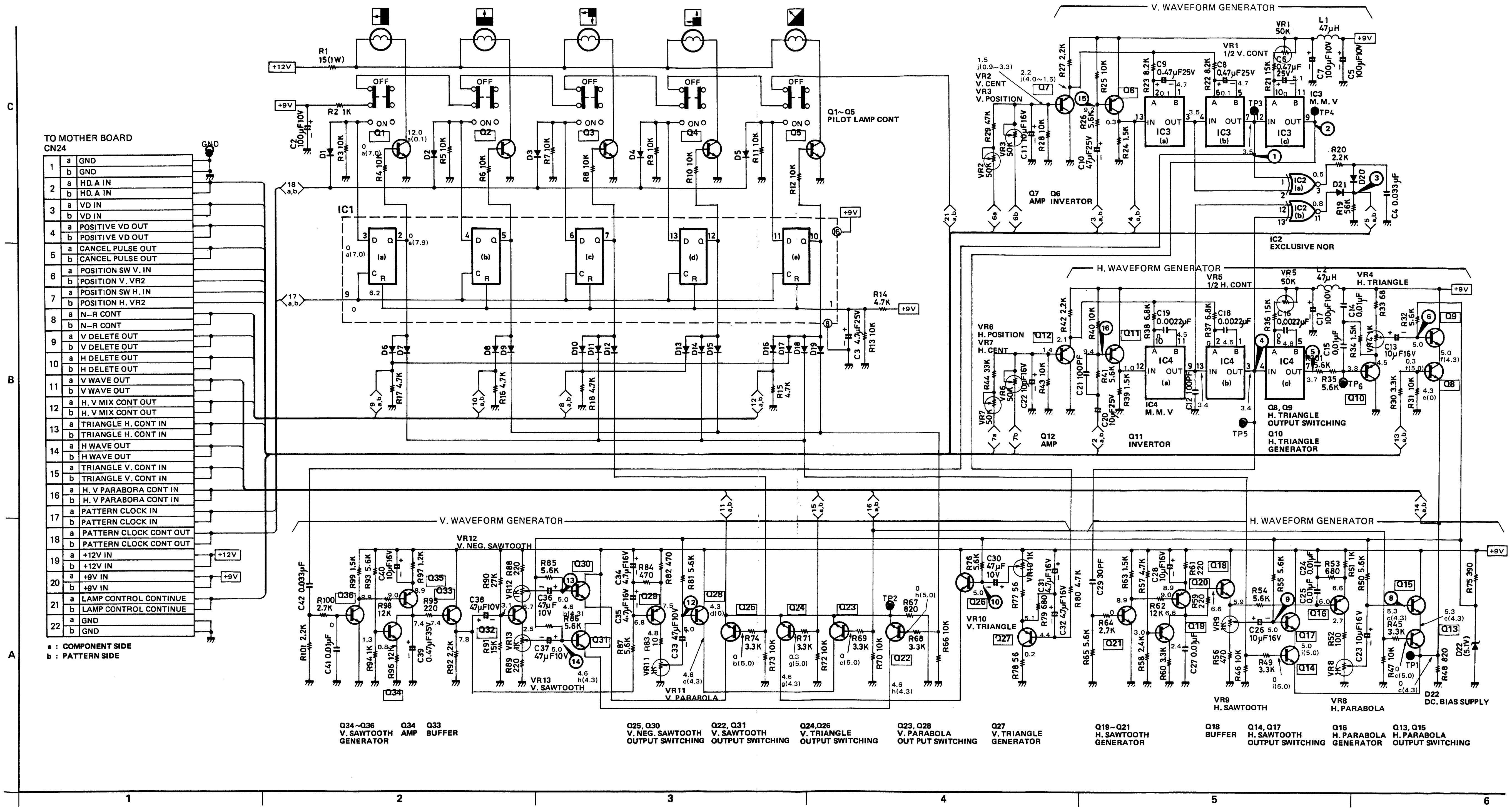


MA165



IC1	HD14081BP	B4
IC2	YWHD14175BP	B5
IC3	YWHD14175BP	B2
IC4	HD14027BP	B1
IC5	HD14053BP	B5
Q1	2SD639RS	A5
Q2	2SD639RS	A4
Q3	2SD639RS	A4
Q4	2SD639RS	A3
Q5	2SD639RS	A3
Q6	2SD639RS	A2
Q7	2SD639RS	A1
Q8	2SD636-RS	B1
Q9	2SD636-RS	B1
Q10	2SA1254-BC	B1
Q11	2SC2377CD	B1
Q12	2SD636-RS	B2
Q13	2SD636-RS	B2
Q14	2SD636-RS	B2
Q15	2SD636-RS	B2
Q16	2SC2377CD	B2
Q17	2SC2377CD	B3
Q18	2SC2377CD	B3
Q19	2SA1254-BC	B3
Q20	2SC2377CD	B3
Q21	2SD636-RS	B3
Q22	2SD636-RS	B3
Q23	2SC2377CD	C5
Q24	2SC2377CD	C5
Q25	2SD636-RS	B1
Q26	2SD636-RS	C1
Q27	2SA1254-BC	C1
Q28	2SC2377CD	B1
Q29	2SD636-RS	C2
Q30	2SD636-RS	C2
Q31	2SD636-RS	C2
Q32	2SC1216F	C2
Q33	2SC2377CD	B4
Q34	2SC2377CD	C2
Q35	2SC2377CD	C3
Q36	2SA1254-BC	C3
Q37	2SC1216F	B3
Q38	2SD636-RS	B3
Q39	2SD636-RS	B3
Q40	2SD636-RS	B4, C4
Q41	2SD636-RS	B4
Q42	2SD636-RS	B4
Q43	2SC2377CD	B4
Q44	2SA1254-BC	B4
Q45	2SD636-RS	C4
Q46	2SD636-RS	B4
Q47	2SD636-RS	B4
D1	MA165	B5
D2	MA165	B5
D3	MA165	B4
D4	MA165	B4
D5	MA165	B4
D6	MA165	B2
D7	MA165	B4
D8	MA165	B3
D9	MA165	B3
D10	MA165	B3
D11	MA165	C4
D12	MA165	C5
D13	MA165	B5, C5
D14	MA165	B5, C5
D15	MA165	C3
D16	MA165	C4
D17	MA165	C4
D18	MA165	C4
D19	MA165	C4
D20	MA165	B4
D21	MA165	B4
D201	MA165	B3
D202	MA165	B3
D203	MA165	C2
D204	MA165	C3
D205	MA165	B3

SCHEMATIC DIAGRAM OF WAVEFORM GEN BOARD


V. WAVEFORM GENERATOR
H. WAVEFORM GENERATOR
TO MOTHER BOARD
CN24
GND
1 a GND
1 b GND
2 a HD.A IN
2 b HD.A IN
3 a VD IN
3 b VD IN
4 a POSITIVE VD OUT
4 b POSITIVE VD OUT
5 a CANCEL PULSE OUT
5 b CANCEL PULSE OUT
6 a POSITION SW V. IN
6 b POSITION V. VR2
7 a POSITION SW H. IN
7 b POSITION H. VR2
8 a N-R CONT
8 b N-R CONT
9 a V DELETE OUT
9 b V DELETE OUT
10 a H DELETE OUT
10 b H DELETE OUT
11 a V WAVE OUT
11 b V WAVE OUT
12 a H. V MIX CONT OUT
12 b H. V MIX CONT OUT
13 a TRIANGLE H. CONT IN
13 b TRIANGLE H. CONT IN
14 a H WAVE OUT
14 b H WAVE OUT
15 a TRIANGLE V. CONT IN
15 b TRIANGLE V. CONT IN
16 a H. V PARABORA CONT IN
16 b H. V PARABORA CONT IN
17 a PATTERN CLOCK IN
17 b PATTERN CLOCK IN
18 a PATTERN CLOCK CONT OUT
18 b PATTERN CLOCK CONT OUT
19 a +12V IN
19 b +12V IN
20 a +9V IN
20 b +9V IN
21 a LAMP CONTROL CONTINUE
21 b LAMP CONTROL CONTINUE
22 a GND
22 b GND
a : COMPONENT SIDE
b : PATTERN SIDE
+12V
+9V
R1 15(1W)
R2 1K
IC1
Q1~Q5 PILOT LAMP CONT
OFF
ON
Q7 AMP
Q6 INVERTOR
VR1 50K
VR1 1/2 V. CONT
L1 47μH
VR2 V. CENT
VR3 V. POSITION
IC3 M. M. V
IC2 EXCLUSIVE NOR
TP4
VR5 1/2 H. CONT
VR4 H. TRIANGLE
L2 47μH
VR6 H. POSITION
VR7 H. CENT
IC4 M. M. V
Q12 AMP
Q11 INVERTOR
TP5
TP6
Q8, Q9 H. TRIANGLE OUTPUT SWITCHING
Q10 H. TRIANGLE GENERATOR
VR12 V. NEG. SAWTOOTH
VR13 V. SAWTOOTH
VR11 V. PARABOLA
VR10 V. TRIANGLE
TP2
VR9 H. SAWTOOTH
VR8 H. PARABOLA
TP1
D22 DC. BIAS SUPPLY
Q34~Q36 V. SAWTOOTH GENERATOR
Q34 AMP
Q33 BUFFER
Q25, Q30 V. NEG. SAWTOOTH OUTPUT SWITCHING
Q22, Q31 V. SAWTOOTH OUTPUT SWITCHING
Q24, Q26 V. TRIANGLE OUTPUT SWITCHING
Q23, Q28 V. PARABOLA OUT PUT SWITCHING
Q27 V. TRIANGLE GENERATOR
Q19~Q21 H. SAWTOOTH GENERATOR
Q18 BUFFER
Q14, Q17 H. SAWTOOTH OUTPUT SWITCHING
Q16 H. PARABOLA GENERATOR
Q13, Q15 H. PARABOLA OUTPUT SWITCHING
A
B
C
1
2
3
4
5
6

Voltages are measured by following conditions

a( ) : ◨ ——→ ON

b( ) : ◳ ——→ ON

c( ) : ⊡ ——→ ON

d( ) : ◨ or ◫ ——→ ON

e( ) : ⬓ or ⊟ ——→ ON

f( ) : ◫ or ▣ ——→ ON

g( ) : ⊟ or ▣ ——→ ON

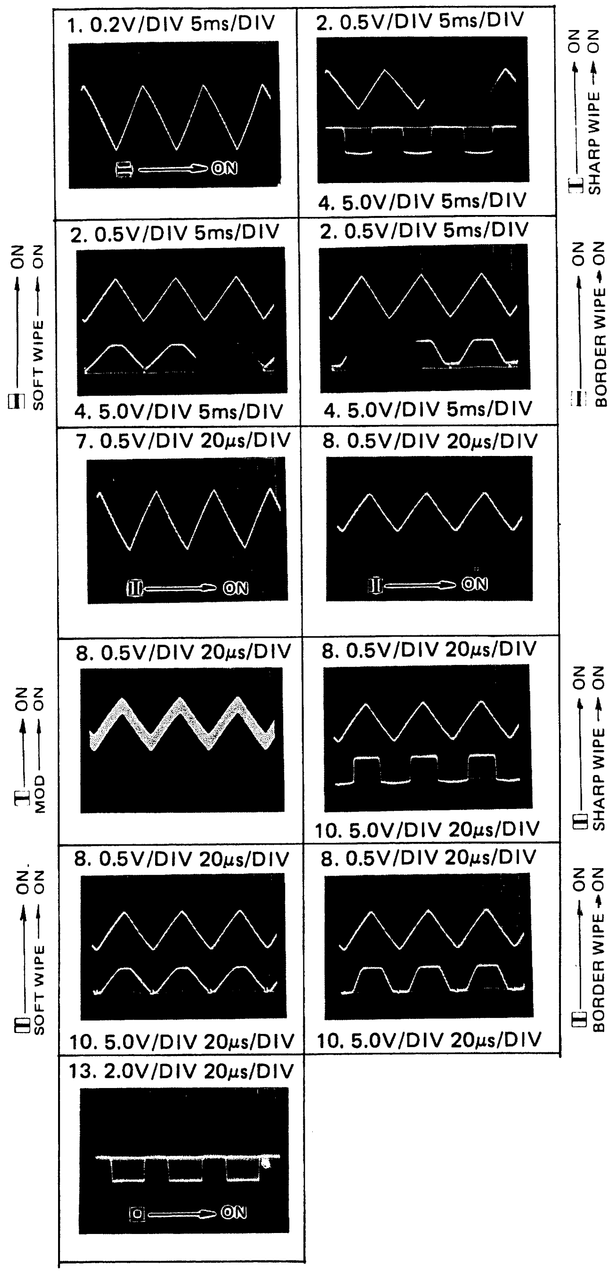
h( ) : ⬓ , ◲ or ◪ ——→ ON

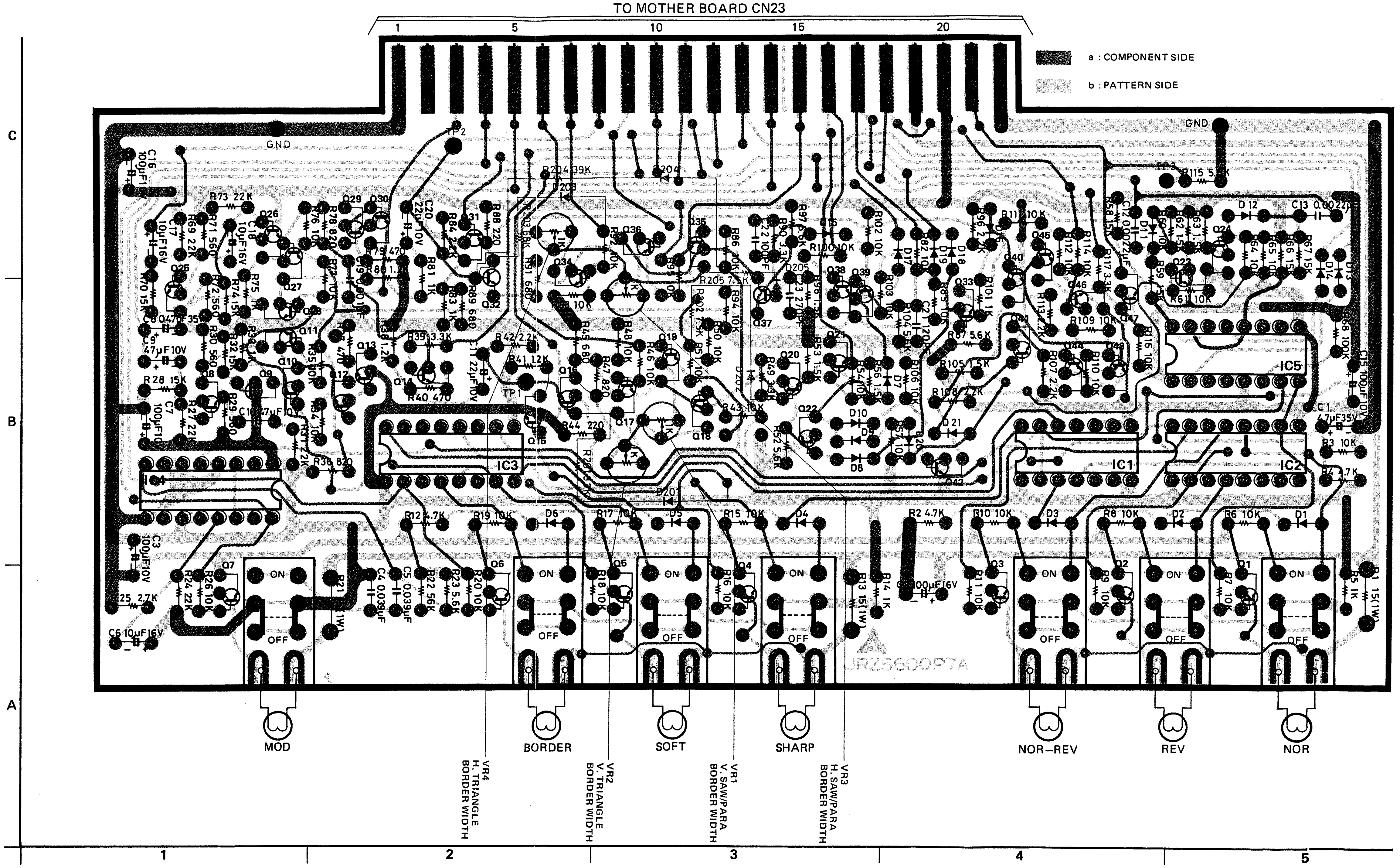
i( ) : ◨ , ◳ , ◲ or ◪ → ON

j( ) : (POSI → ON) and (POSITION → CHANGE)

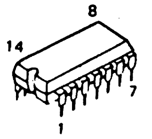
IC1	HD14174BP	B2, B3
IC2	MC14077BP	C5
IC3	DN850	C5
IC4	DN850	B5
Q1	2SD639RS	C2
Q2	2SD639RS	C2
Q3	2SD639RS	C3
Q4	2SD639RS	C3
Q5	2SD639RS	C4
Q6	2SB641-RS	C5
Q7	2SB641-RS	C4
Q8	2SD636-RS	B6
Q9	2SD636-RS	B6
Q10	2SB641-RS	B6
Q11	2SB641-RS	B5
Q12	2SB641-RS	B4
Q13	2SD636-RS	A6
Q14	2SD636-RS	A5
Q15	2SD636-RS	A6
Q16	2SB641-RS	A5
Q17	2SD636-RS	A5
Q18	2SD636-RS	A5
Q19	2SD636-RS	A5
Q20	2SB641-RS	A5
Q21	2SD636-RS	A5
Q22	2SD636-RS	A4
Q23	2SD636-RS	A4
Q24	2SD636-RS	A3
Q25	2SD636-RS	A3
Q26	2SD636-RS	A4
Q27	2SB641-RS	A4
Q28	2SD636-RS	A3
Q29	2SB641-RS	A3
Q30	2SD636-RS	A3
Q31	2SD636-RS	A3
Q32	2SD636-RS	A2
Q33	2SD636-RS	A2
Q34	2SD636-RS	A2
Q35	2SB641-RS	A2
Q36	2SD636-RS	A2
D1	MA165	C2
D2	MA165	C2
D3	MA165	C2
D4	MA165	C3
D5	MA165	C3
D6	MA165	B2
D7	MA165	B2
D8	MA165	B2
D9	MA165	B2
D10	MA165	B3
D11	MA165	B3
D12	MA165	B3
D13	MA165	B3
D14	MA165	B3
D15	MA165	B3
D16	MA165	B3
D17	MA165	B3
D18	MA165	B4
D19	MA165	B4
D20	MA165	C5
D21	MA165	C5
D22	YUD-XZ051	A6

CONDUCTOR VIEW OF WIPE PROCESS BOARD

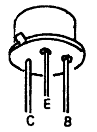



TO MOTHER BOARD CN23
1
5
10
15
20
a : COMPONENT SIDE
b : PATTERN SIDE
GND
TP1
TP2
TP3
IC1
IC2
IC3
IC5
ON
OFF
URZ5600P7A
MOD
BORDER
SOFT
SHARP
NOR-REV
REV
NOR
VR4 H. TRIANGLE BORDER WIDTH
VR2 V. TRIANGLE BORDER WIDTH
VR1 V. SAW/PARA BORDER WIDTH
VR3 H. SAW/PARA BORDER WIDTH
A
B
C
1
2
3
4
5

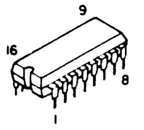
HD14027BP
HD14053BP
HD14081BP



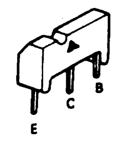
2SC1216F



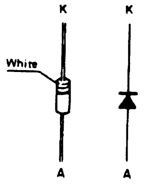
HD14175BP



2SA1254-BC
2SC2377CD
2SD636-RS
2SD639RS

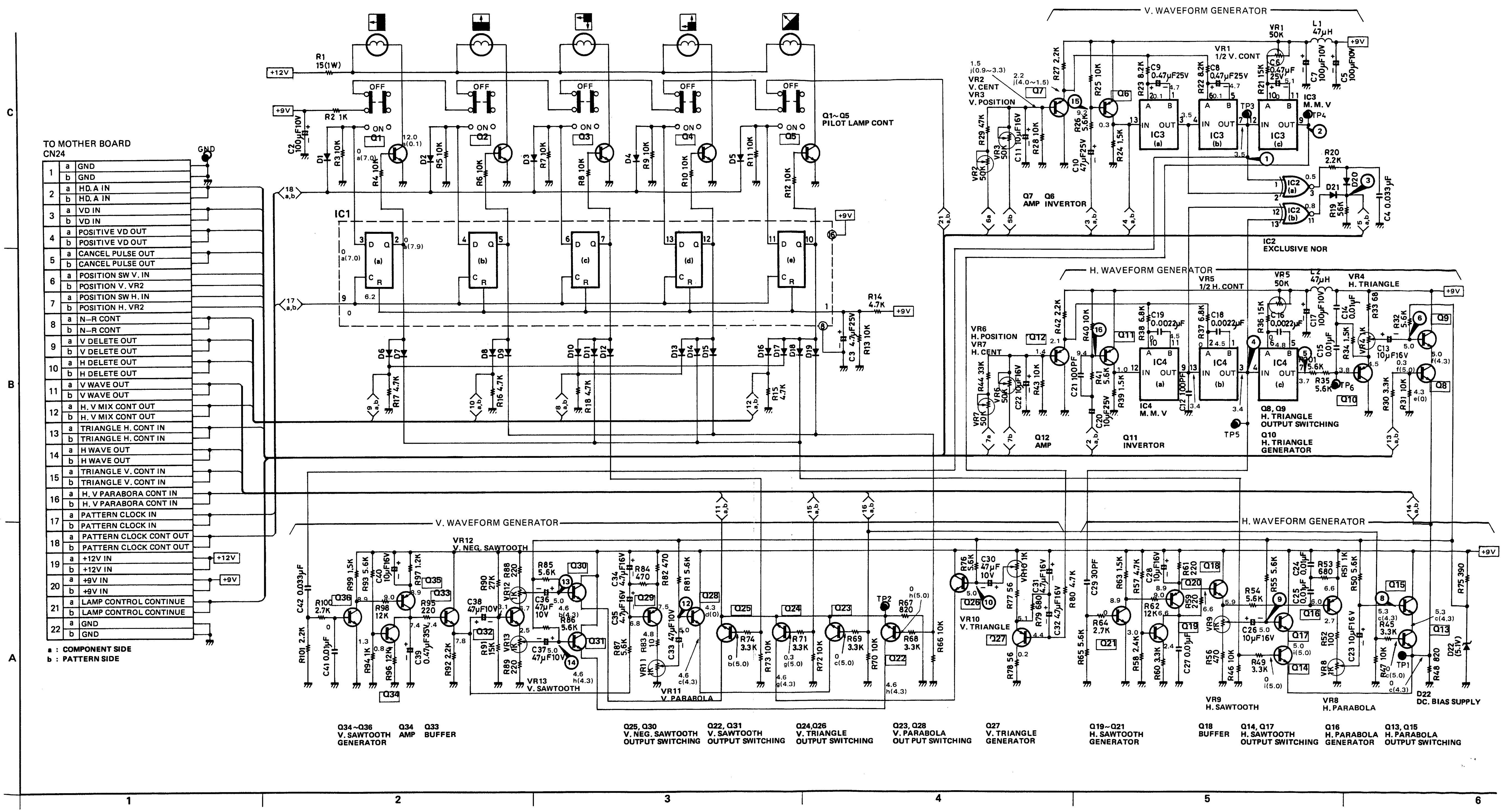


MA165



IC1	HD14081BP	B4	Q9	2SD636-RS	B1	Q22	2SD636-RS	B3	Q35	2SC2377CD	C3	D1	MA165	B5	D14	MA165	B5, C5
IC2	YWHD14175BP	B5	Q10	2SA1254-BC	B1	Q23	2SC2377CD	C5	Q36	2SA1254-BC	C3	D2	MA165	B5	D15	MA165	C3
IC3	YWHD14175BP	B2	Q11	2SC2377CD	B1	Q24	2SC2377CD	C5	Q37	2SC1216F	B3	D3	MA165	B4	D16	MA165	C4
IC4	HD14027BP	B1	Q12	2SD636-RS	B2	Q25	2SD636-RS	B1	Q38	2SD636-RS	B3	D4	MA165	B4	D17	MA165	C4
IC5	HD14053BP	B5	Q13	2SD636-RS	B2	Q26	2SD636-RS	C1	Q39	2SD636-RS	B3	D5	MA165	B4	D18	MA165	C4
Q1	2SD639RS	A5	Q14	2SD636-RS	B2	Q27	2SA1254-BC	C1	Q40	2SD636-RS	B4, C4	D6	MA165	B2	D19	MA165	C4
Q2	2SD639RS	A4	Q15	2SD636-RS	B2	Q28	2SC2377CD	B1	Q41	2SD636-RS	B4	D7	MA165	B4	D20	MA165	B4
Q3	2SD639RS	A4	Q16	2SC2377CD	B2	Q29	2SD636-RS	C2	Q42	2SD636-RS	B4	D8	MA165	B3	D21	MA165	B4
Q4	2SD639RS	A3	Q17	2SC2377CD	B3	Q30	2SD636-RS	C2	Q43	2SC2377CD	B4	D9	MA165	B3	D201	MA165	B3
Q5	2SD639RS	A3	Q18	2SC2377CD	B3	Q31	2SD636-RS	C2	Q44	2SA1254-BC	B4	D10	MA165	B3	D202	MA165	B3
Q6	2SD639RS	A2	Q19	2SA1254-BC	B3	Q32	2SC1216F	C2	Q45	2SD636-RS	C4	D11	MA165	C4	D203	MA165	C2
Q7	2SD639RS	A1	Q20	2SC2377CD	B3	Q33	2SC2377CD	B4	Q46	2SD636-RS	B4	D12	MA165	C5	D204	MA165	C3
Q8	2SD636-RS	B1	Q21	2SD636-RS	B3	Q34	2SC2377CD	C2	Q47	2SD636-RS	B4	D13	MA165	B5, C5	D205	MA165	B3

SCHEMATIC DIAGRAM OF WAVEFORM GEN BOARD


V. WAVEFORM GENERATOR
H. WAVEFORM GENERATOR
TO MOTHER BOARD
CN24
GND
1 a GND
b GND
2 a HD. A IN
b HD. A IN
3 a VD IN
b VD IN
4 a POSITIVE VD OUT
b POSITIVE VD OUT
5 a CANCEL PULSE OUT
b CANCEL PULSE OUT
6 a POSITION SW V. IN
b POSITION V. VR2
7 a POSITION SW H. IN
b POSITION H. VR2
8 a N–R CONT
b N–R CONT
9 a V DELETE OUT
b V DELETE OUT
10 a H DELETE OUT
b H DELETE OUT
11 a V WAVE OUT
b V WAVE OUT
12 a H. V MIX CONT OUT
b H. V MIX CONT OUT
13 a TRIANGLE H. CONT IN
b TRIANGLE H. CONT IN
14 a H WAVE OUT
b H WAVE OUT
15 a TRIANGLE V. CONT IN
b TRIANGLE V. CONT IN
16 a H. V PARABORA CONT IN
b H. V PARABORA CONT IN
17 a PATTERN CLOCK IN
b PATTERN CLOCK IN
18 a PATTERN CLOCK CONT OUT
b PATTERN CLOCK CONT OUT
19 a +12V IN
b +12V IN
20 a +9V IN
b +9V IN
21 a LAMP CONTROL CONTINUE
b LAMP CONTROL CONTINUE
22 a GND
b GND
a : COMPONENT SIDE
b : PATTERN SIDE
+12V
+9V
R1 15(1W)
R2 1K
C2 100μF10V
Q1~Q5 PILOT LAMP CONT
IC1
R14 4.7K
C3 4.7μF25V
R13 10K
VR1 50K
VR1 1/2 V. CONT
L1 47μH
C7 100μF10V
C5 100μF10V
VR2 V. CENT
VR3 V. POSITION
Q7 Q6 AMP INVERTOR
IC3 M.M.V
IC2 EXCLUSIVE NOR
R20 2.2K
C4 0.033μF
VR5 50K
VR5 1/2 H. CONT
L2 47μH
VR4 H. TRIANGLE
VR6 H. POSITION
VR7 H. CENT
Q12 AMP
Q11 INVERTOR
IC4 M.M.V
TP5
Q8, Q9 H. TRIANGLE OUTPUT SWITCHING
Q10 H. TRIANGLE GENERATOR
VR12 V. NEG. SAWTOOTH
VR13 V. SAWTOOTH
VR11 V. PARABOLA
VR10 V. TRIANGLE
VR9 H. SAWTOOTH
VR8 H. PARABOLA
D22 DC. BIAS SUPPLY
TP1
TP2
Q34~Q36 V. SAWTOOTH GENERATOR
Q34 AMP
Q33 BUFFER
Q25, Q30 V. NEG. SAWTOOTH OUTPUT SWITCHING
Q22, Q31 V. SAWTOOTH OUTPUT SWITCHING
Q24, Q26 V. TRIANGLE OUTPUT SWITCHING
Q23, Q28 V. PARABOLA OUT PUT SWITCHING
Q27 V. TRIANGLE GENERATOR
Q19~Q21 H. SAWTOOTH GENERATOR
Q18 BUFFER
Q14, Q17 H. SAWTOOTH OUTPUT SWITCHING
Q16 H. PARABOLA GENERATOR
Q13, Q15 H. PARABOLA OUTPUT SWITCHING
A
B
C
1
2
3
4
5
6

Voltages are measured by following conditions

a(　) : ◨ ——→ ON

b(　) : ◳ ——→ ON

c(　) : ⊡ ——→ ON

d(　) : ◨ or ◫ ——→ ON

e(　) : ⬓ or ⊟ ——→ ON

f(　) : ◫ or ▣ ——→ ON

g(　) : ⊟ or ▣ ——→ ON

h(　) : ⬓, ◲ or ◪ ——→ ON

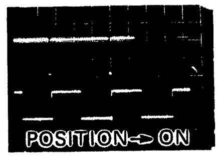
i(　) : ◨, ◳, ◲ or ◪ → ON

j(　) : (POSI → ON) and (POSITION → CHANGE)

IC1	HD14174BP	B2, B3
IC2	MC14077BP	C5
IC3	DN850	C5
IC4	DN850	B5
Q1	2SD639RS	C2
Q2	2SD639RS	C2
Q3	2SD639RS	C3
Q4	2SD639RS	C3
Q5	2SD639RS	C4
Q6	2SB641-RS	C5
Q7	2SB641-RS	C4
Q8	2SD636-RS	B6
Q9	2SD636-RS	B6
Q10	2SB641-RS	B6
Q11	2SB641-RS	B5
Q12	2SB641-RS	B4
Q13	2SD636-RS	A6
Q14	2SD636-RS	A5
Q15	2SD636-RS	A6
Q16	2SB641-RS	A5
Q17	2SD636-RS	A5
Q18	2SD636-RS	A5
Q19	2SD636-RS	A5
Q20	2SB641-RS	A5
Q21	2SD636-RS	A5
Q22	2SD636-RS	A4
Q23	2SD636-RS	A4
Q24	2SD636-RS	A3
Q25	2SD636-RS	A3
Q26	2SD636-RS	A4
Q27	2SB641-RS	A4
Q28	2SD636-RS	A3
Q29	2SB641-RS	A3
Q30	2SD636-RS	A3
Q31	2SD636-RS	A3
Q32	2SD636-RS	A2
Q33	2SD636-RS	A2
Q34	2SD636-RS	A2
Q35	2SB641-RS	A2
Q36	2SD636-RS	A2
D1	MA165	C2
D2	MA165	C2
D3	MA165	C2
D4	MA165	C3
D5	MA165	C3
D6	MA165	B2
D7	MA165	B2
D8	MA165	B2
D9	MA165	B2
D10	MA165	B3
D11	MA165	B3
D12	MA165	B3
D13	MA165	B3
D14	MA165	B3
D15	MA165	B3
D16	MA165	B3
D17	MA165	B3
D18	MA165	B4
D19	MA165	B4
D20	MA165	C5
D21	MA165	C5
D22	YUD-XZ051	A6

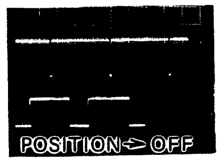
CONDUCTOR VIEW OF WAVEFORM GEN BOARD

15. 0.5V/DIV 5ms/DIV



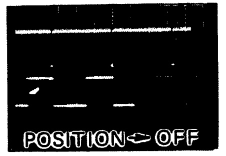
1. 5.0V/DIV 5ms/DIV

15. 0.5V/DIV 5ms/DIV



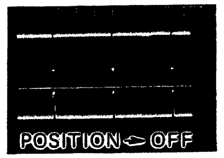
1. 5.0V/DIV 5ms/DIV

15. 0.5V/DIV 5ms/DIV



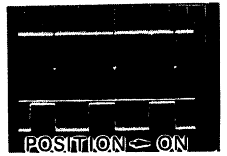
2. 5.0V/DIV 5ms/DIV

15. 0.5V/DIV 5ms/DIV



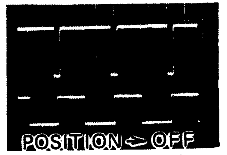
3. 5.0V/DIV 5ms/DIV

15. 0.5V/DIV 5ms/DIV



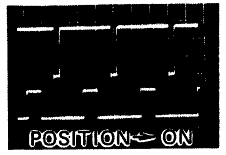
3. 5.0V/DIV 5ms/DIV

16. 0.5V/DIV 20µs/DIV



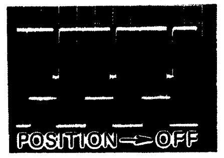
4. 5.0V/DIV 20µs/DIV

16. 0.5V/DIV 20µs/DIV



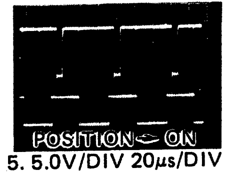
4. 5.0V/DIV 20µs/DIV

16. 0.5V/DIV 20µs/DIV



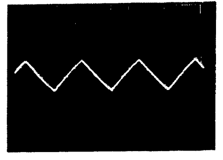
5. 5.0V/DIV 20µs/DIV

16. 0.5V/DIV 20µs/DIV

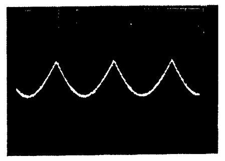


5. 5.0V/DIV 20µs/DIV

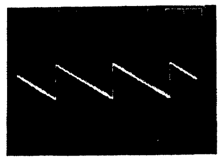
6. 1.0V/DIV 20µs/DIV



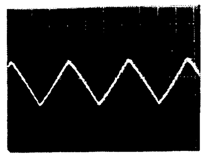
8. 1.0V/DIV 20µs/DIV



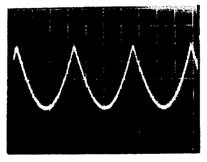
9. 1.0V/DIV 20µs/DIV



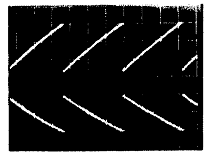
10. 0.5V/DIV 5ms/DIV



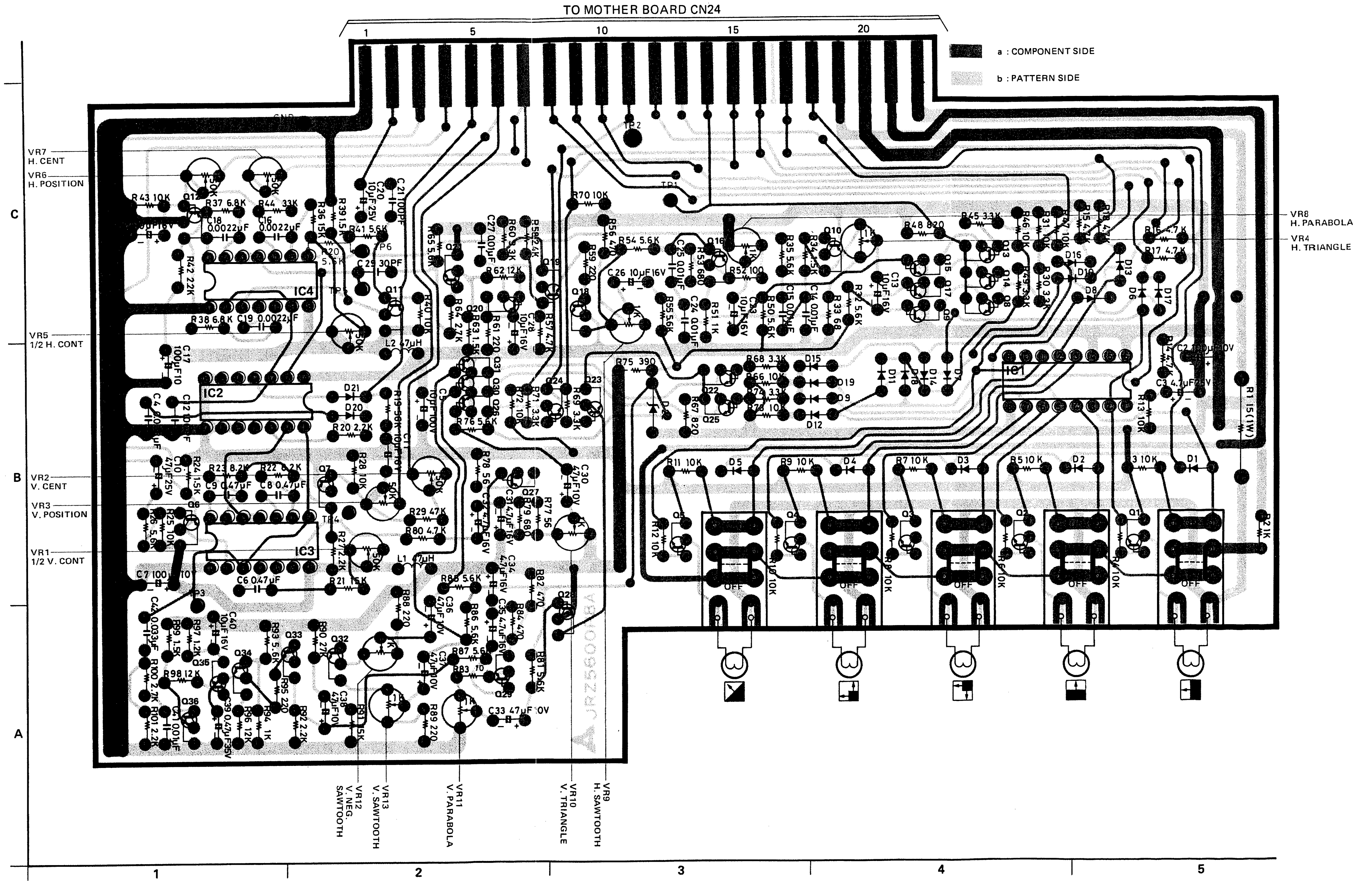
12. 0.2V/DIV 5ms/DIV



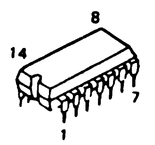
13. 0.5V/DIV 5ms/DIV



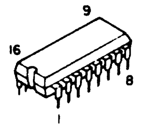
14. 0.5V/DIV 5ms/DIV


TO MOTHER BOARD CN24
1
5
10
15
20
a : COMPONENT SIDE
b : PATTERN SIDE
C
B
A
1
2
3
4
5
VR7 H. CENT
VR6 H. POSITION
VR5 1/2 H. CONT
VR2 V. CENT
VR3 V. POSITION
VR1 1/2 V. CONT
VR8 H. PARABOLA
VR4 H. TRIANGLE
VR12 V. NEG. SAWTOOTH
VR13 V. SAWTOOTH
VR11 V. PARABOLA
VR10 V. TRIANGLE
VR9 H. SAWTOOTH
GND
TP2
TP1
TP3
TP4
IC1
IC2
IC3
IC4
L1 47µH
L2 47µH
R1 15(1W)
OFF
JRZ5600BA

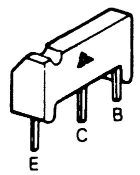
MC14077BP
DN850



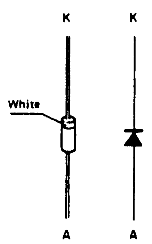
HD14174BP



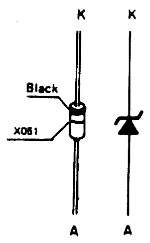
2SB641-RS
2SD636-RS
2SD639RS



MA165

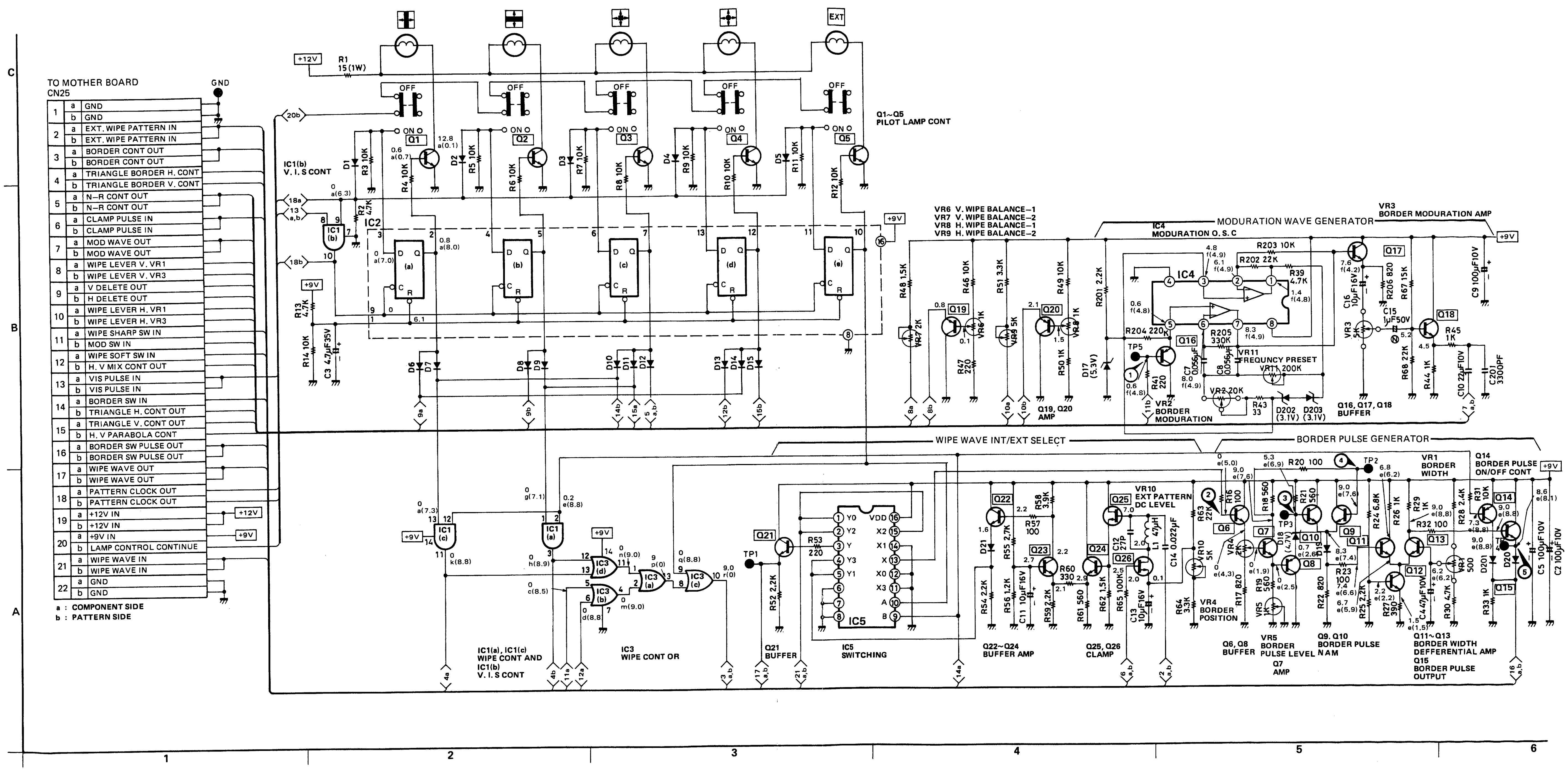


YUD-XZ051


K
K
Black
X051
A
A

IC1	HD14174BP	B4, B5	Q10	2SB641-RS	C4	Q23	2SD636-RS	B3	Q36	2SD636-RS	A1	D12	MA165	B4
IC2	MC14077BP	B1	Q11	2SB641-RS	C2	Q24	2SD636-RS	B3	D1	MA165	B5	D13	MA165	C5
IC3	DN850	B1	Q12	2SB641-RS	C1	Q25	2SD636-RS	B3	D2	MA165	B5	D14	MA165	B4
IC4	DN850	C1	Q13	2SD636-RS	C4	Q26	2SD636-RS	B2	D3	MA165	B4	D15	MA165	B4
Q1	2SD639RS	B5	Q14	2SD636-RS	C4	Q27	2SB641-RS	B2	D4	MA165	B4	D16	MA165	C5
Q2	2SD639RS	B4	Q15	2SD636-RS	C4	Q28	2SD636-RS	A3	D5	MA165	B3	D17	MA165	C5
Q3	2SD639RS	B4	Q16	2SB641-RS	C3	Q29	2SB641-RS	A2	D6	MA165	C5	D18	MA165	B4
Q4	2SD639RS	B3	Q17	2SD636-RS	C4	Q30	2SD636-RS	B2	D7	MA165	B4	D19	MA165	B4
Q5	2SD639RS	B3	Q18	2SD636-RS	C3	Q31	2SD636-RS	B2	D8	MA165	C5	D20	MA165	B2
Q6	2SB641-RS	B1	Q19	2SD636-RS	C3	Q32	2SD636-RS	A2	D9	MA165	B4	D21	MA165	B2
Q7	2SB641-RS	B2	Q20	2SB641-RS	C2	Q33	2SD636-RS	A1, A2	D10	MA165	C5	D22	YUD-XZ051	B3
Q8	2SD636-RS	C4	Q21	2SD636-RS	C2	Q34	2SD636-RS	A1	D11	MA165	B4			
Q9	2SD636-RS	C4	Q22	2SD636-RS	B3	Q35	2SB641-RS	A1						

SCHEMATIC DIAGRAM OF MODULATION BOARD


TO MOTHER BOARD
CN25
GND
1 a GND
1 b GND
2 a EXT. WIPE PATTERN IN
2 b EXT. WIPE PATTERN IN
3 a BORDER CONT OUT
3 b BORDER CONT OUT
4 a TRIANGLE BORDER H. CONT
4 b TRIANGLE BORDER V. CONT
5 a N-R CONT OUT
5 b N-R CONT OUT
6 a CLAMP PULSE IN
6 b CLAMP PULSE IN
7 a MOD WAVE OUT
7 b MOD WAVE OUT
8 a WIPE LEVER V. VR1
8 b WIPE LEVER V. VR3
9 a V DELETE OUT
9 b H DELETE OUT
10 a WIPE LEVER H. VR1
10 b WIPE LEVER H. VR3
11 a WIPE SHARP SW IN
11 b MOD SW IN
12 a WIPE SOFT SW IN
12 b H. V MIX CONT OUT
13 a VIS PULSE IN
13 b VIS PULSE IN
14 a BORDER SW IN
14 b TRIANGLE H. CONT OUT
15 a TRIANGLE V. CONT OUT
15 b H. V PARABOLA CONT
16 a BORDER SW PULSE OUT
16 b BORDER SW PULSE OUT
17 a WIPE WAVE OUT
17 b WIPE WAVE OUT
18 a PATTERN CLOCK OUT
18 b PATTERN CLOCK OUT
19 a +12V IN
19 b +12V IN
20 a +9V IN
20 b LAMP CONTROL CONTINUE
21 a WIPE WAVE IN
21 b WIPE WAVE IN
22 a GND
22 b GND
a : COMPONENT SIDE
b : PATTERN SIDE
+12V
R1 15(1W)
EXT
OFF
ON
Q1 Q2 Q3 Q4 Q5
Q1~Q5 PILOT LAMP CONT
IC1(b) V. I. S CONT
IC2
VR6 V. WIPE BALANCE-1
VR7 V. WIPE BALANCE-2
VR8 H. WIPE BALANCE-1
VR9 H. WIPE BALANCE-2
Q19, Q20 AMP
MODURATION WAVE GENERATOR
IC4 MODURATION O. S. C
VR3 BORDER MODURATION AMP
R203 10K
R202 22K
R39 4.7K
R204 220K
R205 330K
VR11 FREQUNCY PRESET
VR11 200K
VR2 20K
VR2 BORDER MODURATION
D202 D203 (3.1V) (3.1V)
Q16, Q17, Q18 BUFFER
+9V
WIPE WAVE INT/EXT SELECT
BORDER PULSE GENERATOR
VR1 BORDER WIDTH
Q14 BORDER PULSE ON/OFF CONT
VR10 EXT PATTERN DC LEVEL
TP1 TP2 TP3 TP5
IC1(a), IC1(c) WIPE CONT AND
IC1(b) V. I. S CONT
IC3 WIPE CONT OR
Q21 BUFFER
IC5 SWITCHING
Q22~Q24 BUFFER AMP
Q25, Q26 CLAMP
VR4 BORDER POSITION
Q6, Q8 BUFFER
VR5 BORDER PULSE LEVEL
Q7 AMP
Q9, Q10 BORDER PULSE NAM
Q11~Q13 BORDER WIDTH DEFFERENTIAL AMP
Q15 BORDER PULSE OUTPUT
A B C
1 2 3 4 5 6

Voltages are measured by following conditions

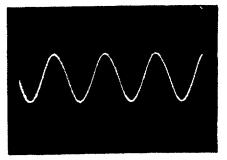
a( ) : ◫ ——→ ON
b( ) : ▣ ——→ ON
c( ) : SHARP WIPE ——→ ON
d( ) : SOFT WIPE ——→ ON
e( ) : BOARD WIPE ——→ ON
f( ) : MOD ——→ ON
g( ) : ⊟ or ▣ ——→ ON
h( ) : ⊟ or ▣ and BOARD WIPE ——→ ON
i( ) : (◫ or ▣ → ON) and (BOARD WIPE → OFF)

h( ) : ⊟ or ▣ and BOARD WIPE → ON
r( ) : (◫, ⊟, ▣ and EXT → OFF) and (BOARD WIPE → ON)
k( ) : ◫ and BOARD WIPE → ON
m( ) : SHARP WIPE or SOFT WIPE → ON
n( ) : (◫, ⊟ or ▣ → ON) and (BOARD WIPE → ON)
p( ) : (◫ ⊟ and ▣ → OFF) and (BOARD WIPE → ON)
q( ) : EXT → ON

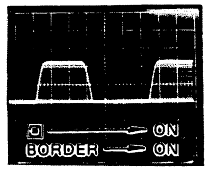
IC1	HD14081BP	A2, B2
IC2	HD14174BP	B2, B3
IC3	HD14071BP	A3
IC4	HA17555PS	B5
IC5	YWHD14052BP	A3, A4
Q1	2SD639RS	C2
Q2	2SD639RS	C2
Q3	2SD639RS	C3
Q4	2SD639RS	C4
Q5	2SD639RS	C5
Q6	2SD636-RS	A5
Q7	2SD636-RS	A5
Q8	2SB641-RS	A5
Q9	2SD636-RS	A5
Q10	2SD636-RS	A5
Q11	2SC1216F	A5
Q12	2SD636-RS	A5
Q13	2SC1216F	A5
Q14	2SB644-RS	A6
Q15	2SD636-RS	A6
Q16	2SD636-RS	B5
Q17	2SD636-RS	B5
Q18	2SD636-RS	B5
Q19	2SB641-RS	B4
Q20	2SB641-RS	B4
Q21	2SD636-RS	A3
Q22	2SD636-RS	A4
Q23	2SD636-RS	A4
Q24	2SD636-RS	A4
Q25	2SK19-Y	A4
Q26	2SK34-CD	A4
D1	MA165	C2
D2	MA165	C2
D3	MA165	C2
D4	MA165	C3
D5	MA165	C3
D6	MA165	B2
D7	MA165	B2
D8	MA165	B2
D9	MA165	B2
D10	MA165	B3
D11	MA165	B3
D12	MA165	B3
D13	MA165	B3
D14	MA165	B3
D15	MA165	B3
D17	XZ053	B4
D18	MA4047L	A5
D19	MA165	A5
D20	MA165	A6
D201	MA27A	A4
D202	XZ031	B5
D203	XZ031	B5

CONDUTOR VIEW OF MODULATION BOARD

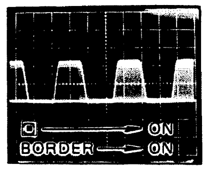
1. 1.0V/DIV 5ms/DIV



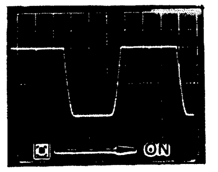
2. 2.0V/DIV 10µs/DIV



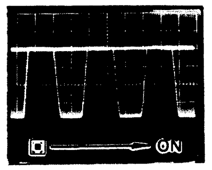
2. 2.0V/DIV 5ms/DIV



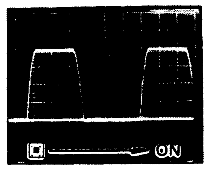
3. 0.5V/DIV 10µs/DIV



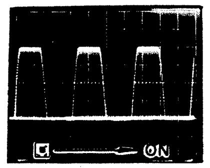
3. 0.5V/DIV 5ms/DIV



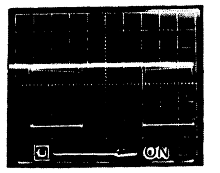
4. 0.5V/DIV 10µs/DIV



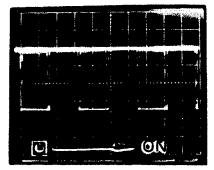
4. 0.5V/DIV 5ms/DIV

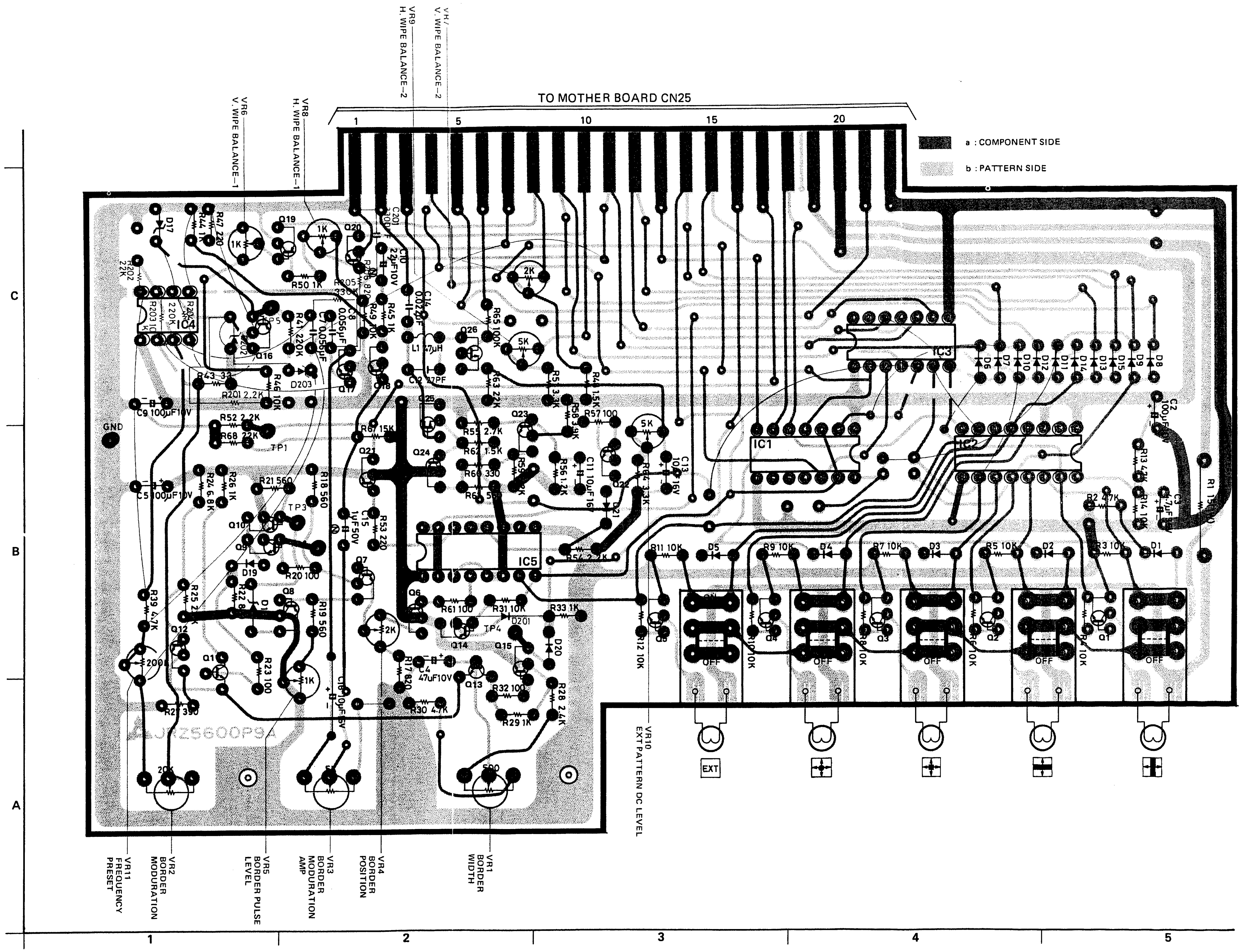


5. 1.0V/DIV 10µs/DIV

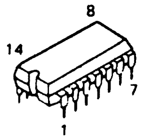


5. 1.0V/DIV 5ms/DIV

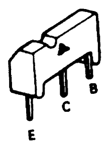



VR9— H. WIPE BALANCE—2
VR7— V. WIPE BALANCE—2
VR6— V. WIPE BALANCE—1
VR8— H. WIPE BALANCE—1
TO MOTHER BOARD CN25
1
5
10
15
20
a : COMPONENT SIDE
b : PATTERN SIDE
C
B
A
GND
IC1
IC2
IC3
IC4
IC5
TP1
TP3
TP4
EXT
OFF
AJRZ5600P9A
VR11 FREQUENCY PRESET
VR2 BORDER MODURATION
VR5 BORDER PULSE LEVEL
VR3 BORDER MODURATION AMP
VR4 BORDER POSITION
VR1 BORDER WIDTH
VR10 EXT PATTERN DC LEVEL
1
2
3
4
5

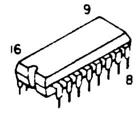
HD14071BP
HD14081BP



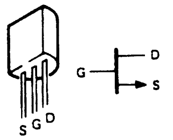
2SB641-RS
2SB644-RS
2SD636-RS
2SD639RS



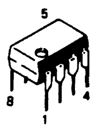
HD14174BP
YWHD14052BP



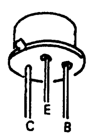
2SK34-CD



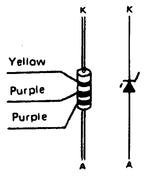
NJM4558D



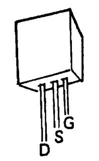
2SC1216F



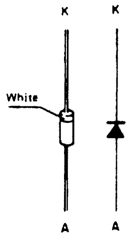
MA4047L


K
K
Yellow
Purple
Purple
A
A

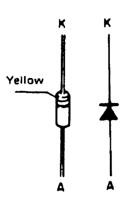
2SK19-Y



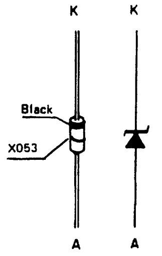
MA165



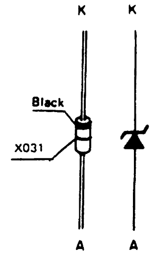
MA27A


K
K
Yellow
A
A

XZ053


K
K
Black
X053
A
A

XZ031


K
K
Black
X031
A
A

IC1	HD14081BP	B3, B4
IC2	HD14174BP	B4, B5
IC3	HD14071BP	C4
IC4	NJM4558D	C1
IC5	YWHD14052BP	B2
Q1	2SD639RS	B5
Q2	2SD639RS	B4
Q3	2SD639RS	B4
Q4	2SD639RS	B3
Q5	2SD639RS	B3
Q6	2SD636-RS	B2
Q7	2SD636-RS	B2
Q8	2SB641-RS	B2
Q9	2SD636-RS	B1
Q10	2SD636-RS	B1
Q11	2SC1216F	B1
Q12	2SD636-RS	B1
Q13	2SC1216F	A2
Q14	2SB644-RS	B2
Q15	2SD636-RS	B2
Q16	2SB641-RS	C1
Q17	2SD636-RS	C2
Q18	2SD636-RS	C2
Q19	2SB641-RS	C1
Q20	2SB641-RS	C2
Q21	2SD636-RS	B2
Q22	2SD636-RS	B3
Q23	2SD636-RS	B2
Q24	2SD636-RS	B2
Q25	2SK19-Y	C2
Q26	2SK34-CD	C2
D1	MA165	B5
D2	MA165	B5
D3	MA165	B4
D4	MA165	B4
D5	MA165	B3
D6	MA165	C4
D7	MA165	C4
D8	MA165	C5
D9	MA165	C5
D10	MA165	C4
D11	MA165	C5
D12	MA165	C4
D13	MA165	C5
D14	MA165	C5
D15	MA165	C5
D17	XZ031	C1
D18	MA4047L	B1
D19	MA165	B1
D20	MA165	B3
D21	MA27A	B3
D201	MA27A	B2
D202	XZ031	C1
D203	XZ031	C2

SCHEMATIC DIAGRAM OF LEVER BOARD/POSITION–1 BOARD/POSITION–2 BOARD

LEVER BOARD

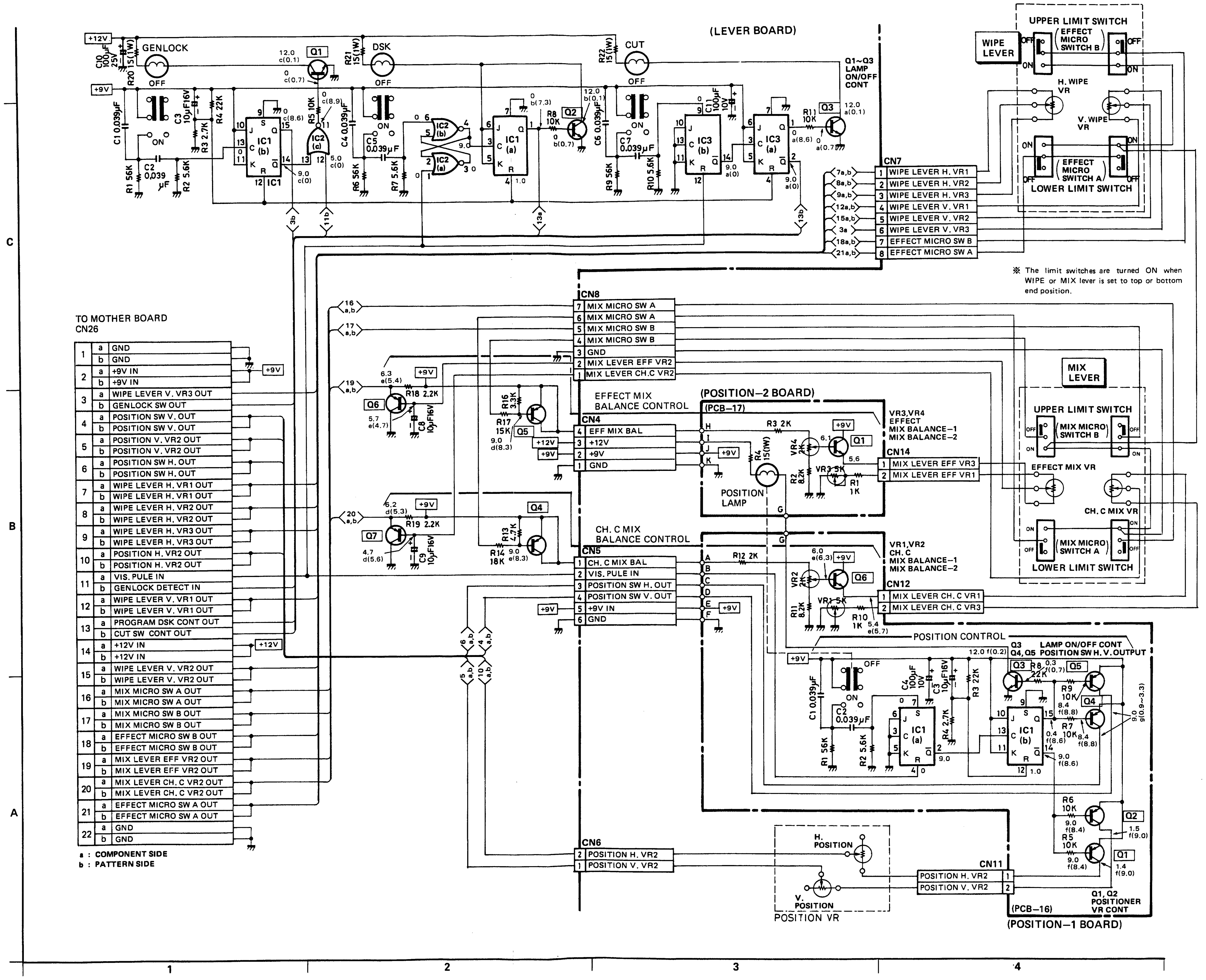
IC1	HD14027BP	C1, C2
IC2	YWHD14001BP	C2
IC3	HD14027BP	C3
Q1	2SD639RS	D2
Q2	2SD639RS	C2
Q3	2SD639RS	C3
Q4	2SB641-RS	B2
Q5	2SB641-RS	B2
Q6	2SB641-RS	B2
Q7	2SB641-RS	B2

POSITION-1 BOARD

IC1	HD14027BP	A4
Q1	2SB644-RS	A4
Q2	2SB644-RS	A4
Q3	2SD639RS	A4
Q4	2SB644-RS	A4
Q5	2SB644-RS	A4
Q6	2SD636-RS	B3

POSITION-2 BOARD

Q1	2SD636-RS	B3


(LEVER BOARD)
GENLOCK
DSK
CUT
OFF
ON
+12V
+9V
Q1~Q3 LAMP ON/OFF CONT
UPPER LIMIT SWITCH
WIPE LEVER
EFFECT MICRO SWITCH B
H. WIPE VR
V. WIPE VR
EFFECT MICRO SWITCH A
LOWER LIMIT SWITCH
CN7
1 WIPE LEVER H. VR1
2 WIPE LEVER H. VR2
3 WIPE LEVER H. VR3
4 WIPE LEVER V. VR1
5 WIPE LEVER V. VR2
6 WIPE LEVER V. VR3
7 EFFECT MICRO SW B
8 EFFECT MICRO SW A
※ The limit switches are turned ON when WIPE or MIX lever is set to top or bottom end position.
TO MOTHER BOARD CN26
1 a GND
1 b GND
2 a +9V IN
2 b +9V IN
3 a WIPE LEVER V. VR3 OUT
3 b GENLOCK SW OUT
4 a POSITION SW V. OUT
4 b POSITION SW V. OUT
5 a POSITION V. VR2 OUT
5 b POSITION V. VR2 OUT
6 a POSITION SW H. OUT
6 b POSITION SW H. OUT
7 a WIPE LEVER H. VR1 OUT
7 b WIPE LEVER H. VR1 OUT
8 a WIPE LEVER H. VR2 OUT
8 b WIPE LEVER H. VR2 OUT
9 a WIPE LEVER H. VR3 OUT
9 b WIPE LEVER H. VR3 OUT
10 a POSITION H. VR2 OUT
10 b POSITION H. VR2 OUT
11 a VIS. PULE IN
11 b GENLOCK DETECT IN
12 a WIPE LEVER V. VR1 OUT
12 b WIPE LEVER V. VR1 OUT
13 a PROGRAM DSK CONT OUT
13 b CUT SW CONT OUT
14 a +12V IN
14 b +12V IN
15 a WIPE LEVER V. VR2 OUT
15 b WIPE LEVER V. VR2 OUT
16 a MIX MICRO SW A OUT
16 b MIX MICRO SW A OUT
17 a MIX MICRO SW B OUT
17 b MIX MICRO SW B OUT
18 a EFFECT MICRO SW B OUT
18 b EFFECT MICRO SW B OUT
19 a MIX LEVER EFF VR2 OUT
19 b MIX LEVER EFF VR2 OUT
20 a MIX LEVER CH. C VR2 OUT
20 b MIX LEVER CH. C VR2 OUT
21 a EFFECT MICRO SW A OUT
21 b EFFECT MICRO SW A OUT
22 a GND
22 b GND
a : COMPONENT SIDE
b : PATTERN SIDE
CN8
7 MIX MICRO SW A
6 MIX MICRO SW A
5 MIX MICRO SW B
4 MIX MICRO SW B
3 GND
2 MIX LEVER EFF VR2
1 MIX LEVER CH.C VR2
MIX LEVER
UPPER LIMIT SWITCH
MIX MICRO SWITCH B
EFFECT MIX VR
CH. C MIX VR
MIX MICRO SWITCH A
LOWER LIMIT SWITCH
EFFECT MIX BALANCE CONTROL
(POSITION–2 BOARD)
(PCB–17)
CN4
4 EFF MIX BAL
3 +12V
2 +9V
1 GND
VR3,VR4 EFFECT MIX BALANCE–1 MIX BALANCE–2
CN14
1 MIX LEVER EFF VR3
2 MIX LEVER EFF VR1
POSITION LAMP
CH. C MIX BALANCE CONTROL
CN5
1 CH. C MIX BAL
2 VIS. PULE IN
3 POSITION SW H. OUT
4 POSITION SW V. OUT
5 +9V IN
6 GND
VR1,VR2 CH. C MIX BALANCE–1 MIX BALANCE–2
CN12
1 MIX LEVER CH. C VR1
2 MIX LEVER CH. C VR3
POSITION CONTROL
Q3 LAMP ON/OFF CONT
Q4, Q5 POSITION SW H. V. OUTPUT
CN6
2 POSITION H. VR2
1 POSITION V. VR2
H. POSITION
V. POSITION
POSITION VR
CN11
POSITION H. VR2 1
POSITION V. VR2 2
Q1, Q2 POSITIONER VR CONT
(PCB–16)
(POSITION–1 BOARD)
C
B
A
1
2
3
4

Voltages are measured by following conditions

a( ) : [CUT] ⟶ ON

b( ) : [DSK] ⟶ ON

c( ) : [GEN LOCK] ⟶ ON

d( ) : MIX LEVER ⟶ TOP

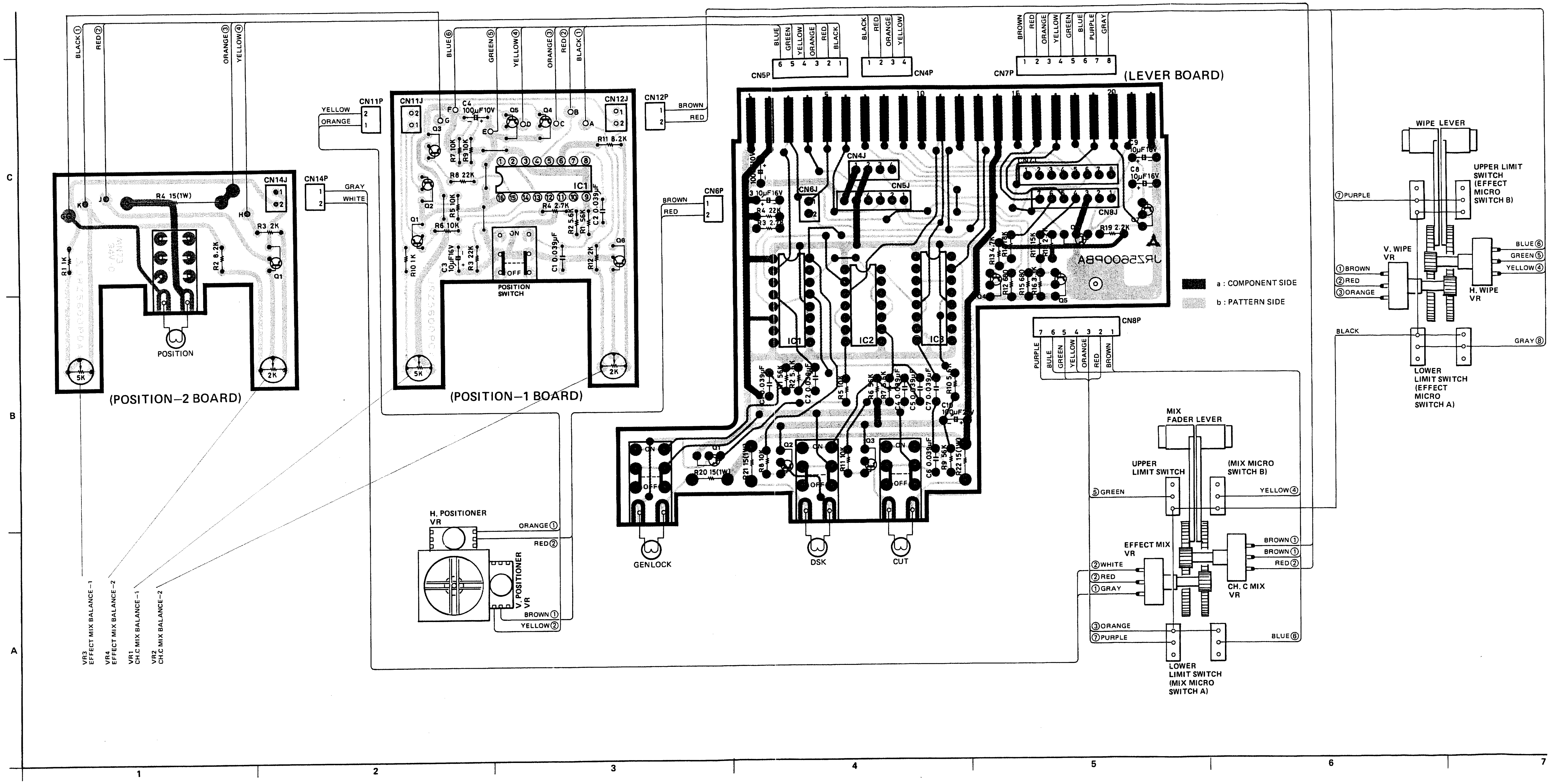
e( ) : MIX LEVER ⟶ BOTTOM

f( ) : [POSI] ⟶ ON

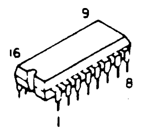
g( ) : ([POSI] → ON) and (POSI LEVER → CHANGE)

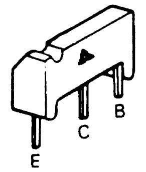
h( ) : GENLOCK ⟶ IN

CONDUCTOR VIEW OF LEVER BOARD/POSITION−1 BOARD/POSITION−2 BOARD



(LEVER BOARD)
(POSITION−1 BOARD)
(POSITION−2 BOARD)
CN4P
CN5P
CN6P
CN7P
CN8P
CN11P
CN11J
CN12P
CN12J
CN14P
CN14J
CN4J
CN5J
CN6J
CN7J
CN8J
IC1
IC2
IC3
POSITION SWITCH
POSITION
GENLOCK
DSK
CUT
ON
OFF
H. POSITIONER VR
V. POSITIONER VR
WIPE LEVER
UPPER LIMIT SWITCH (EFFECT MICRO SWITCH B)
LOWER LIMIT SWITCH (EFFECT MICRO SWITCH A)
V. WIPE VR
H. WIPE VR
MIX FADER LEVER
UPPER LIMIT SWITCH
(MIX MICRO SWITCH B)
EFFECT MIX VR
CH. C MIX VR
LOWER LIMIT SWITCH (MIX MICRO SWITCH A)
VR3 EFFECT MIX BALANCE−1
VR4 EFFECT MIX BALANCE−2
VR1 CH.C MIX BALANCE−1
VR2 CH.C MIX BALANCE−2
a : COMPONENT SIDE
b : PATTERN SIDE
JR25600PBA
BLACK①
RED②
ORANGE③
YELLOW④
GREEN⑤
BLUE⑥
PURPLE⑦
GRAY⑧
BROWN①
WHITE
R4 15(1W)
R3 2K
R2 8.2K
R1 1K
C4 100μF10V
R11 8.2K
R8 22K
R7 10K
R9 10K
R5 10K
R6 10K
R4 2.7K
R2 5.6K
R1 56K
C2 0.039μF
C1 0.039μF
C3 10μF16V
R3 22K
R10 1K
R12 2K
C9 10μF10V
C8 10μF16V
R19 2.2K
R20 15(1W)
R21 15(1W)
R22 15(1W)
5K
2K
1
2
3
4
5
6
7
A
B
C


HD14001BP
HD14027BP


2SB641-RS 2SB644-RS
2SD636-RS 2SD639-RS

LEVER BOARD

IC1	HD14027BP	B4
IC2	YWHD14001BP	B4
IC3	HD14027BP	B4
Q1	2SD639RS	B3
Q2	2SD639RS	B4
Q3	2SD639RS	B4
Q4	2SB641-RS	C5
Q5	2SB641-RS	C5
Q6	2SB641-RS	C5
Q7	2SB641-RS	C5

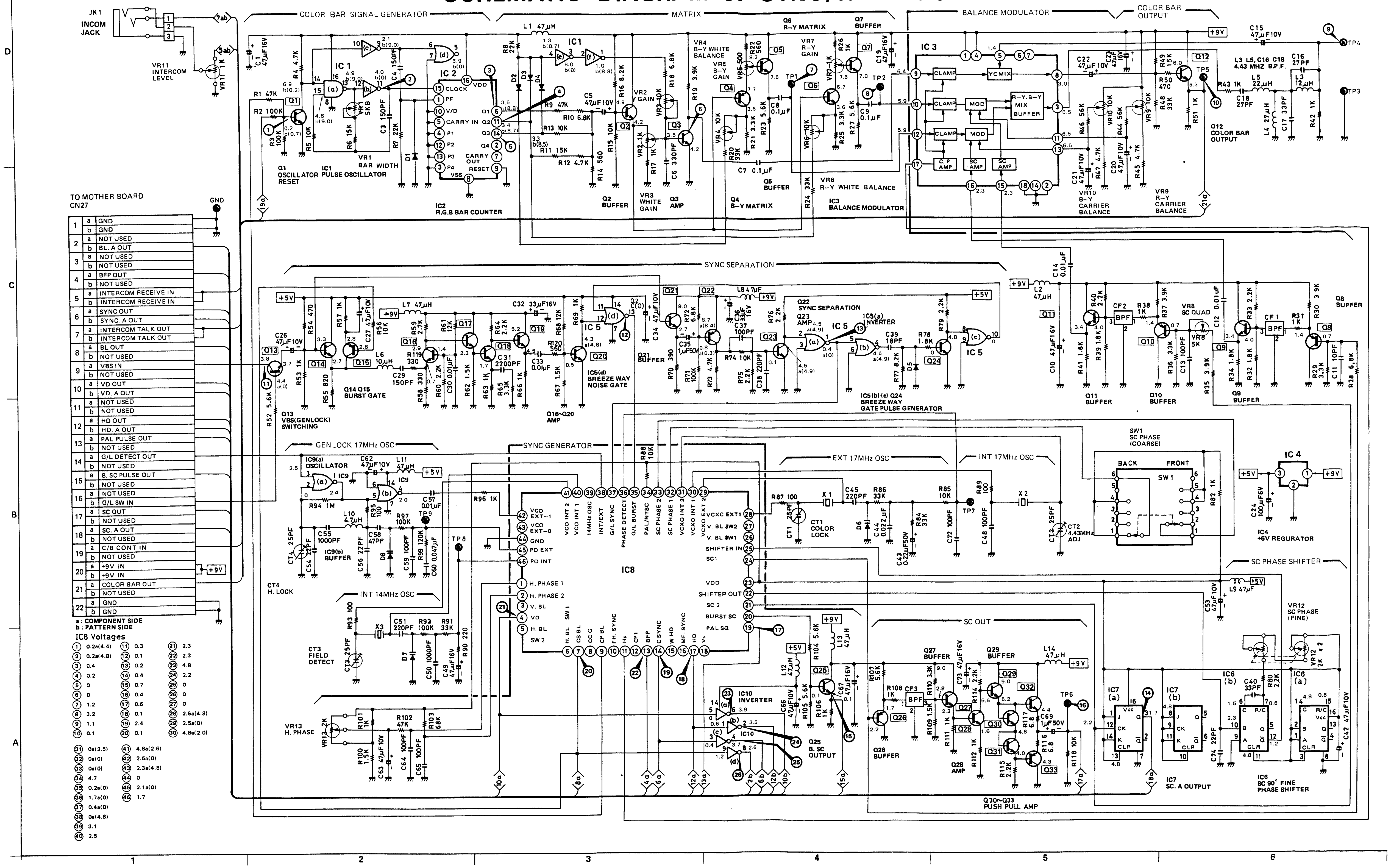
POSITION-1 BOARD

IC1	HD14027BP	C3
Q1	2SB644-RS	C2
Q2	2SB644-RS	C2
Q3	2SD639RS	C2
Q4	2SB644-RS	C3
Q5	2SB644-RS	C3
Q6	2SD636-RS	C3

POSITION-2 BOARD

Q1	2SD636-RS	C2

SCHEMATIC DIAGRAM OF SYNC,C/BAR BOARD


JK1 INCOM JACK
VR11 INTERCOM LEVEL
COLOR BAR SIGNAL GENERATOR
MATRIX
BALANCE MODULATOR
COLOR BAR OUTPUT
Q1 OSCILLATOR RESET
IC1 PULSE OSCILLATOR
VR1 BAR WIDTH
IC2 R.G.B BAR COUNTER
Q2 BUFFER
VR2 GAIN
VR3 WHITE GAIN
Q3 AMP
VR4 B-Y WHITE BALANCE
VR5 B-Y GAIN
Q4 B-Y MATRIX
Q5 BUFFER
Q6 R-Y MATRIX
Q7 BUFFER
VR6 R-Y WHITE BALANCE
VR7 R-Y GAIN
IC3 BALANCE MODULATOR
CLAMP
YCMIX
MOD
R-Y, B-Y MIX BUFFER
C.P AMP
SC AMP
VR10 B-Y CARRIER BALANCE
VR9 R-Y CARRIER BALANCE
Q12 COLOR BAR OUTPUT
L3 L5, C16 C18 4.43 MHZ B.P.F.
TP1
TP2
TP3
TP4
TP5
TO MOTHER BOARD CN27
GND
SYNC SEPARATION
Q13 VBS(GENLOCK) SWITCHING
Q14 Q15 BURST GATE
Q16~Q20 AMP
IC5(d) BREEZE WAY NOISE GATE
Q21 BUFFER
Q22 SYNC SEPARATION
Q23 AMP
IC5(a) INVERTER
IC5(b)(c) Q24 BREEZE WAY GATE PULSE GENERATOR
Q8 BUFFER
Q9 BUFFER
Q10 BUFFER
Q11 BUFFER
VR8 SC QUAD
CF1 BPF
CF2 BPF
GENLOCK 17MHz OSC
IC9(a) OSCILLATOR
IC9(b) BUFFER
CT4 H. LOCK
INT 14MHz OSC
CT3 FIELD DETECT
VR13 H. PHASE
SYNC GENERATOR
IC8
EXT 17MHz OSC
CT1 COLOR LOCK
INT 17MHz OSC
CT2 4.43MHz ADJ
SW1 SC PHASE (COARSE)
BACK
FRONT
IC4 +5V REGURATOR
SC PHASE SHIFTER
VR12 SC PHASE (FINE)
IC10 INVERTER
Q25 B.SC OUTPUT
SC OUT
Q26 BUFFER
Q27 BUFFER
Q28 AMP
Q29 BUFFER
Q30~Q33 PUSH PULL AMP
TP6
TP7
TP8
TP9
IC7 SC. A OUTPUT
IC6 SC 90° FINE PHASE SHIFTER
+5V
+9V
1
2
3
4
5
6
A
B
C
D

TO MOTHER BOARD
CN27

1	a	GND
	b	GND
2	a	NOT USED
	b	BL. A OUT
3	a	NOT USED
	b	NOT USED
4	a	BFP OUT
	b	NOT USED
5	a	INTERCOM RECEIVE IN
	b	INTERCOM RECEIVE IN
6	a	SYNC OUT
	b	SYNC. A OUT
7	a	INTERCOM TALK OUT
	b	INTERCOM TALK OUT
8	a	BL OUT
	b	NOT USED
9	a	VBS IN
	b	NOT USED
10	a	VD OUT
	b	VD. A OUT
11	a	NOT USED
	b	NOT USED
12	a	HD OUT
	b	HD. A OUT
13	a	PAL PULSE OUT
	b	NOT USED
14	a	G/L DETECT OUT
	b	NOT USED
15	a	B. SC PULSE OUT
	b	NOT USED
16	a	NOT USED
	b	G/L SW IN
17	a	SC OUT
	b	NOT USED
18	a	SC. A OUT
	b	NOT USED
19	a	C/B CONT IN
	b	NOT USED
20	a	+9V IN
	b	+9V IN
21	a	COLOR BAR OUT
	b	NOT USED
22	a	GND
	b	GND

a : COMPONENT SIDE
b : PATTERN SIDE

IC8 Voltages

①	0.2a(4.4)	⑪	0.3	㉑	2.3
②	0.2a(4.8)	⑫	0.1	㉒	2.3
③	0.4	⑬	0.2	㉓	4.8
④	0.2	⑭	0.4	㉔	2.2
⑤	0	⑮	0.7	㉕	0
⑥	0	⑯	0.4	㉖	0
⑦	1.2	⑰	0.6	㉗	0
⑧	3.2	⑱	0.1	㉘	2.6a(4.8)
⑨	1.1	⑲	2.4	㉙	2.5a(0)
⑩	0.1	⑳	0.1	㉚	4.8a(2.0)
㉛	0a(2.5)	㊶	4.8a(2.6)		
㉜	0a(0)	㊷	2.5a(0)		
㉝	0a(0)	㊸	2.3a(4.8)		
㉞	4.7	㊹	0		
㉟	0.2a(0)	㊺	2.1a(0)		
㊱	1.7a(0)	㊻	1.7		
㊲	0.4a(0)				
㊳	0a(4.8)				
㊴	3.1				
㊵	2.5				

Voltages are measured by following conditions

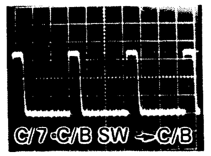
a ( ) : NORM ——→ ON

b ( ) : C/7. C/B SW ——→ C/7

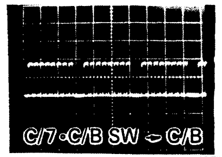
IC1	HD14572UBP	D2, D3	Q4	2SD636-RS	D4	Q17	2SD636-RS	C2	Q30	2SD636-RS	A5
IC2	YWHD14516BP	D2, D3	Q5	2SD636-RS	D4	Q18	2SD636-RS	C3	Q31	2SD636-RS	A5
IC3	HA11720	D5	Q6	2SD636-RS	D4	Q19	2SD636-RS	C3	Q32	2SD636-RS	A5
IC4	AN78N05	B6	Q7	2SD636-RS	D4	Q20	2SC641K-C	C3	Q33	2SB641-RS	A5
IC5	TC40H002P	C4, C5	Q8	2SB641-RS	C6	Q21	2SD636-RS	C3	D1	MA165	D2
IC6	YWHD74LS221P	A6	Q9	2SD636-RS	C6	Q22	2SB641-RS	C4	D2	MA165	D3
IC7	YWHD74LS107P	A5, A6	Q10	2SB641-RS	C6	Q23	2SC641K-C	C4	D3	MA165	D3
IC8	MP7260	B3	Q11	2SD636-RS	C5	Q24	2SD636-RS	C5	D4	MA165	D3
IC9	TC40H002P	B2	Q12	2SD636-RS	D6	Q25	2SD636-RS	A4	D5	MA165	C4
IC10	YWHD74LS04P	A4	Q13	2SD636-RS	C2	Q26	2SB641-RS	A4	D6	YUD1S2688	B4
Q1	2SC641K-C	D2	Q14	2SD636-RS	C2	Q27	2SD636-RS	A5	D7	YUD1S2688	A2
Q2	2SD636-RS	D3	Q15	2SB641-RS	C2	Q28	2SD636-RS	A5	D8	YUD1S2688	B2
Q3	2SB641-RS	D3	Q16	2SD636-RS	C2	Q29	2SD636-RS	A5			

CONDUCTOR VIEW OF SYNC,C/BAR BOARD

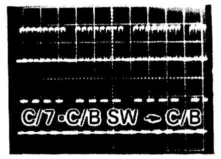
1. 0.2V/DIV 20µs/DIV



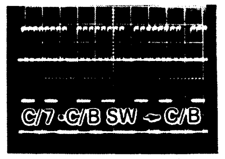
2. 5.0V/DIV 20µs/DIV



2. 5.0V/DIV 20µs/DIV



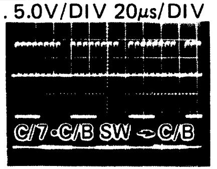
2. 5.0V/DIV 20µs/DIV



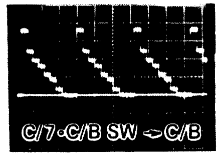
3. 5.0V/DIV 20µs/DIV

4. 5.0V/DIV 20µs/DIV

2. 5.0V/DIV 20µs/DIV

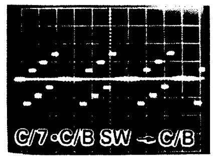


6. 0.2V/DIV 20µs/DIV

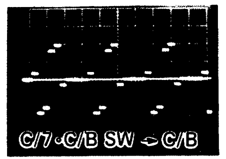


5. 5.0V/DIV 20µs/DIV

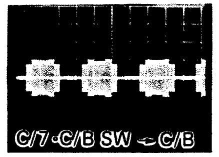
7. 0.1V/DIV 20µs/DIV



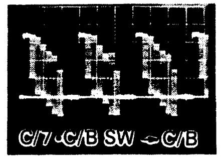
8. 0.1V/DIV 20µs/DIV



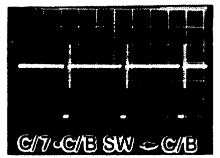
9. 0.1V/DIV 20µs/DIV



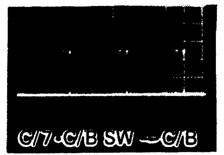
10. 0.2V/DIV 20µs/DIV



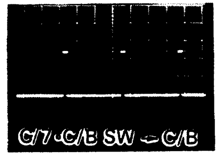
11. 0.5V/DIV 20µs/DIV



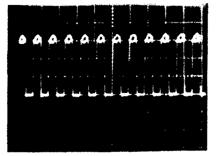
12. 2.0V/DIV 20µs/DIV



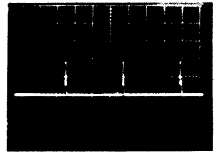
13. 2.0V/DIV 20µs/DIV



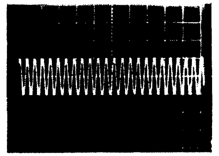
14. 1.0V/DIV 0.5µs/DIV



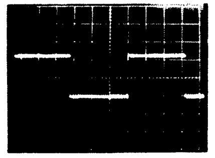
15. 1.0V/DIV 20µs/DIV



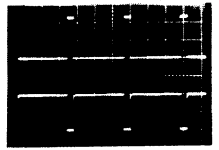
16. 2.0V/DIV 0.5µs/DIV



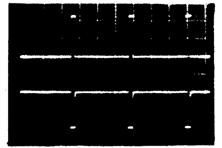
17. 2.0V/DIV 20µs/DIV



18. 2.0V/DIV 20µs/DIV



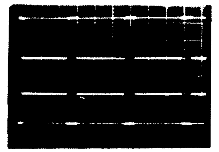
19. 2.0V/DIV 20µs/DIV



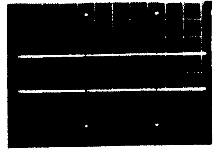
24. 2.0V/DIV 20µs/DIV

25. 2.0V/DIV 20µs/DIV

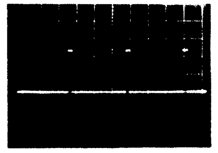
20. 2.0V/DIV 20µs/DIV



21. 2.0V/DIV 5ms/DIV

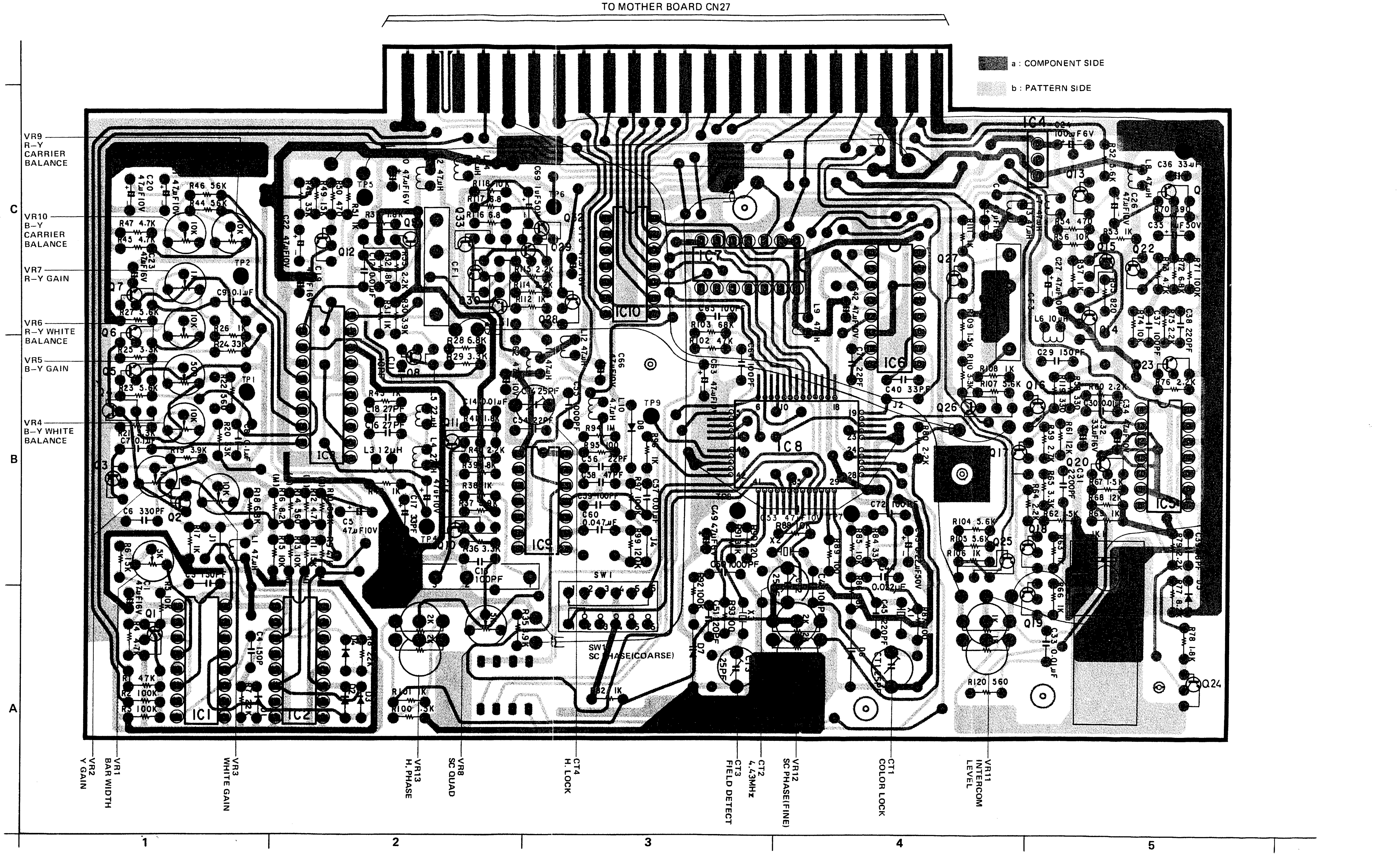


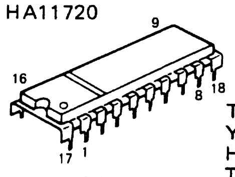
22. 2.0V/DIV 20µs/DIV

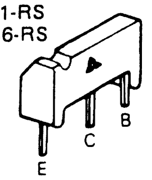


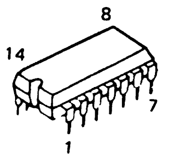
26. 2.0V/DIV 20µs/DIV

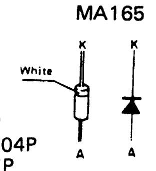
23. 2.0V/DIV 5ms/DIV

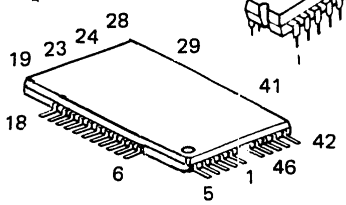

TO MOTHER BOARD CN27
a : COMPONENT SIDE
b : PATTERN SIDE
VR9 R–Y CARRIER BALANCE
VR10 B–Y CARRIER BALANCE
VR7 R–Y GAIN
VR6 R–Y WHITE BALANCE
VR5 B–Y GAIN
VR4 B–Y WHITE BALANCE
C
B
A
VR2 Y GAIN
VR1 BAR WIDTH
VR3 WHITE GAIN
VR13 H. PHASE
VR8 SC QUAD
CT4 H. LOCK
CT3 FIELD DETECT
CT2 4.43MHz
VR12 SC PHASE(FINE)
CT1 COLOR LOCK
VR11 INTERCOM LEVEL
SW1 SC PHASE(COARSE)
IC1
IC2
IC3
IC4
IC5
IC6
IC7
IC8
IC9
IC10
TP1
TP2
TP4
TP5
TP6
TP9
1
2
3
4
5

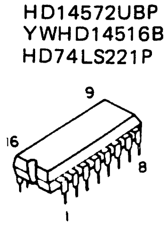

HA11720
9
16
18
8
17
1

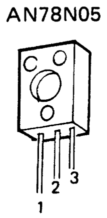

2SB641-RS
2SD636-RS
E
C
B


TC40H002P
YWHD74LS04P
HD74LS107P
TC40H002P
14
8
7
1

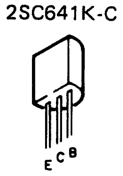

MA165
White
K
K
A
A

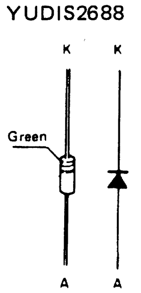

MP7260
19
23
24
28
29
41
18
42
6
5
1
46


HD14572UBP
YWHD14516BP
HD74LS221P
9
16
8
1


AN78N05
1
2
3

1 : IN PUT
2 : COM MON
3 : OUT PUT


2SC641K-C
E
C
B


YUDIS2688
K
K
Green
A
A

IC1	HD14572UBP	A1
IC2	YWHD14516BP	A2
IC3	HA11720	B2
IC4	AN78N05	C5
IC5	TC40H002P	B5
IC6	YWHD74LS221P	B4, C4
IC7	YWHD74LS107P	C3
IC8	MP7260	B3, B4
IC9	TC40H002P	B3
IC10	YWHD74LS04P	C3
Q1	2SC641K-C	A1
Q2	2SD636-RS	D1
Q3	2SB641-RS	D1
Q4	2SD636-RS	D1
Q5	2SD636-RS	D1
Q6	2SD636-RS	C1
Q7	2SD636-RS	C1
Q8	2SB641-RS	B2
Q9	2SD636-RS	C2
Q10	2SB641-RS	B2
Q11	2SD636-RS	B2
Q12	2SD636-RS	C2
Q13	2SD636-RS	C5
Q14	2SD636-RS	C5
Q15	2SB641-RS	C5
Q16	2SD636-RS	B5
Q17	2SD636-RS	B4
Q18	2SD636-RS	B5
Q19	2SD636-RS	A5
Q20	2SC641K-C	B5
Q21	2SD636-RS	C5
Q22	2SB641-RS	C5
Q23	2SC641K-C	B5
Q24	2SD636-RS	A5
Q25	2SD636-RS	B4
Q26	2SB641-RS	B4
Q27	2SD636-RS	C4
Q28	2SD636-RS	C3
Q29	2SD636-RS	C3
Q30	2SD636-RS	C2
Q31	2SD636-RS	C2
Q32	2SD636-RS	C3
Q33	2SB641-RS	C2
D1	MA165	A1
D2	MA165	A2
D3	MA165	A2
D4	MA165	A2
D5	MA165	A5
D6	YUD1S2688	A4
D7	YUD1S2688	A3
D8	YUD1S2688	B3

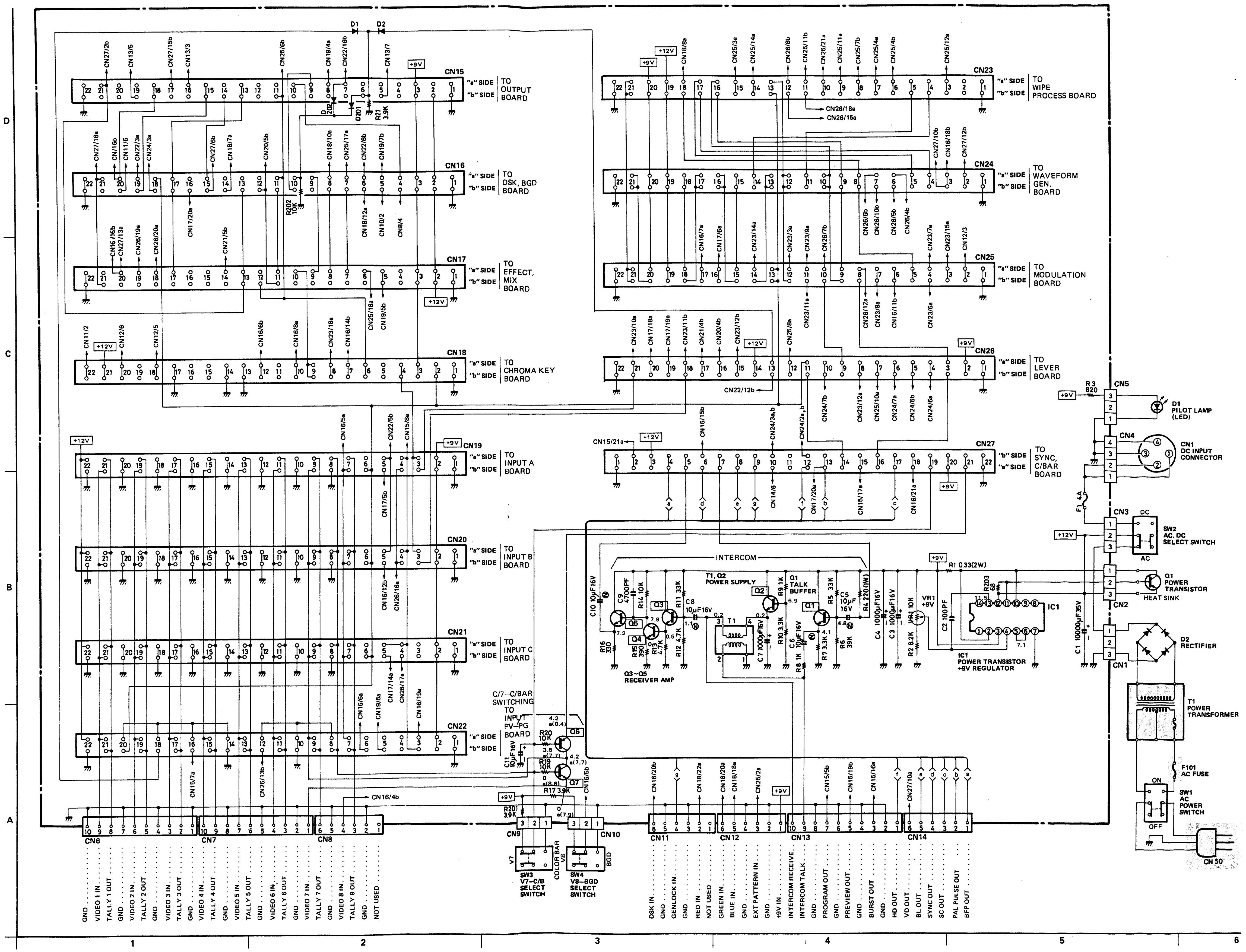
SCHEMATIC DIAGRAM OF MOTHER BOARD

SPECIAL EFFECTS GENERATOR MISCELLANEOUS

Q1	2SA837-PQ	B5
D1	LN21RPH	C5
D2	S15VB20	B5

MOTHER BOARD

IC	HA17723G	B5
Q1	2SD636-RS	B4
Q2	2SC1226-QR	B4
Q3	2SD636-RS	B3
Q4	2SD636-RS	B3
Q5	2SD636-RS	B3
Q6	2SA1254-BC	A3
Q7	2SC2377CD	A3
D1	MA150	D2
D2	MA150	D2
D201	MA162	D2
D202	MA162	D2


CN15 "a" SIDE "b" SIDE TO OUTPUT BOARD
CN16 "a" SIDE "b" SIDE TO DSK, BGD BOARD
CN17 "a" SIDE "b" SIDE TO EFFECT, MIX BOARD
CN18 "a" SIDE "b" SIDE TO CHROMA KEY BOARD
CN19 "a" SIDE "b" SIDE TO INPUT A BOARD
CN20 "a" SIDE "b" SIDE TO INPUT B BOARD
CN21 "a" SIDE "b" SIDE TO INPUT C BOARD
CN22 "a" SIDE "b" SIDE
C/7–C/BAR SWITCHING TO INPUT PV–PG BOARD
CN23 "a" SIDE "b" SIDE TO WIPE PROCESS BOARD
CN24 "a" SIDE "b" SIDE TO WAVEFORM GEN. BOARD
CN25 "a" SIDE "b" SIDE TO MODULATION BOARD
CN26 "a" SIDE "b" SIDE TO LEVER BOARD
CN27 "b" SIDE "a" SIDE TO SYNC, C/BAR BOARD
D1 D2 D201 D202 R202 10K R21 3.5K
+12V +9V
INTERCOM
T1, Q2 POWER SUPPLY
Q1 TALK BUFFER
Q3–Q5 RECEIVER AMP
IC1 POWER TRANSISTOR +9V REGULATOR
R1 0.33(2W)
CN5 D1 PILOT LAMP (LED)
R3 820
CN4 CN1 DC INPUT CONNECTOR
F1 4A
CN3 DC AC SW2 AC, DC SELECT SWITCH
Q1 POWER TRANSISTOR HEAT SINK
CN2
C1 1000µF35V
D2 RECTIFIER
CN1
T1 POWER TRANSFORMER
F101 AC FUSE
ON OFF SW1 AC POWER SWITCH
CN50
Q6 Q7 R20 10K R19 10K R17 3.9K R201 3.9K
CN9 CN10
SW3 V7–C/B SELECT SWITCH
SW4 V8–BGD SELECT SWITCH
V7 COLOR BAR V8 BGD
CN6 CN7 CN8
GND
VIDEO 1 IN
TALLY 1 OUT
GND
VIDEO 2 IN
TALLY 2 OUT
GND
VIDEO 3 IN
TALLY 3 OUT
GND
VIDEO 4 IN
TALLY 4 OUT
GND
VIDEO 5 IN
TALLY 5 OUT
GND
VIDEO 6 IN
TALLY 6 OUT
GND
VIDEO 7 IN
TALLY 7 OUT
GND
VIDEO 8 IN
TALLY 8 OUT
GND
NOT USED
CN11 CN12 CN13 CN14
DSK IN
GND
GENLOCK IN
GND
RED IN
NOT USED
GREEN IN
BLUE IN
GND
EXT PATTERN IN
GND
+9V IN
INTERCOM RECEIVE
INTERCOM TALK
GND
PROGRAM OUT
GND
PREVIEW OUT
GND
BURST OUT
GND
HD OUT
VD OUT
BL OUT
SYNC OUT
SC OUT
PAL PULSE OUT
BFP OUT
A B C D
1 2 3 4 5 6

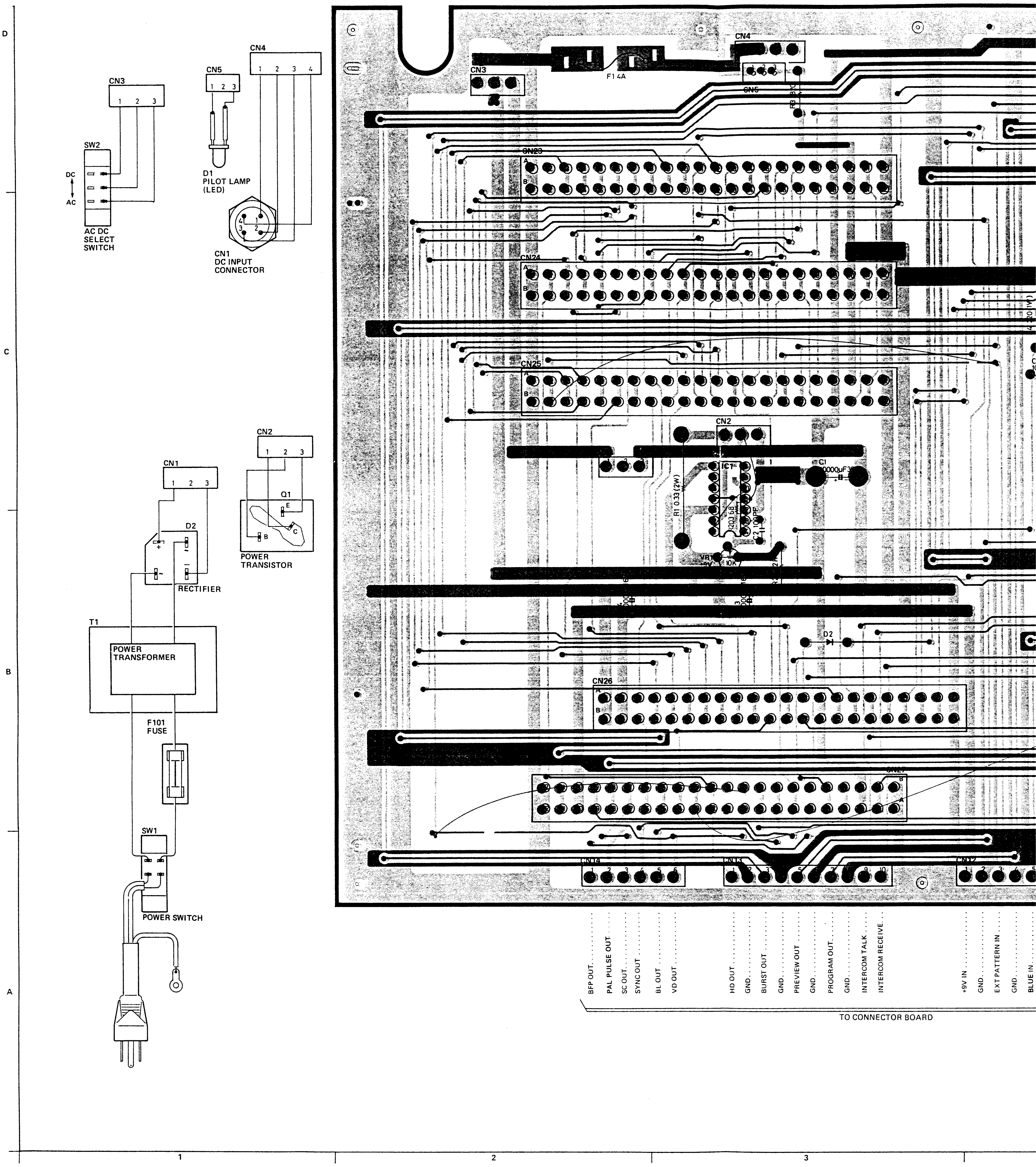
Voltages are measured by following conditions

a( ) : C/7, COLOR BAR SELECTOR → C/7

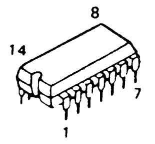
PRODUCT SAFETY NOTE

The shaded area on this schematic diagram incorporates special features important for protection from X-Radiation, fire and electrical shock hazards. When servicing it is essential that only manufacturer's specified parts be used for the critical components in the shaded areas of the schematic.

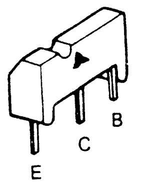
Peuvoit V11047


D
C
B
A
1
2
3
CN3
1 2 3
SW2
DC
AC
AC DC
SELECT
SWITCH
CN5
1 2 3
D1
PILOT LAMP
(LED)
CN4
1 2 3 4
CN1
DC INPUT
CONNECTOR
CN2
1 2 3
Q1
E
B
C
POWER
TRANSISTOR
CN1
1 2 3
D2
RECTIFIER
T1
POWER
TRANSFORMER
F101
FUSE
SW1
POWER SWITCH
CN4
F1 4A
CN3
CN5
CN23
CN24
CN25
CN2
IC1
C1
R1 0.33 (2W)
VR1
10K
D2
CN26
CN27
CN14
CN13
CN12
BFP OUT
PAL PULSE OUT
SC OUT
SYNC OUT
BL OUT
VD OUT
HD OUT
GND
BURST OUT
GND
PREVIEW OUT
GND
PROGRAM OUT
GND
INTERCOM TALK
INTERCOM RECEIVE
+9V IN
GND
EXT PATTERN IN
GND
BLUE IN
TO CONNECTOR BOARD

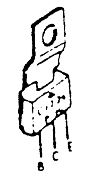
HA17723G



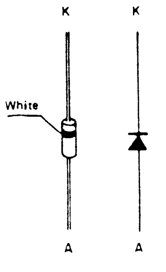
2SA1254-BC
2SC2377CD
2SD636-RS



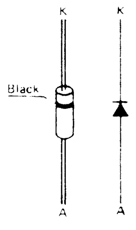
2SC1226-QR



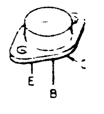
MA150



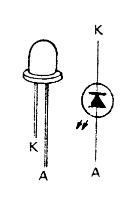
MA162



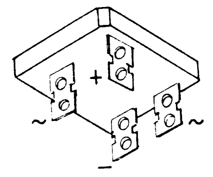
2SA837-PQ



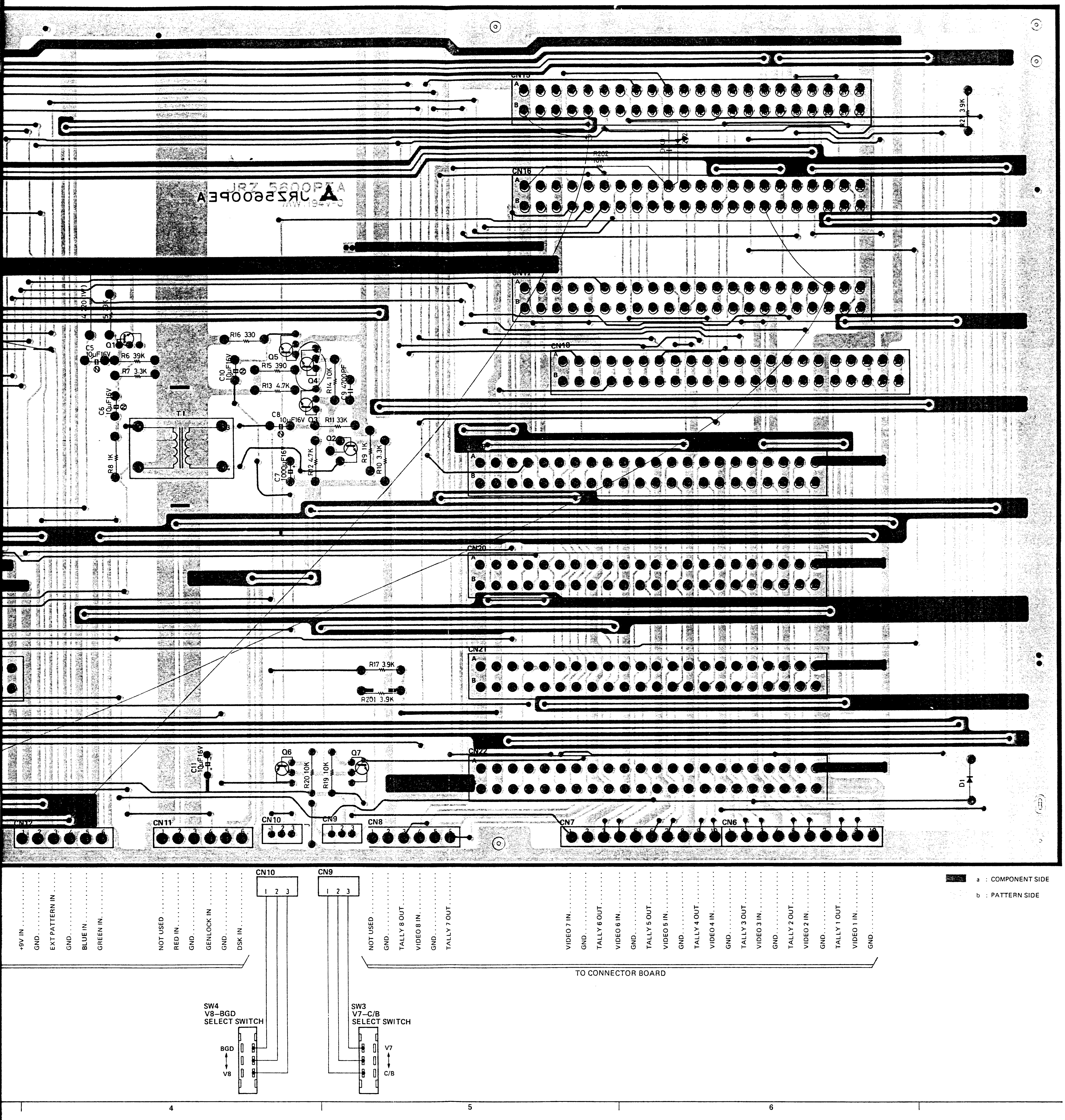
LN21RPH



S15VB20



EW OF MOTHER BOARD


CN15
CN16
CN17
CN18
CN19
CN20
CN21
CN22
A
B
R2 3.9K
R202 10K
D201
D202
JRZ560OPEA
C5 10μF16V
Q1
R6 39K
R7 3.3K
C6 10μF16V
R8 1K
T1
R16 330
C10 10μF16V
Q5
R15 390
R13 4.7K
Q4
R14 10K
C9 4700PF
C8 10μF16V
Q3
R11 33K
Q2
C7 100μF16V
R12 4.7K
R9 1K
R10 3.3K
R17 3.9K
R201 3.9K
C11 10μF16V
Q6
R20 10K
R19 10K
Q7
D1
CN12
CN11
CN10
CN9
CN8
CN7
CN6
1
2
3
4
5
6
7
8
9
10
+9V IN
GND
EXT PATTERN IN
GND
BLUE IN
GREEN IN
NOT USED
RED IN
GND
GENLOCK IN
GND
DSK IN
NOT USED
GND
TALLY 8 OUT
VIDEO 8 IN
GND
TALLY 7 OUT
VIDEO 7 IN
GND
TALLY 6 OUT
VIDEO 6 IN
GND
TALLY 5 OUT
VIDEO 5 IN
GND
TALLY 4 OUT
VIDEO 4 IN
GND
TALLY 3 OUT
VIDEO 3 IN
GND
TALLY 2 OUT
VIDEO 2 IN
GND
TALLY 1 OUT
VIDEO 1 IN
GND
TO CONNECTOR BOARD
SW4
V8–BGD
SELECT SWITCH
BGD
V8
SW3
V7–C/B
SELECT SWITCH
V7
C/B
a : COMPONENT SIDE
b : PATTERN SIDE
4
5
6

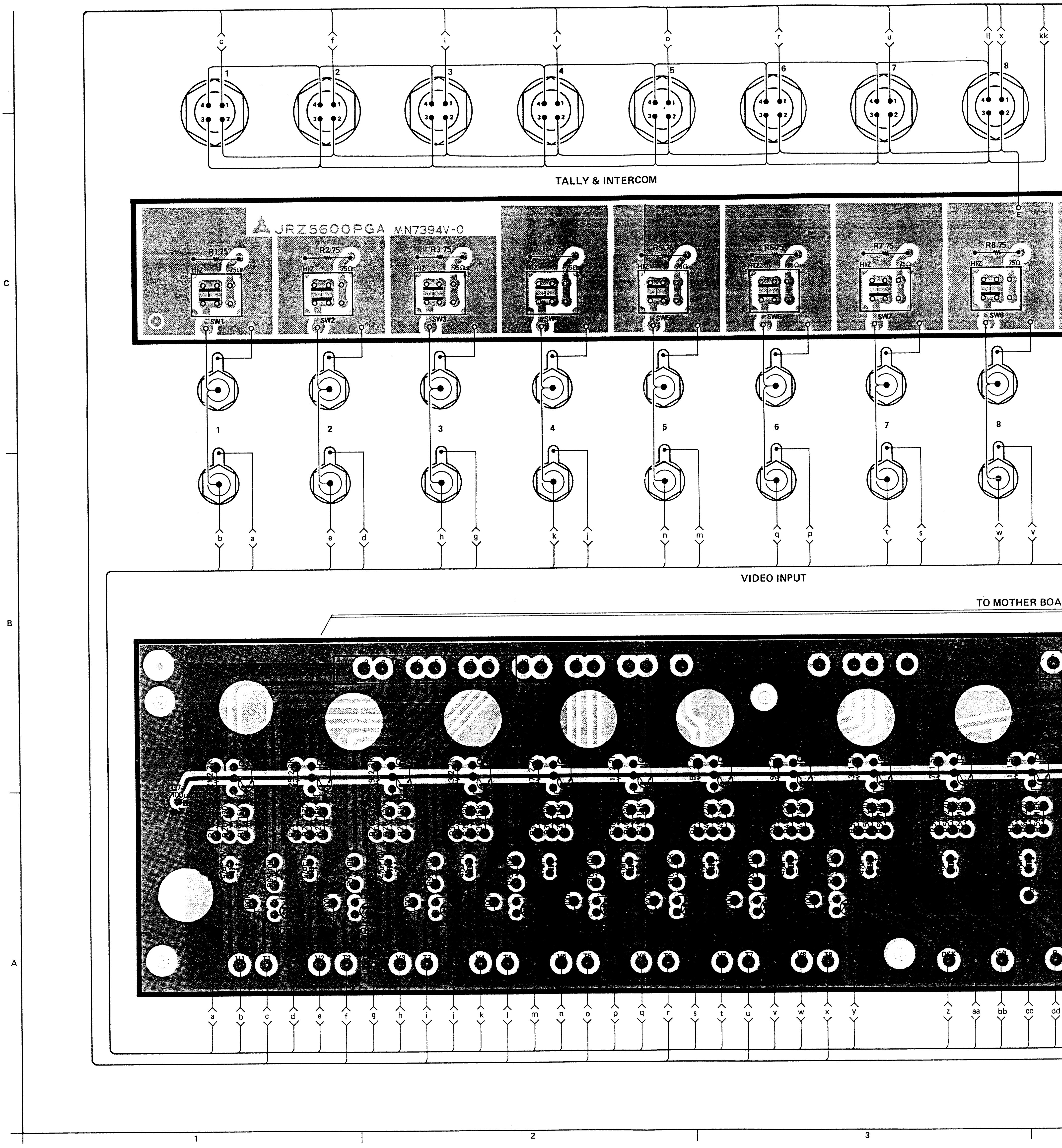
SPECIAL EFFECTS GENERATOR MISCELLANEOUS

Q1	2SA837-PQ	B1
D1	LN21RPH	B7
D2	S15VB20	B3

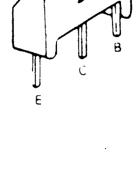
MOTHER BOARD

IC	HA17723G	C3	Q7	2SC2377CD	B5
Q1	2SD636-RS	C4	D1	MA150	B7
Q2	2SC1226-QR	C5	D2	MA150	B3
Q3	2SD636-RS	C4	D201	MA162	D6
Q4	2SD636-RS	C4	D202	MA162	D6
Q5	2SD636-RS	C4			
Q6	2SA1254-BC	B4			

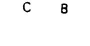
CONDUCTOR VIEW OF CONNEC


TALLY & INTERCOM
VIDEO INPUT
TO MOTHER BOA
JRZ5600PGA MN7394V-0
R1 75
R2 75
R3 75
R4 75
R5 75
R6 75
R7 75
R8 75
HiZ
75Ω
SW1
SW2
SW3
SW4
SW5
SW6
SW7
SW8
1
2
3
4
5
6
7
8
c
f
i
l
o
r
u
ll
x
kk
E
b
a
e
d
h
g
k
j
n
m
q
p
t
s
w
v
a
b
c
d
e
f
g
h
i
j
k
l
m
n
o
p
q
r
s
t
u
v
w
x
y
z
aa
bb
cc
dd
C
B
A
1
2
3

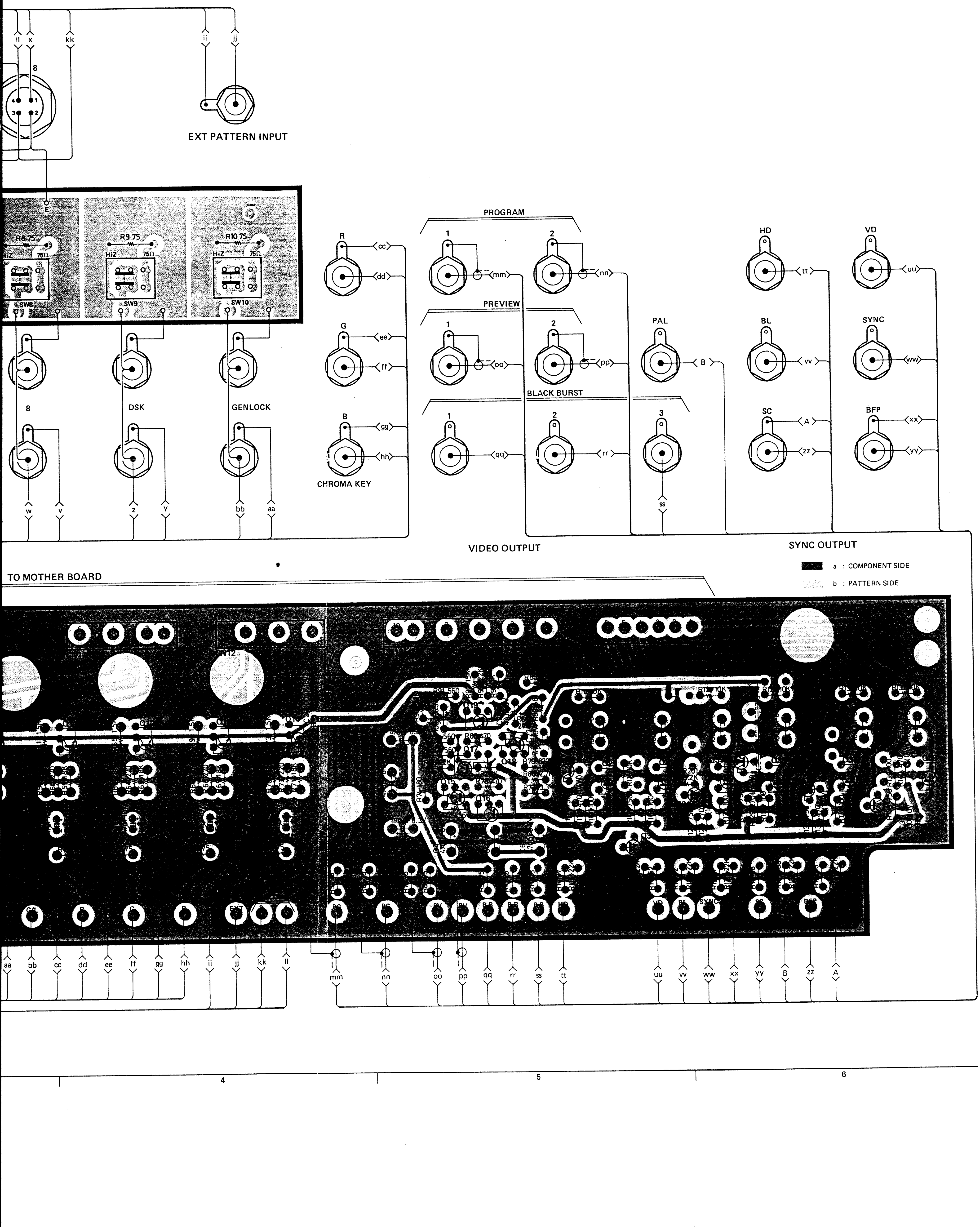
2SB644-RS
2SD636-RS
2SD639RS



2SC1216F

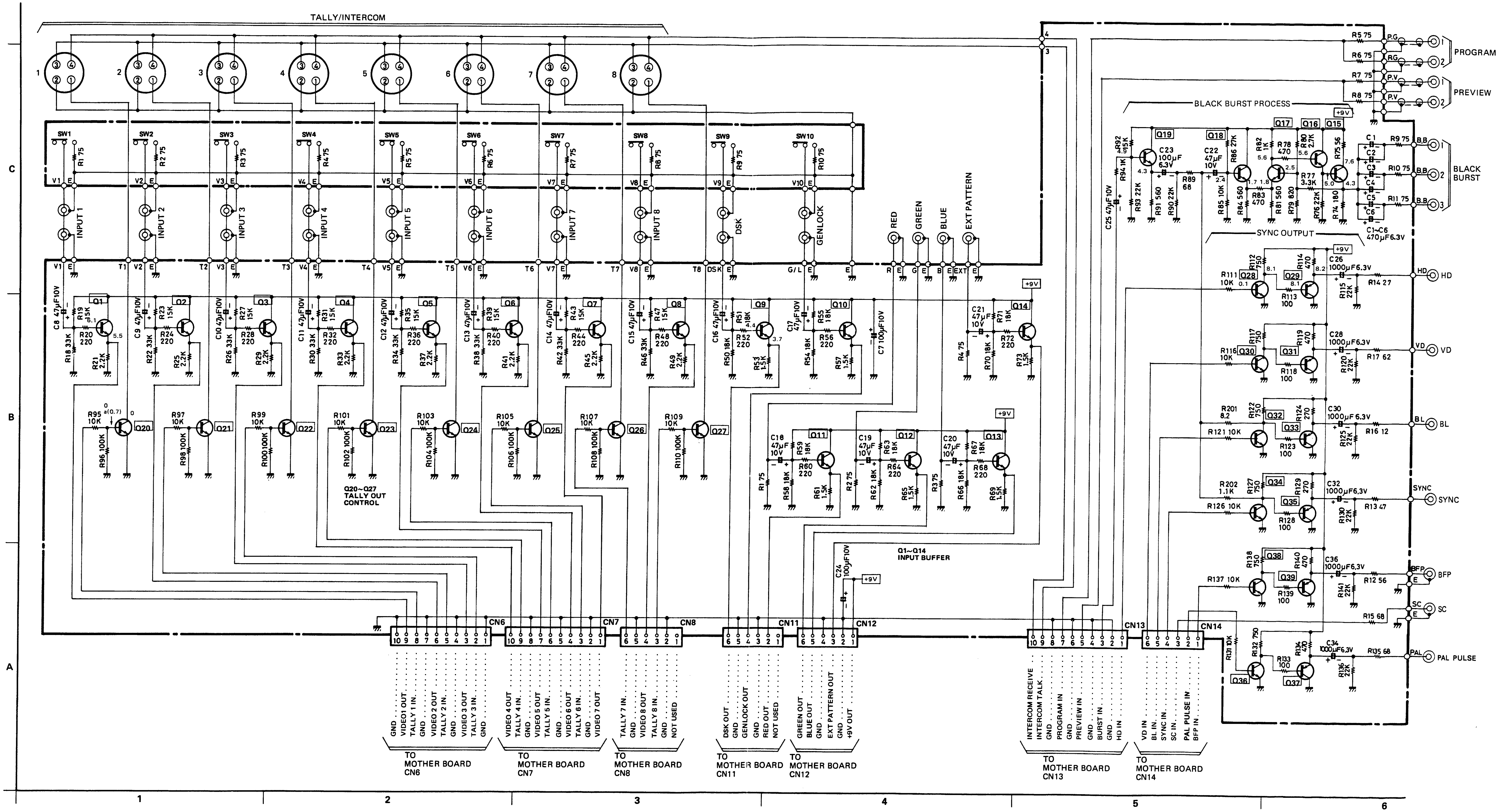


CONNECTOR BOARD/TERMINATION BOARD


EXT PATTERN INPUT
R8 75
R9 75
R10 75
HiZ
75Ω
SW8
SW9
SW10
8
DSK
GENLOCK
R
G
B
CHROMA KEY
PROGRAM
PREVIEW
BLACK BURST
PAL
HD
VD
BL
SYNC
SC
BFP
VIDEO OUTPUT
SYNC OUTPUT
TO MOTHER BOARD
a : COMPONENT SIDE
b : PATTERN SIDE
4
5
6

Q1	2SD636-RS	B1	Q9	2SD636-RS	B3	Q16	2SD636-RS	A5	Q23	2SD639RS	A2	Q30	2SC1216F	A5
Q2	2SD636-RS	B1	Q10	2SD636-RS	B3	Q17	2SD636-RS	A5	Q24	2SD639RS	A2	Q31	2SB644-RS	A5
Q3	2SD636-RS	B2	Q11	2SD636-RS	B4	Q18	2SD636-RS	B5	Q25	2SD639RS	A2	Q32	2SC1216F	A5
Q4	2SD636-RS	B2	Q12	2SD636-RS	B4	Q19	2SD639RS	B5	Q26	2SD639RS	A3	Q33	2SB644-RS	A6
Q5	2SD636-RS	B2	Q13	2SD636-RS	B4	Q20	2SD639RS	A1	Q27	2SD639RS	A3	Q34	2SC1216F	A6
Q6	2SD636-RS	B2	Q14	2SD636-RS	B4	Q21	2SD639RS	A2	Q28	2SC1216F	A5	Q35	2SB644-RS	A6
Q7	2SD636-RS	B3	Q15	2SD636-RS	A5	Q22	2SD639RS	A2	Q29	2SB644-RS	A5	Q38	2SC1216F	A6
Q8	2SD636-RS	B3										Q39	2SB644RS	A6

SCHEMATIC DIAGRAM OF CONNECTOR BOARD/TERMINATION BOARD


TALLY/INTERCOM
SW1 SW2 SW3 SW4 SW5 SW6 SW7 SW8 SW9 SW10
INPUT 1
INPUT 2
INPUT 3
INPUT 4
INPUT 5
INPUT 6
INPUT 7
INPUT 8
DSK
GENLOCK
RED
GREEN
BLUE
EXT PATTERN
PROGRAM
PREVIEW
BLACK BURST PROCESS
BLACK BURST
SYNC OUTPUT
C1~C6 470μF6.3V
HD
VD
BL
SYNC
BFP
SC
PAL PULSE
Q20~Q27 TALLY OUT CONTROL
Q1~Q14 INPUT BUFFER
CN6
GND
VIDEO1 OUT
TALLY 1 IN.
GND
VIDEO 2 OUT
TALLY 2 IN.
GND
VIDEO 3 OUT
TALLY 3 IN.
GND
TO MOTHER BOARD CN6
CN7
VIDEO 4 OUT
TALLY 4 IN.
GND
VIDEO 5 OUT
TALLY 5 IN.
GND
VIDEO 6 OUT
TALLY 6 IN.
GND
VIDEO 7 OUT
TO MOTHER BOARD CN7
CN8
TALLY 7 IN.
GND
VIDEO 8 OUT
TALLY 8 IN.
GND
NOT USED
TO MOTHER BOARD CN8
CN11
DSK OUT
GND
GENLOCK OUT
GND
RED OUT
NOT USED
TO MOTHER BOARD CN11
CN12
GREEN OUT
BLUE OUT
GND
EXT PATTERN OUT
GND
+9V OUT
TO MOTHER BOARD CN12
CN13
INTERCOM RECEIVE
INTERCOM TALK
GND
PROGRAM IN
GND
PREVIEW IN
GND
BURST IN
GND
HD IN
TO MOTHER BOARD CN13
CN14
VD IN
BL IN.
SYNC IN.
SC IN.
PAL PULSE IN
BFP IN.
TO MOTHER BOARD CN14
A
B
C
1
2
3
4
5
6

Voltages are measured by following conditions

a( ) : ☐ ——————→ ON

Q1	2SD636-RS	B1	Q9	2SD636-RS	B4	Q17	2SD636-RS	C6	Q25	2SD639RS	B3	Q33	2SB644-RS	B6
Q2	2SD636-RS	B1	Q10	2SD636-RS	B4	Q18	2SD636-RS	C5	Q26	2SD639RS	B3	Q34	2SC1216F	B5
Q3	2SD636-RS	B1	Q11	2SD636-RS	B4	Q19	2SD639RS	C5	Q27	2SD639RS	B3	Q35	2SB644-RS	B6
Q4	2SD636-RS	B2	Q12	2SD636-RS	B4	Q20	2SD639RS	B1	Q28	2SC1216F	C5	Q38	2SC1216F	A5
Q5	2SD636-RS	B2	Q13	2SD636-RS	B4	Q21	2SD639RS	B1	Q29	2SB644-RS	C6	Q39	2SB644RS	A6
Q6	2SD636-RS	B3	Q14	2SD636-RS	B5	Q22	2SD639RS	B2	Q30	2SC1216F	B5			
Q7	2SD636-RS	B3	Q15	2SD636-RS	C6	Q23	2SD639RS	B2	Q31	2SB644-RS	B6			
Q8	2SD636-RS	B3	Q16	2SD636-RS	C6	Q24	2SD639RS	B2	Q32	2SC1216F	B5			

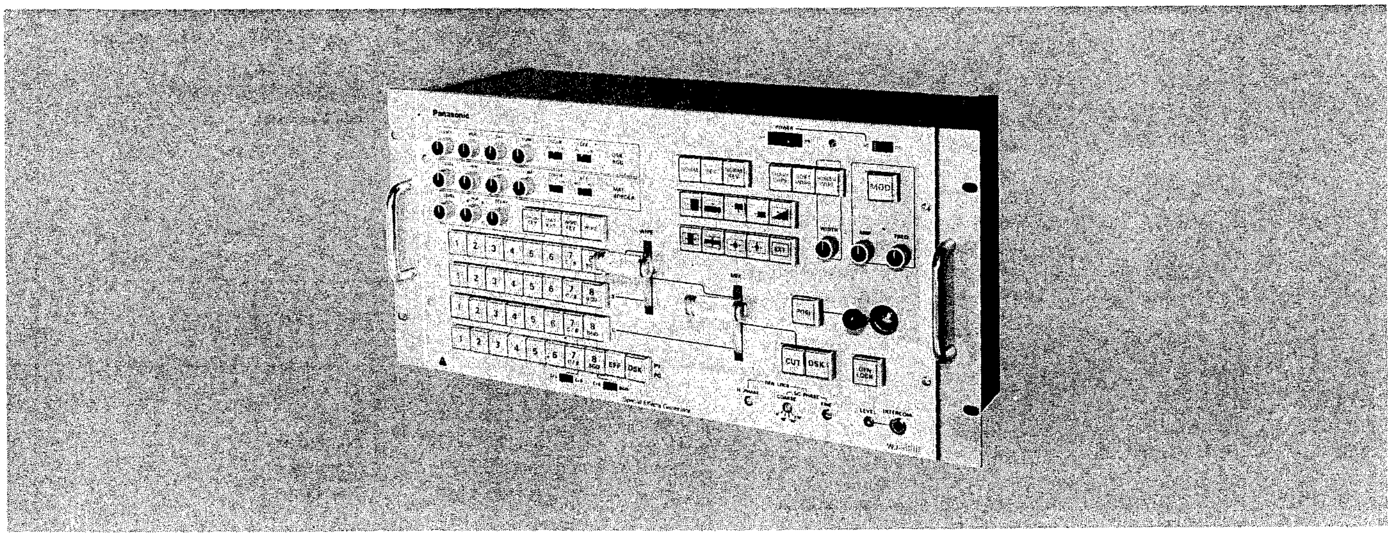
ORDER NO. VKD84040819C8

Service Manual

Vol. 4

Replacement Parts List
Exploded View

Special Effects Generator
WJ-5600



CONTENTS

PARTS LIST

Special Effects Generator 1
Miscellaneous 1
Output Board .... 1~4
DSK, BGD Board .... 4~6
Effect, Mix Board .... 6~9
Input A Board 9
Input B Board 9
Input C Board 9
Input PV-PG Board .... 9~10
Wipe Process Board .... 10~11
Waveform Gen Board .... 11~12
Modulation Board .... 12~13
Sync. C/Bar Board .... 13~15
Chroma Key Board .... 15~16
Delay Board 16
Level Board 16
Lever Board .... 16~17
Position-1 Board 17
Position-2 Board 17
Mother Board .... 17~18
Connector Board .... 18~19
Terminal Board 19
Accessory Parts/Packaging Parts 19

EXPLODED VIEW

Special Effects Generator .... 20~21
Packaging .... 20~21

Panasonic

Matsushita Electric Trading Co., Ltd.
P.O. Box 288, Central Osaka Japan

REPLACEMENT PARTS LIST

Important Notice

1. Components identified by ⚠ mark have special characteristics important for safety.
   When replacing any of these components, use only manufacturer's specified parts.
2. Components identified by *mark are new parts used from this model.
3. Complete printed circuit board assembly is not available as replacement part.

MODEL WJ-5600

SPECIAL EFFECTS GENERATOR MISCELLANEOUS

SYMBOL NO.	PART NO.	DESCRIPTION
Q1	2SA837-PQ	Transistor
D1	LN21RPH	LED (Red)
D2	S15VB20	Rectifier
VR1 2	YWMSF1000-4A	Wipe Mix Lever Assy
VR3	EVXP2A001B15	Variable Resistor 100K ohms
T1 ⚠	* YFPHE86V002	Power Transformer
SW1	EST1554	AC Power Switch
SW2	ESD391T	AC-DC Select Switch
SW3, 4	YWSSB02206	C/7-C/B and C/8-BGD Select Switch
F101 ⚠	XBA2C05ET0A	Current Fuse 500 mA
E1 ⚠	YWX-N1153-07	Fuse Holder
CN1	YWRM12BRD-4P	4-pin DC Input Connector
CN2-9	YWAA-34	Tally & Intercom Jack
CN10-47	YWBNC-R	BNC Connector
CN48	YWS2-104W1S0	Transistor Socket
CN50 ⚠	YFKPGTSA25	AC Power Cord for WJ-5600/A
⚠	YFHBS308A	AC Power Cord for WJ-5600/B
⚠	YFCE009908FA	AC Power Cord for WJ-5600/C
⚠	YFVM0 09908A	AC Power Cord for WJ-5600/G
M1	* YFV5WA0134B2	Front Panel
M2	* YFV2CA0043A2	Hold Plate for Front Panel
M3	YWMSF1004-5	Wipe Mix Knob G
M4	YWMSF1003-5	Wipe Mix Knob R
M5	YWL3X6BER01	Polyethylene Washer
M6	YWUM50-HM01A	Knob A for Control
M7	* YFV2SA0105A3	Mounting Angle A for Change Over Switch
M8	* YFV2SA0104A3	Mounting Angle B for Power Switch
M9	YWJ800PWB01	Rubber Holder for LED
M10	* YFV5EA0166A2	Left Side Cover
M11	* YFV5EA0165A2	Right Side Cover
M12	YFV2PA0051A4	Insulator Cover for Transformer
M13	* YFV2SA0113A2	Mounting Angle C for Fader Board
M14	* YFV5EA0163A3	Upper Cover
M15	* YFV5EA0164A3	Bottom Cover
M17	YWJ5500HR01	Knob B for Position Lever
M18	* YFV2SA0108A4	Mounting Angle D for Cord Clamp
M19	YWSR6W-1	Cord Clamp
M21	* YFV2KB0071A2	Rear Chassis
M22	YFV7DA0007A4	Hear Sink
M23	* YFV5EA0084A4	Heat Sink Cover
M26	* YFV7QA0441B4	Main Label
M27	YVZC700RB50	Serial No. Label
M30	YFV7MA0053A4	Caution Label
M32	YFV7SA0106A4	Position Switch Label

SYMBOL NO.	PART NO.	DESCRIPTION
M33	* YFV2SA0112A4	Mounting Angle E for Mix Variable Resistor
M40	YWFL-BUTTON	Push Switch Button
M41	* YFV7SA0105A3	Expression Card A for Switch
M52	YWS-F00RB05A	Fuse Exchange Label
M55	YW-BCG-UR01B	Earth Label

PCB1 OUTPUT BOARD

SYMBOL NO.	PART NO.	DESCRIPTION
IC1,2	AN610P	IC
IC3	AN610P	IC
Q1	2SA1254-BC	Transistor
Q2	2SD636-RS	Transistor
Q3	2SA1254-BC	Transistor
Q4	2SD636-RS	Transistor
Q5	2SC2377CD	Transistor
Q6	2SA1254-BC	Transistor
Q7	2SK34-CD	Transistor
Q8	2SK19-Y	Transistor
Q9,10	2SD636-RS	Transistor
Q11	2SA1254-BC	Transistor
Q12	2SD636-RS	Transistor
Q13,14	2SA1254-BC	Transistor
Q15	2SD636-RS	Transistor
Q16	2SC2377CD	Transistor
Q17	2SD636-RS	Transistor
Q18,19	2SD639RS	Transistor
Q20	2SK34-CD	Transistor
Q21	2SK19-Y	Transistor
Q22-24	2SD636-RS	Transistor
Q25	2SK19-Y	Transistor
Q26	2SK34-CD	Transistor
Q27	2SA1254-BC	Transistor
Q28	2SD636-RS	Transistor
Q29,30	2SA1254-BC	Transistor
Q31-36	2SD636-RS	Transistor
Q38	2SD636-RS	Transistor
Q39,40	2SC2377CD	Transistor
Q41,42	2SA1254-BC	Transistor
Q43	2SA1254-BC	Transistor
Q44	2SD636-RS	Transistor
Q45	2SA1254-BC	Transistor
Q46	2SD636-RS	Transistor
Q47	2SC2377CD	Transistor
Q48	2SA1254-BC	Transistor
Q49	2SK34-CD	Transistor
Q50	2SK19-Y	Transistor

SYMBOL NO.	PART NO.	DESCRIPTION	
Q51,52	2SD636-RS	Transistor	
Q53	2SA1254-BC	Transistor	
Q54	2SD636-RS	Transistor	
Q55,56	2SA1254-BC	Transistor	
Q57	2SD636-RS	Transistor	
Q58	2SA1254-BC	Transistor	
Q59	2SD636-RS	Transistor	
Q60	2SC2377CD	Transistor	
Q61	2SD636-RS	Transistor	
Q62	2SD639RS	Transistor	
Q63	2SD639RS	Transistor	
Q64	2SD636-RS	Transistor	
Q65	2SD636-RS	Transistor	
Q66	2SA1254-BC	Transistor	
Q67	2SC828-QR	Transistor	
Q201	2SC828-QR	Transistor	
D1,2	MA4075L	Diode	
D3,4	MA27WA	Diode	
R1	ERD10TJ183	Carbon	18K ohms 1/8W
R2	ERD10TJ243	Carbon	24K ohms 1/8W
R3	ERD10TJ222	Carbon	2.2K ohms 1/8W
R4	ERD10TJ101	Carbon	100 ohms 1/8W
R5,7	ERD10TJ102	Carbon	1K ohms 1/8W
R8,9	ERD10TJ101	Carbon	100 ohms 1/8W
R10	ERD10TJ222	Carbon	2.2K ohms 1/8W
R11,13	ERD10TJ103	Carbon	10K ohms 1/8W
R14	ERD10TJ104	Carbon	100K ohms 1/8W
R15	ERD10TJ103	Carbon	10K ohms 1/8W
R16	ERD10TJ222	Carbon	2.2K ohms 1/8W
R17	ERD10TJ332	Carbon	3.3K ohms 1/8W
R18	ERD10TJ681	Carbon	680 ohms 1/8W
R19	ERD10TJ152	Carbon	1.5K ohms 1/8W
R20	ERD10TJ472	Carbon	4.7K ohms 1/8W
R21	ERD10TJ222	Carbon	2.2K ohms 1/8W
R22	ERD10TJ102	Carbon	1K ohms 1/8/W
R23	ERD10TJ271	Carbon	270 ohms 1/8W
R24	ERD10TJ221	Carbon	220 ohms 1/8W
R25	ERD10TJ681	Carbon	680 ohms 1/8W
R26	ERD10TJ682	Carbon	6.8K ohms 1/8W
R27	ERD10TJ681	Carbon	680 ohms 1/8W
R28	ERD10TJ271	Carbon	270 ohms 1/8W
R29	ERD10TJ271	Carbon	270 ohms 1/8W
R30	ERD10TJ103	Carbon	10K ohms 1/8W
R31	ERD10TJ821	Carbon	820 ohms 1/8W
R32	ERD10TJ221	Carbon	220 ohms 1/8W
R33	ERD10TJ222	Carbon	2.2K ohms 1/8W
R34	ERD10TJ562	Carbon	5.6K ohms 1/8W
R35	ERD10TJ122	Carbon	1.2K ohms 1/8W
R36	ERD10TJ101	Carbon	100 ohms 1/8W
R37	ERD10TJ392	Carbon	3.9K ohms 1/8W
R38	ERD10TJ822	Carbon	8.2K ohms 1/8W
R39	ERD10TJ682	Carbon	6.8K ohms 1/8W
R40	ERD10TJ333	Carbon	33K ohms 1/8W
R41	ERD10TJ243	Carbon	24K ohms 1/8W
R42	ERD10TJ271	Carbon	270 ohms 1/8W
R43	ERD10TJ101	Carbon	100 ohms 1/8W
R44	ERD10TJ152	Carbon	1.5K ohms 1/8W
R45	ERD10TJ122	Carbon	1.2K ohms 1/8W
R46	ERD10TJ272	Carbon	2.7K ohms 1/8W
R47	ERD10TJ162	Carbon	1.6K ohms 1/8W
R48	ERD10TJ560	Carbon	56 ohms 1/8W
R50	ERD10TJ561	Carbon	560 ohms 1/8W
R51	ERD10TJ101	Carbon	100 ohms 1/8W
R52	ERD10TJ183	Carbon	18K ohms 1/8W
R53	ERD10TJ222	Carbon	2.2K ohms 1/8W
R54	ERD10TJ392	Carbon	3.9K ohms 1/8W
R55,56	ERD10TJ8R2	Carbon	8.2 ohms 1/8W
R57	ERD10TJ121	Carbon	120 ohms 1/8W
R58	ERD10TJ223	Carbon	22K ohms 1/8W
R59	ERD10TJ104	Carbon	100K ohms 1/8W
R60	ERD10TJ562	Carbon	5.6K ohms 1/8W
R61	ERD10TJ152	Carbon	1.5K ohms 1/8W
R62,63	ERD10TJ561	Carbon	560 ohms 1/8W
R64	ERD10TJ332	Carbon	3.3K ohms 1/8W
R65	ERD10TJ681	Carbon	680 ohms 1/8W
R66	ERD10TJ152	Carbon	1.5K ohms 1/8W
R67	ERD10TJ472	Carbon	4.7K ohms 1/8W
R68	ERD10TJ222	Carbon	2.2K ohms 1/8W
R69	ERD10TJ471	Carbon	470 ohms 1/8W
R70	ERD10TJ331	Carbon	330 ohms 1/8W
R71	ERD10TJ103	Carbon	10K ohms 1/8W
R72	ERD10TJ271	Carbon	270 ohms 1/8W
R73	ERD10TJ681	Carbon	680 ohms 1/8W
R74	ERD10TJ562	Carbon	5.6K ohms 1/8W
R75	ERD10TJ681	Carbon	680 ohms 1/8W
R76	ERD10TJ331	Carbon	330 ohms 1/8W
R77	ERD10TJ271	Carbon	270 ohms 1/8W
R78	ERD10TJ821	Carbon	820 ohms 1/8W
R79	ERD10TJ681	Carbon	680 ohms 1/8W
R80	ERD10TJ332	Carbon	3.3K ohms 1/8W
R81	ERD10TJ104	Carbon	100Kohms 1/8W
R82	ERD10TJ331	Carbon	330 ohms 1/8W
R83	ERD10TJ221	Carbon	220 ohms 1/8W
R84	ERD10TJ222	Carbon	2.2K ohms 1/8W
R85	ERD10TJ562	Carbon	5.6K ohms 1/8W
R86	ERD10TJ122	Carbon	1.2K ohms 1/8W
R87	ERD10TJ101	Carbon	100 ohms 1/8W
R88	ERD10TJ102	Carbon	1K ohms 1/8W
R89,90	ERD10TJ222	Carbon	2.2K ohms 1/8W
R91	ERD10TJ103	Carbon	10K ohms 1/8W
R92	ERD10TJ101	Carbon	100 ohms 1/8W
R93	ERD10TJ222	Carbon	2.2K ohms 1/8W
R94	ERD10TJ332	Carbon	3.3K ohms 1/8W
R95	ERD10TJ392	Carbon	3.9K ohms 1/8W
R96	ERD10TJ222	Carbon	2.2K ohms 1/8W
R97	ERD10TJ103	Carbon	10K ohms 1/8W
R98	ERD10TJ333	Carbon	33K ohms 1/8W
R99	ERD10TJ562	Carbon	5.6K ohms 1/8W
R100	ERD10TJ182	Carbon	1.8K ohms 1/8W
R101	ERD10TJ101	Carbon	100 ohms 1/8W
R102,103	ERD10TJ223	Carbon	22K ohms 1/8W
R104,105	ERD10TJ102	Carbon	1K ohms 1/8W
R106	ERD10TJ332	Carbon	3.3K ohms 1/8W
R110	ERD10TJ331	Carbon	330 ohms 1/8W
R111	ERD10TJ561	Carbon	560 ohms 1/8W
R112	ERD10TJ393	Carbon	39K ohms 1/8W
R113	ERD10TJ103	Carbon	10K ohms 1/8W
R114, 115	ERD10TJ152	Carbon	1.5K ohms 1/8W

SYM-BOL NO.	PART NO.	DESCRIPTION	
R116	ERD10TJ222	Carbon	2.2K ohms 1/8W
R117	ERD10TJ182	Carbon	1.8K ohms 1/8W
R118,119	ERD10TJ222	Carbon	2.2K ohms 1/8W
R120	ERD10TJ332	Carbon	3.2K ohms 1/8W
R121	ERD10TJ222	Carbon	2.2K ohms 1/8W
R122	ERD10TJ103	Carbon	10K ohms 1/8W
R123	ERD10TJ183	Carbon	18K ohme 1/8W
R124	ERD10TJ223	Carbon	22K ohms 1/8W
R125	ERD10TJ101	Carbon	100 ohms 1/8W
R126,127	ERD10TJ102	Carbon	1K ohms 1/8W
R128,129	ERD10TJ101	Carbon	100 ohms 1/8W
R130	ERD10TJ222	Carbon	2.2K ohms 1/8W
R131,132	ERD10TJ103	Carbon	10K ohms 1/8W
R133	ERD10TJ104	Carbon	100K ohms 1/8W
R134	ERD10TJ103	Carbon	10K ohms 1/8W
R135	ERD10TJ222	Carbon	2.2K ohms 1/8W
R136	ERD10TJ332	Carbon	3.3K ohms 1/8W
R137	ERD10TJ681	Carbon	680 ohms 1/8W
R138	ERD10TJ152	Carbon	1.5K ohms 1/8W
R139	ERD10TJ472	Carbon	4.7K ohms 1/8W
R140	ERD10TJ222	Carbon	2.2K ohms 1/8W
R141	ERD10TJ102	Carbon	1K ohms 1/8W
R142	ERD10TJ221	Carbon	220 ohms 1/8W
R143	ERD10TJ271	Carbon	270 ohms 1/8W
R144	ERD10TJ681	Carbon	680 ohms 1/8W
R145	ERD10TJ682	Carbon	6.8K ohms 1/8W
R146	ERD10TJ681	Carbon	680 ohms 1/8W
R147	ERD10TJ271	Carbon	270 ohms 1/8W
R148	ERD10TJ271	Carbon	270 ohms 1/8W
R149	ERD10TJ103	Carbon	10K ohms 1/8W
R150	ERD10TJ821	Carbon	820 ohms 1/8W
R151	ERD10TJ221	Carbon	220 ohms 1/8W
R152	ERD10TJ222	Carbon	2.2K ohms 1/8W
R153	ERD10TJ562	Carbon	5.6K ohms 1/8W
R154	ERD10TJ122	Carbon	1.2K ohms 1/8W
R155	ERD10TJ392	Carbon	3.9K ohms 1/8W
R156	ERD10TJ103	Carbon	10K ohms 1/8W
R157	ERD10TJ682	Carbon	6.8K ohms 1/8W
R158	ERD10TJ153	Carbon	15K ohms 1/8W
R159	ERD10TJ273	Carbon	27K ohms 1/8W
R160	ERD10TJ101	Carbon	100 ohms 1/8W
R161,162	ERD10TJ102	Carbon	1K ohms 1/8W
R163,164	ERD10TJ101	Carbon	100 ohms 1/8W
R165	ERD10TJ333	Carbon	33K ohms 1/8W
R166	ERD10TJ243	Carbon	24K ohms 1/8W
R167	ERD10TJ271	Carbon	270 ohms 1/8W
R168	ERD10TJ101	Carbon	100 ohms 1/8W
R169	ERD10TJ222	Carbon	2.2K ohms 1/8W
R170	ERD10TJ122	Carbon	1.2K ohms 1/8W
R171	ERD10TJ101	Carbon	100 ohms 1/8W
R172	ERD10TJ272	Carbon	2.7K ohms 1/8W
R173	ERD10TJ162	Carbon	1.6K ohms 1/8W
R174	ERD10TJ561	Carbon	560 ohms 1/8W
R176	ERD10TJ183	Carbon	18K ohms 1/8W
R178	ERD10TJ222	Carbon	2.2K ohms 1/8W
R179	ERD10TJ392	Carbon	3.9K ohms 1/8W
R180,181	ERD10TJ8R2	Carbon	8.2 ohms 1/8W
R182	ERD10TJ121	Carbon	120 ohms 1/8W
R183	ERD10TJ223	Carbon	22K ohms 1/8W
R184	ERD10TJ221	Carbon	220 ohms 1/8W
R185,186	ERD10TJ101	Carbon	100 ohms 1/8W
R187	ERD10TJ222	Carbon	2.2K ohms 1/8W
R188, 189	ERD10TJ821	Carbon	820 ohms 1/8W
R190	ERD10TJ101	Carbon	100 ohms 1/8W
R191	ERD10TJ332	Carbon	3.3K ohms 1/8W
R192	ERD10TJ272	Carbon	2.7K ohms 1/8W
R193	ERD10TJ102	Carbon	1K ohms 1/8W
R201	ERD10TJ561	Carbon	560 ohms 1/8W
VR1	YFP0T3321P52	Variable Resistor	500 ohms
VR2,3	YFP0T3321P23	Variable Resistor	2K ohms
VR4	YFP0T3321P52	Variable Resistor	500 ohms
VR5	YFP0T3321P23	Variable Resistor	2K ohms
VR6	YFP0T3321P13	Variable Resistor	1K ohms
VR7	YFP0T3321P23	Variable Resistor	2K ohms
VR8	YFP0T3321P53	Variable Resistor	5K ohms
VR9	YFP0T3321P52	Variable Resistor	500 ohms
VR10	YFP0T3321P53	Variable Resistor	5K ohms
VR11	YFP0T3321P14	Variable Resistor	10K ohms
VR12	YFP0T3321P13	Variable Resistor	1K ohms
VR13	YFP0T3321P52	Variable Resistor	500 ohms
VR14,15	YFP0T3321P23	Variable Resistor	2K ohms
VR16	YFP0T3321P13	Variable Resistor	1K ohms
VR17	YFP0T3321P23	Variable Resistor	2K ohms
VR18	YFP0T3321P53	Variable Resistor	5K ohms
VR19,20	YFP0T3321P52	Variable Resistor	500 ohms
VR21	YFP0T3321P23	Variable Resistor	2K ohms
VR22	YFP0T3321P52	Variable Resistor	500 ohms
VR23,24	YFP0T3321P23	Variable Resistor	2K ohms
VR25	YFP0T3321P13	Variable Resistor	1K ohms
VR26	YFP0T3321P23	Variable Resistor	2K ohms
VR27	YFP0T3321P53	Variable Resistor	5K ohms
VR28,29	YFP0T3321P52	Variable Resistor	500 ohms
VR30	YFP0T3321P53	Variable Resistor	5K ohms
VR31	YFP0T3321P14	Variable Resistor	10K ohms
C1	ECEA1ASS101	Electrolytic	100 µF 10V
C2	ECEA1AN470S	Electrolytic	47 µF 10V
C3,4	ECCF1H680JC	Ceramic	68 pF 50V
C6	ECQV05223JZ	Plastic	0.022 µF 50V
C7	ECEA1CSS100	Electrolytic	10 µF 16V
C8	ECCF1H270JC	Ceramic	27 pF 50V
C9-11	ECEA1CSS100	Electrolytic	10 µF 16V
C12	ECEA1ASS470	Electrolytic	47 µF 10V
C13	ECEA1ASS101	Electrolytic	100 µF 10V
C14	ECEA1CSS100	Electrolytic	10 µF 16V
C15	ECEA1AN470S	Electrolytic	47 µF 10V
C17	ECEA0JSS470	Electrolytic	47µF 6.3V
C18	ECEA1ASS101	Electrolytic	100 µF 10V
C19,20	ECEA1ASS222	Electrolytic	2200 µF 10V
C21,22	ECEA1ASS101	Electrolytic	100 µF 10V
C23	ECQV05223JZ	Plastic	0.022 µF 50V
C24	ECCF1H270JC	Ceramic	27 pF 50V
C25-28	ECEA1CSS100	Electrolytic	10 µF 16V

SYM-BOL NO.	PART NO.	DESCRIPTION	
C30	ECEA1CSS100	Electrolytic	10 μF 16V
C32	ECEA1ASS470	Electrolytic	47 μF 10V
C33	ECQV05222JZ	Plastic	2200 pF 50V
C34	ECEA1ASS470	Electrolytic	47 μF 10V
C36	ECEA1ASS101	Electrolytic	100 μF 10V
C37	ECEA1HS010	Electrolytic	1 μF 50V
C38	ECEA1ASS470	Electrolytic	47 μF 10V
C40	ECCW1H101JC	Ceramic	100 pF 50V
C41	ECEA1ASS470	Electrolytic	47 μF 10V
C42,43	ECEA1ASS101	Electrolytic	100 μF 10V
C44	ECEA1AN470S	Electrolytic	47 μF 10V
C45,46	ECCF1H680JC	Ceramic	68 pF 50V
C48	ECQV05223JZ	Plastic	0.022 μF 50V
C49	ECCF1H270JC	Ceramic	27 pF 50V
C50-53	ECEA1CSS100	Electrolytic	10 μF 16V
C54	ECEA1ASS470	Electrolytic	47 μF 10V
C56	ECEA1CSS100	Electrolytic	10 μF 16V
C57,58	ECCF1H680JC	Ceramic	68 pF 50V
C59	ECEA1AN470S	Electrolytic	47 μF 10V
C60	ECEA0JSS470	Electrolytic	47μF 6.3V
C61	ECEA1ASS101	Electrolytic	100 μF 10V
C63	ECEA1ASS101	Electrolytic	100 μF 10V
C64,65	ECEA1ASS222	Electrolytic	2200 μF 10V
C66	ECCF1H100JC	Ceramic	10 pF 50V
C67	ECCF1H101JC	Ceramic	100 pF 50V
C68	ECEA1ASS101	Electrolytic	100 μF 10V
C201	ECQV05223JZ	Plastic	0.022μF 50V
L1,2	ELEY470KA	Coil	47μH
L4	ELEY470KA	Coil	47μH
CF1	SLC871-197	Filter	4.43MHz
CT1,2	ECRHA040E11	Trimmer Capaciton	40pF

PCB2 DSK, BGD BOARD

SYM-BOL NO.	PART NO.	DESCRIPTION	
IC1	AN610P	IC	
IC2	AN78N05	IC	
IC3	MC14077BP	IC	
IC4	YWHD74LS221P	IC	
IC5	YWHD74LS157P	IC	
IC6	YWHD74LS221P	IC	
IC7	YWHD74LS157P	IC	
Q1,2	2SD636-RS	Transistor	
Q9,10	2SD636-RS	Transistor	
Q11	2SA1254-BC	Transistor	
Q12-14	2SD636-RS	Transistor	
Q15	2SA1254-BC	Transistor	
Q16,17	2SD636-RS	Transistor	
Q18	2SK34-CD	Transistor	
Q19	2SD636-RS	Transistor	
Q20	2SC2377CD	Transistor	
Q21-23	2SA1254-BC	Transistor	
Q24	2SC2377CD	Transistor	
Q25	2SA1254-BC	Transistor	
Q26	2SC2377CD	Transistor	
Q27	2SC1216F	Transistor	
Q28	2SC2377CD	Transistor	
Q29	2SC1216F	Transistor	
Q30,32	2SD636-RS	Transistor	
Q33	2SA1254-BC	Transistor	
Q34,35	2SC2377CD	Transistor	
Q36	2SD636-RS	Transistor	
Q37	2SA1254-BC	Transistor	
Q38	2SD636-RS	Transistor	
Q39,40	2SA1254-BC	Transistor	
Q41	2SD636-RS	Transistor	
Q42	2SA1254 BC	Transistor	
Q43	2SC2377CD	Transistor	
Q44,45	2SD636-RS	Transistor	
Q46-48	2SA1254-BC	Transistor	
Q49,52	2SD636-RS	Transistor	
Q53	2SK34-CD	Transistor	
Q54-56	2SD636-RS	Transistor	
Q57	2SC2377CD	Transistor	
Q58	2SD636-RS	Transistor	
Q59	2SC2377CD	Transistor	
Q60,61	2SD636-RS	Transistor	
Q62	2SA1254-BC	Transistor	
Q63	2SC2377CD	Transistor	
Q64	2SD636-RS	Transistor	
Q65	2SC2377CD	Transistor	
Q66	2SA1254-BC	Transistor	
Q67	2SC2377CD	Transistor	
Q68,69	2SD636-RS	Transistor	
Q70-72	2SA1254-BC	Transistor	
Q73,80	2SD636-RS	Transistor	
Q81	2SC2377CD	Transistor	
D1	MA165	Diode	
D2	MA27TA	Diode	
D3	MA165	Diode	
D4	MA27A	Diode	
D5	MA26TA	Diode	
D6	MA26A	Diode	
R1,2	ERD10TJ222	Carbon	2.2K ohms 1/8W
R3	ERD10TJ822	Carbon	8.2K ohms 1/8W
R4	ERD10TJ221	Carbon	220 ohms 1/8W
R5	ERD10TJ472	Carbon	4.7K ohms 1/8W
R6,7	ERD10TJ223	Carbon	22K ohms 1/8W
R8	ERD10TJ122	Carbon	1.2K ohms 1/8W
R9,10	ERD10TJ102	Carbon	1K ohms 1/8W
R11,12	ERD10TJ223	Carbon	22K ohms 1/8W
R13,14	ERD10TJ102	Carbon	1K ohms 1/8W
R21	ERD10TJ103	Carbon	10K ohms 1/8W
R24	ERD10TJ182	Carbon	1.8K ohms 1/8W
R25	ERD10TJ681	Carbon	680 ohms 1/8W
R26	ERD10TJ242	Carbon	2.4K ohms 1/8W
R27	ERD10TJ821	Carbon	820 ohms 1/8W
R28	ERD10TJ472	Carbon	4.7K ohms 1/8W
R29	ERD10TJ222	Carbon	2.2K ohms 1/8W
R30	ERD10TJ271	Carbon	270 ohms 1/8W

MODEL WJ-5600

SYMBOL NO.	PART NO.	DESCRIPTION	
R31	ERD10TJ331	Carbon	330 ohms 1/8W
R32	ERD10TJ681	Carbon	680 ohms 1/8W
R33	ERD10TJ331	Carbon	330 ohms 1/8W
R34	ERD10TJ681	Carbon	680 ohms 1/8W
R35,36	ERD10TJ561	Carbon	560 ohms 1/8W
R37	ERD10TJ222	Carbon	2.2K ohms 1/8W
R38	ERD10TJ472	Carbon	4.7K ohms 1/8W
R39	ERD10TJ153	Carbon	15K ohms 1/8W
R40	ERD10TJ222	Carbon	2.2K ohms 1/8W
R41	ERD10TJ122	Carbon	1.2K ohms 1/8W
R42	ERD10TJ221	Carbon	220 ohms 1/8W
R43	ERD10TJ222	Carbon	2.2K ohms 1/8W
R44	ERD10TJ562	Carbon	5.6K ohms 1/8W
R45	ERD10TJ152	Carbon	1.5K ohms 1/8W
R46	ERD10TJ222	Carbon	2.2K ohms 1/8W
R47	ERD10TJ152	Carbon	1.5K ohms 1/8W
R48	ERD10TJ472	Carbon	4.7K ohms 1/8W
R49	ERD10TJ223	Carbon	22K ohms 1/8W
R50	ERD10TJ153	Carbon	15K ohms 1/8W
R51,52	ERD10TJ471	Carbon	470 ohms 1/8W
R53	ERD10TJ392	Carbon	3.9K ohms 1/8W
R54-56	ERD10TJ471	Carbon	470 ohms 1/8W
R57	ERD10TJ222	Carbon	2.2K ohms 1/8W
R58	ERD10TJ104	Carbon	100K ohms 1/8W
R59	ERD10TJ821	Carbon	820 ohms 1/8W
R60	ERD10TJ151	Carbon	150 ohms 1/8W
R61	ERD10TJ153	Carbon	15K ohms 1/8W
R62	ERD10TJ152	Carbon	1.5K ohms 1/8W
R63	ERD10TJ681	Carbon	680 ohms 1/8W
R64	ERD10TJ102	Carbon	1K ohms 1/8W
R65	ERD10TJ152	Carbon	1.5K ohms 1/8W
R66	ERD10TJ332	Carbon	3.3K ohms 1/8W
R67	ERD10TJ101	Carbon	100 ohms 1/8W
R68	ERD10TJ102	Carbon	1K ohms 1/8W
R69	ERD10TJ151	Carbon	150 ohms 1/8W
R70	ERD10TJ332	Carbon	3.3K ohms 1/8W
R71,72	ERD10TJ101	Carbon	100 ohms 1/8W
R73,74	ERD10TJ102	Carbon	1K ohms 1/8W
R75	ERD10TJ751	Carbon	750 ohms 1/8W
R76	ERD10TJ101	Carbon	100 ohms 1/8W
R77,78	ERD10TJ102	Carbon	1K ohms 1/8W
R79	ERD10TJ472	Carbon	4.7K ohms 1/8W
R81	ERD10TJ101	Carbon	100 ohms 1/8W
R82	ERD10TJ102	Carbon	1K ohms 1/8W
R86	ERD10TJ221	Carbon	220 ohms 1/8W
R87,88	ERD10TJ222	Carbon	2.2K ohms 1/8W
R89	ERD10TJ221	Carbon	220 ohms 1/8W
R90	ERD10TJ562	Carbon	5.6K ohms 1/8W
R91	ERD10TJ561	Carbon	560 ohms 1/8W
R92	ERD10TJ222	Carbon	2.2K ohms 1/8W
R93	ERD10TJ101	Carbon	100 ohms 1/8W
R94	ERD10TJ102	Carbon	1K ohms 1/8W
R95-97	ERD10TJ101	Carbon	100 ohms 1/8W
R98	ERD10TJ102	Carbon	1K ohms 1/8W
R99	ERD10TJ222	Carbon	2.2K ohms 1/8W
R100	ERD10TJ101	Carbon	100 ohms 1/8W

SYMBOL NO.	PART NO.	DESCRIPTION	
R101	ERD10TJ102	Carbon	1K ohms 1/8W
R102,103	ERD10TJ101	Carbon	100 ohms 1/8W
R104	ERD10TJ102	Carbon	1K ohms 1/8W
R106,107	ERD10TJ103	Carbon	10K ohms 1/8W
R108	ERD10TJ332	Carbon	3.3K ohms 1/8W
R109	ERD10TJ333	Carbon	33K ohms 1/8W
R110	ERD10TJ103	Carbon	10K ohms 1/8W
R111-113	ERD10TJ562	Carbon	5.6K ohms 1/8W
R114	ERD10TJ222	Carbon	2.2K ohms 1/8W
R115	ERD10TJ562	Carbon	5.6K ohms 1/8W
R116	ERD10TJ153	Carbon	15K ohms 1/8W
R117	ERD10TJ562	Carbon	5.6K ohms 1/8W
R118	ERD10TJ681	Carbon	680 ohms 1/8W
R119	ERD10TJ682	Carbon	6.8K ohms 1/8W
R120	ERD10TJ562	Carbon	5.6K ohms 1/8W
R121	ERD10TJ332	Carbon	3.3K ohms 1/8W
R122	ERD10TJ682	Carbon	6.8K ohms 1/8W
R123	ERD10TJ333	Carbon	33K ohms 1/8W
R124	ERD10TJ153	Carbon	15K ohms 1/8W
R125	ERD10TJ681	Carbon	680 ohms 1/8W
R126	ERD10TJ222	Carbon	2.2K ohms 1/8W
R130	ERD10TJ473	Carbon	47K ohms 1/8W
R131	ERD10TJ223	Carbon	22K ohms 1/8W
R132	ERD10TJ101	Carbon	100 ohms 1/8W
R133	ERD10TJ152	Carbon	1.5K ohms 1/8W
R134	ERD10TJ102	Carbon	1K ohms 1/8W
R135	ERD10TJ104	Carbon	100K ohms 1/8W
R136	ERD10TJ222	Carbon	2.2K ohms 1/8W
R137	ERD10TJ151	Carbon	150 ohms 1/8W
R138	ERD10TJ153	Carbon	15K ohms 1/8W
R139	ERD10TJ122	Carbon	1.2K ohms 1/8W
R140	ERD10TJ681	Carbon	680 ohms 1/8W
R141	ERD10TJ222	Carbon	2.2K ohms 1/8W
R142	ERD10TJ562	Carbon	5.6K ohms 1/8W
R143	ERD10TJ392	Carbon	3.9K ohms 1/8W
R144	ERD10TJ152	Carbon	1.5K ohms 1/8W
R145	ERD10TJ332	Carbon	3.3K ohms 1/8W
R146	ERD10TJ152	Carbon	1.5K ohms 1/8W
R147	ERD10TJ222	Carbon	2.2K ohms 1/8W
R148	ERD10TJ682	Carbon	6.8K ohms 1/8W
R149,150	ERD10TJ102	Carbon	1K ohms 1/8W
R151,152	ERD10TJ332	Carbon	3.3K ohms 1/8W
R153	ERD10TJ103	Carbon	10K ohms 1/8W
R154	ERD10TJ562	Carbon	5.6K ohms 1/8W
R155	ERD10TJ102	Carbon	1K ohms 1/8W
R156	ERD10TJ152	Carbon	1.5K ohms 1/8W
R157-159	ERD10TJ103	Carbon	10K ohms 1/8W
R160	ERD10TJ331	Carbon	330 ohms 1/8W
R161	ERD10TJ182	Carbon	1.8K ohms 1/8W
R162	ERD10TJ331	Carbon	330 ohms 1/8W
R163	ERD10TJ153	Carbon	15K ohms 1/8W
R164	ERD10TJ562	Carbon	5.6K ohms 1/8W
R165	ERD10TJ332	Carbon	3.3K ohms 1/8W
R166	ERD10TJ273	Carbon	27K ohms 1/8W
R167	ERD10TJ153	Carbon	15K ohms 1/8W
R168	ERD10TJ103	Carbon	10K ohms 1/8W

SYMBOL NO.	PART NO.	DESCRIPTION	
R170	ERD10TJ681	Carbon	680 ohms 1/8W
R171	ERD10TJ101	Carbon	100 ohms 1/8W
R172	ERD10TJ123	Carbon	12K ohms 1/8W
R173	ERD10TJ223	Carbon	22K ohms 1/8W
R174	ERD10TJ222	Carbon	2.2K ohms 1/8W
R175	ERD10TJ102	Carbon	1K ohms 1/8W
R176	ERD10TJ332	Carbon	3.3K ohms 1/8W
VR1	YFK12142KB	Variable Resistor	2K ohms
VR2,3	YFK121410KB	Variable Resistor	10K ohms
VR4	YFK12142KB	Variable Resistor	2K ohms
VR5	YFP0T3321P23	Variable Resistor	2K ohms
VR6	YFP0T3321P53	Variable Resistor	5K ohms
VR7-9	YFP0T3321P23	Variable Resistor	2K ohms
VR10,11	YFP0T3321P52	Variable Resistor	500 ohms
VR12	YFP0T3321P23	Variable Resistor	2K ohms
VR13,14	YFP0T3321P52	Variable Resistor	500 ohms
VR15	YFP0T3321P23	Variable Resistor	2K ohms
C1,2	ECCF1H180JC	Ceramic	18 pF 50V
C3	ECSF10E47	Electrolytic	47 µF 10V
C4	ECCF1H220JC	Ceramic	22 pF 50V
C5	ECSF10E47	Electrolytic	47 µF 10V
C6	ECCF1H220JC	Ceramic	22PF 50V
C7	ECCF1H221J	Ceramic	220 pF 50V
C8	ECSF16E33	Electrolytic	33 µF 16V
C9,10	ECQV05223JZ	Plastic	0.022 µF 50V
C11	ECCF1H070DC	Ceramic	7 pF 50V
C12	ECCF1H101JC	Ceramic	100 pF 50V
C17	ECQV05103JZ	Plastic	0.01 µF 50V
C18-20	ECEA1CSS100	Electrolytic	10 µF 16V
C23,24	ECEA1ASS470	Electrolytic	47 µF 10V
C25	ECEA1ASS101	Electrolytic	100 µF 10V
C26	ECEA1CSS100	Electrolytic	10 µF 16V
C27	ECEA1ASS470	Electrolytic	47 µF 10V
C28,29	ECCF1H101JC	Ceramic	100 pF 50V
C31	ECCF1H181JC	Ceramic	180 pF 50V
C32	ECSF16E33	Electrolytic	33 µF 16V
C35	ECEA1ASS101	Electrolytic	100 µF 10V
C36	ECQV05563JZ	Plastic	0.056 µF 50V
C37	ECEA1CSS100	Electrolytic	10 µF 16V
C38	ECCF1H151JR	Ceramic	150 pF 50V
C39	ECEA1ASS101	Electrolytic	100 µF 10V
C40,43	ECCF1H680JC	Ceramic	68 pF 50V
C44-46	ECCF1H680JC	Ceramic	68 pF 50V
C47	ECEA1ASS101	Electrolytic	100 µF 10V
C48	ECEA1CSS100	Electrolytic	10 µF 16V
C49	ECSF16E33	Electrolytic	33 µF 16V
C50	ECSF16E47	Electrolytic	47 µF 16V
C51	ECEA1ASS101	Electrolytic	100 µF 10V
C52	ECQV05223JZ	Plastic	0.022 µF 50V
C53	ECCF1H101JC	Ceramic	100 pF 50V
C54	ECEA1ESS470	Electrolytic	47 µF 25V
C55	ECCF1H390JC	Ceramic	39 pF 50V
C56	ECSF16E47	Electrolytic	47 µF 16V
C58,60	ECEA1ASS101	Electrolytic	100 µF 10V

SYMBOL NO.	PART NO.	DESCRIPTION	
C61	ECEA1ASS470	Electrolytic	47 µF 10V
C62	ECQV05563JZ	Plastic	0.056 µF 50V
C63	ECCF1H270J	Ceramic	27 pF 50V
C64	ECEA1CSS100	Electrolytic	10 µF 16V
C65	ECCF1H270J	Ceramic	27 pF 50V
C66,67	ECSF10E10	Electrolytic	10 µF 10V
C68-70	ECEA1CSS100	Electrolytic	10 µF 16V
C71	ECEA1ASS470	Electrolytic	47 µF 10V
C72	ECCF1H560JC	Ceramic	56 pF 50V
C73	ECCF1H680JC	Ceramic	68 pF 50V
C74	ECEA1ASS101	Electrolytic	100 µF 10V
C75	ECCF1H151JR	Ceramic	150 pF 50V
C80	ECCF1H560JC	Ceramic	56 pF 50V
C82	ECEA1ASS470	Electrolytic	47 µF 10V
C83	ECEA1CSS470	Electrolytic	47 µF 16V
CT1,2	ECV1ZW25X53T	Trimmer Capacitor	25 pF
L1	ELEY470KA	Coil	47 µH
L3,4	ELEY470KA	Coil	47 µH
SW1,2	YWSSB02206	Slide Switch	
CF1	YFSLC871-197	Filter	
CN1-JM	YFB2B-XH-A	2 pin Jack Male	
CN2-JM	YFB2B-XH-A	2 pin Jack Male	
M36	YFV2SA0110A3	Mounting Angle B for Variable Resistor	

PCB 3 EFFECT, MIX BOARD

SYMBOL NO.	PART NO.	DESCRIPTION
IC1	AN610P	IC
IC2	AN78N05	IC
IC3-6	AN610P	IC
IC7	YWHD74LS157P	IC
IC8,9	YWHD74LS221P	IC
IC10	YWHD74LS157P	IC
Q1,2	2SD636-RS	Transistor
Q3	2SA1254-BC	Transistor
Q4,9	2SD636-RS	Transistor
Q10	2SD636-RS	Transistor
Q11	2SA1254-BC	Transistor
Q12,13	2SD636-RS	Transistor
Q14	2SC2377CD	Transistor
Q15	2SA1254-BC	Transistor
Q16	2SC2377CD	Transistor
Q17-20	2SD636-RS	Transistor
Q21	2SA721TU	Transistor
Q22,23	2SK34-CD	Transistor
Q24	2SK19-Y	Transistor
Q25,26	2SC2377CD	Transistor
Q28	2SA1254-BC	Transistor
Q29	2SD636-RS	Transistor
Q30	2SC2377CD	Transistor
Q31	2SK19-Y	Transistor
Q32	2SK34-CD	Transistor
Q33	2SC2377CD	Transistor

MODEL WJ-5600

SYMBOL NO.	PART NO.	DESCRIPTION	
Q34	2SA1254-BC	Transistor	
Q35	2SD636-RS	Transistor	
Q36	2SA721TU	Transistor	
Q37	2SK34-CD	Transistor	
Q38,39	2SA1254-BC	Transistor	
Q40,41	2SD636-RS	Transistor	
Q42	2SA1254-BC	Transistor	
Q43	2SC2377CD	Transistor	
Q44	2SK34-CD	Transistor	
Q45	2SK19-Y	Transistor	
Q46	2SC2377CD	Transistor	
Q47	2SD636-RS	Transistor	
Q48	2SA1254-BC	Transistor	
Q49	2SD636-RS	Transistor	
Q50	2SC2377CD	Transistor	
Q51	2SK19-Y	Transistor	
Q52	2SK34-CD	Transistor	
Q53	2SC2377CD	Transistor	
Q54	2SA1254-BC	Transistor	
Q55	2SD636-RS	Transistor	
D1	MA27A	Diode	
R1,2	ERD10TJ222	Carbon	2.2K ohms 1/8W
R3	ERD10TJ822	Carbon	8.2K ohms 1/8W
R4	ERD10TJ221	Carbon	220 ohms 1/8W
R5	ERD10TJ472	Carbon	4.7K ohms 1/8W
R6,7	ERD10TJ223	Carbon	22K ohms 1/8W
R8	ERD10TJ122	Carbon	1.2K ohms 1/8W
R9,10	ERD10TJ102	Carbon	1K ohms 1/8W
R11,12	ERD10TJ223	Carbon	22K ohms 1/8W
R13,14	ERD10TJ102	Carbon	1K ohms 1/8W
R15	ERD10TJ332	Carbon	3.3K ohms 1/8W
R16	ERD10TJ153	Carbon	15K ohms 1/8W
R17	ERD10TJ562	Carbon	5.6K ohms 1/8W
R18	ERD10TJ102	Carbon	1K ohms 1/8W
R19	ERD10TJ182	Carbon	1.8K ohms 1/8W
R20	ERD10TJ101	Carbon	100 ohms 1/8W
R24	ERD10TJ182	Carbon	1.8K ohms 1/8W
R25	ERD10TJ102	Carbon	1K ohms 1/8W
R26	ERD10TJ242	Carbon	2.4K ohms 1/8W
R27	ERD10TJ821	Carbon	820 ohms 1/8W
R28	ERD10TJ472	Carbon	4.7K ohms 1/8W
R29	ERD10TJ222	Carbon	2.2K ohms 1/8W
R30	ERD10TJ271	Carbon	270 ohms 1/8W
R31	ERD10TJ331	Carbon	330 ohms 1/8W
R32	ERD10TJ681	Carbon	680 ohms 1/8W
R33	ERD10TJ331	Carbon	330 ohms 1/8W
R34	ERD10TJ681	Carbon	680 ohms 1/8W
R35,36	ERD10TJ561	Carbon	560 ohms 1/8W
R37	ERD10TJ222	Carbon	2.2K ohms 1/8W
R38	ERD10TJ472	Carbon	4.7K ohms 1/8W
R39	ERD10TJ153	Carbon	15K ohms 1/8W
R40	ERD10TJ222	Carbon	2.2K ohms 1/8W
R41	ERD10TJ122	Carbon	1.2K ohms 1/8W
R42	ERD10TJ221	Carbon	220 ohms 1/8W
R43	ERD10TJ222	Carbon	2.2K ohms 1/8W
R44	ERD10TJ562	Carbon	5.6K ohms 1/8W
R45	ERD10TJ122	Carbon	1.2K ohms 1/8W
R46	ERD10TJ222	Carbon	2.2K ohms 1/8W
R47	ERD10TJ152	Carbon	1.5K ohms 1/8W
R48	ERD10TJ472	Carbon	4.7K ohms 1/8W
R49	ERD10TJ223	Carbon	22K ohms 1/8W
R50	ERD10TJ153	Carbon	15K ohms 1/8W
R51,52	ERD10TJ471	Carbon	470 ohms 1/8W
R53	ERD10TJ392	Carbon	3.9K ohms 1/8W
R54,55	ERD10TJ471	Carbon	470 ohms 1/8W
R56	ERD10TJ271	Carbon	270 ohms 1/8W
R57	ERD10TJ222	Carbon	2.2K ohms 1/8W
R58,59	ERD10TJ332	Carbon	3.3K ohms 1/8W
R60	ERD10TJ471	Carbon	470 ohms 1/8W
R61	ERD10TJ681	Carbon	680 ohms 1/8W
R62,63	ERD10TJ271	Carbon	270 ohms 1/8W
R64	ERD10TJ471	Carbon	470 ohms 1/8W
R65,66	ERD10TJ821	Carbon	820 ohms 1/8W
R67	ERD10TJ391	Carbon	390 ohms 1/8W
R68	ERD10TJ152	Carbon	1.5K ohms 1/8W
R69	ERD10TJ271	Carbon	270 ohms 1/8W
R70	ERD10TJ681	Carbon	680 ohms 1/8W
R71	ERD10TJ103	Carbon	10K ohms 1/8W
R72	ERD10TJ222	Carbon	2.2K ohms 1/8W
R73-75	ERD10TJ561	Carbon	560 ohms 1/8W
R76,77	ERD10TJ104	Carbon	100K ohms 1/8W
R78	ERD10TJ153	Carbon	15K ohms 1/8W
R79	ERD10TJ681	Carbon	680 ohms 1/8W
R80	ERD10TJ471	Carbon	470 ohms 1/8W
R81	ERD10TJ221	Carbon	220 ohms 1/8W
R82	ERD10TJ681	Carbon	680 ohms 1/8W
R83	ERD10TJ222	Carbon	2.2K ohms 1/8W
R84	ERD10TJ562	Carbon	5.6K ohms 1/8W
R85	ERD10TJ271	Carbon	270 ohms 1/8W
R86	ERD10TJ122	Carbon	1.2K ohms 1/8W
R87	ERD10TJ472	Carbon	4.7K ohms 1/8W
R88	ERD10TJ222	Carbon	2.2K ohms 1/8W
R89	ERD10TJ561	Carbon	560 ohms 1/8W
R90	ERD10TJ271	Carbon	270 ohms 1/8W
R91	ERD10TJ331	Carbon	330 ohms 1/8W
R92	ERD10TJ681	Carbon	680 ohms 1/8W
R93	ERD10TJ562	Carbon	5.6K ohms 1/8W
R94	ERD10TJ681	Carbon	680 ohms 1/8W
R95	ERD10TJ331	Carbon	330 ohms 1/8W
R96	ERD10TJ103	Carbon	10K ohms 1/8W
R97	ERD10TJ102	Carbon	1K ohms 1/8W
R98	ERD10TJ681	Carbon	680 ohms 1/8W
R99	ERD10TJ153	Carbon	15K ohms 1/8W
R100,101	ERD10TJ221	Carbon	220 ohms 1/8W
R102	ERD10TJ182	Carbon	1,8K ohms 1/8W
R103	ERD10TJ681	Carbon	680 ohms 1/8W
R104	ERD10TJ104	Carbon	100K ohms 1/8W
R105	ERD10TJ561	Carbon	560 ohms 1/8W
R106	ERD10TJ152	Carbon	1.5K ohms 1/8W
R107	ERD10TJ272	Carbon	2.7K ohms 1/8W
R108	ERD10TJ221	Carbon	220 ohms 1/8W
R109	ERD10TJ681	Carbon	680 ohms 1/8W

SYMBOL NO.	PART NO.	DESCRIPTION	
R110,111	ERD10TJ271	Carbon	270 ohms 1/8W
R112	ERD10TJ152	Carbon	1.5K ohms 1/8W
R113	ERD10TJ471	Carbon	470 ohms 1/8W
R114,115	ERD10TJ821	Carbon	820 ohms 1/8W
R116	ERD10TJ331	Carbon	330 ohms 1/8W
R118	ERD10TJ271	Carbon	270 ohms 1/8W
R119	ERD10TJ681	Carbon	680 ohms 1/8W
R120	ERD10TJ103	Carbon	10K ohms 1/8W
R121	ERD10TJ104	Carbon	100K ohms 1/8W
R122	ERD10TJ821	Carbon	820 ohms 1/8W
R123	ERD10TJ121	Carbon	120 ohms 1/8W
R124	ERD10TJ122	Carbon	1.2K ohms 1/8W
R125-127	ERD10TJ121	Carbon	120 ohms 1/8W
R128	ERD10TJ122	Carbon	1.2K ohms 1/8W
R129	ERD10TJ152	Carbon	1.5K ohms 1/8W
R130	ERD10TJ221	Carbon	220 ohms 1/8W
R131	ERD10TJ122	Carbon	1.2K ohms 1/8W
R132,133	ERD10TJ121	Carbon	120 ohms 1/8W
R134	ERD10TJ102	Carbon	1K ohms 1/8W
R135	ERD10TJ101	Carbon	100 ohms 1/8W
R136	ERD10TJ104	Carbon	100K ohms 1/8W
R137	ERD10TJ332	Carbon	3.3K ohms 1/8W
R138	ERD10TJ681	Carbon	680 ohms 1/8W
R139	ERD10TJ122	Carbon	1.2K ohms 1/8W
R140	ERD10TJ222	Carbon	2.2K ohms 1/8W
R141	ERD10TJ562	Carbon	5.6K ohms 1/8W
R142	ERD10TJ221	Carbon	220 ohms 1/8W
R143	ERD10TJ681	Carbon	680 ohms 1/8W
R144	ERD10TJ821	Carbon	820 ohms 1/8W
R145	ERD10TJ222	Carbon	2.2K ohms 1/8W
R146	ERD10TJ472	Carbon	4.7K ohms 1/8W
R147	ERD10TJ222	Carbon	2.2K ohms 1/8W
R148	ERD10TJ102	Carbon	1K ohms 1/8W
R149	ERD10TJ271	Carbon	270 ohms 1/8W
R150	ERD10TJ331	Carbon	330 ohms 1/8W
R151	ERD10TJ681	Carbon	680 ohms 1/8W
R152	ERD10TJ562	Carbon	5.6K ohms 1/8W
R153	ERD10TJ681	Carbon	680 ohms 1/8W
R154	ERD10TJ221	Carbon	220 ohms 1/8W
R155	ERD10TJ103	Carbon	10K ohms 1/8W
R156	ERD10TJ561	Carbon	560 ohms 1/8W
R157	ERD10TJ681	Carbon	680 ohms 1/8W
R158	ERD10TJ332	Carbon	3.3K ohms 1/8W
R159	ERD10TJ682	Carbon	6.8K ohms 1/8W
R160,161	ERD10TJ102	Carbon	1K ohms 1/8W
R162	ERD10TJ182	Carbon	1.8K ohms 1/8W
R163	ERD10TJ104	Carbon	100K ohms 1/8W
R164	ERD10TJ332	Carbon	3.3K ohms 1/8W
R165	ERD10TJ272	Carbon	2.7K ohms 1/8W
R166	ERD10TJ122	Carbon	1.2K ohms 1/8W
R167	ERD10TJ101	Carbon	100 ohms 1/8W
R168	ERD10TJ223	Carbon	22K ohms 1/8W
R169	ERD10TJ183	Carbon	18K ohms 1/8W
R170	ERD10TJ222	Carbon	2.2K ohms 1/8W
VR1	YFK12142KB	Variable Resistor	2K ohms
VR2,3	YFK121410KB	Variable Resistor	10K ohms
VR4	YFK12142KB	Variable Resistor	2K ohms

SYMBOL NO.	PART NO.	DESCRIPTION	
VR5-9	YFP0T3321P23	Variable Resistor	2K ohms
VR10	YFP0T3321P52	Variable Resistor	500 ohms
VR11	YFP0T3321P53	Variable Resistor	5K ohms
VR12	YFP0T3321P23	Variable Resistor	2K ohms
VR13,14	YFP0T3321P52	Variable Resistor	500 ohms
VR15	YFP0T3321P23	Variable Resistor	2K ohms
VR16	YFP0T3321P13	Variable Resistor	1K ohms
VR17,18	YFP0T3321P23	Variable Resistor	2K ohms
VR19,20	YFP0T3321P52	Variable Resistor	500 ohms
VR21	YFP0T3321P23	Variable Resistor	2K ohms
VR22	YFP0T3321P52	Variable Resistor	500 ohms
VR23	YFP0T3321P23	Variable Resistor	2K ohms
VR24	YFP0T3321P53	Variable Resistor	5K ohms
VR25,26	YFP0T3321P23	Variable Resistor	2K ohms
VR27-29	YFP0T3321P52	Variable Resistor	500 ohms
VR30	YFP0T3321P13	Variable Resistor	1K ohms
C1,2	ECCF1H180JC	Ceramic	18 pF 50V
C3	ECSF10E47	Electrolytic	47 µF 10V
C4	ECCF1H220JC	Ceramic	22 pF 50V
C5	ECSF10E47	Electrolytic	47 µF 10V
C6	ECCF1H220JC	Ceramic	22 pF 50V
C7	ECCF1H221J	Ceramic	220 pF 50V
C9,10	ECQV05223JZ	Plastic	0.022 µF 50V
C11	ECCF1H070DC	Ceramic	7 pF 50V
C12,13	ECCF1H101JC	Ceramic	100 pF 50V
C14	ECCF1H100JC	Ceramic	10 pF 50V
C17	ECQV05103JZ	Plastic	0.01 µF 50V
C18-20	ECEA1CSS100	Electrolytic	10 µF 16V
C23,24	ECEA1ASS470	Electrolytic	47 µF 10V
C25	ECSF16E33	Electrolytic	33 µF 16V
C26	ECEA1CSS100	Electrolytic	10 µF 16V
C27	ECEA1ASS470	Electrolytic	47 µF 10V
C29	ECCF1H101JC	Ceramic	100 pF 50V
C31	ECCF1H181JC	Ceramic	180 pF 50V
C32	ECSF16E47	Electrolytic	47 µF 16V
C35	ECEA1ASS101	Electrolytic	100 µF 10V
C36-39	ECEA1CSS100	Electrolytic	10 µF 16V
C40	ECCF1H270J	Ceramic	27 pF 50V
C41	ECEA1CSS100	Electrolytic	10 µF 16V
C42	ECQV05104JZ	Plastic	0.1 µF 50V
C43	ECQV05223JZ	Plastic	0.022 µF 50V
C44	ECCF1H270J	Ceramic	27 pF 50V
C45	ECEA1CSS100	Electrolytic	10 µF 16V
C46	ECEA1ASS101	Electrolytic	100 µF 10V
C47	ECEA1ASS470	Electrolytic	47 µF 10V
C48	ECQV05103JZ	Plastic	0.01 µF 50V
C49,50	ECEA1CSS100	Electrolytic	10 µF 16V
C51	ECCF1H270J	Ceramic	27 pF 50V
C52	ECEA1CSS100	Electrolytic	10 µF 16V
C53	ECQV05223JZ	Plastic	0.022 µF 50V
C54,55	ECEA1ASS101	Electrolytic	100 µF 10V
C57,58	ECEA1CSS100	Electrolytic	10 µF 16V
C59	ECCF1H270J	Ceramic	27 pF 50V
C60	ECEA1CSS100	Electrolytic	10 µF 16V
C61	ECQV05104JZ	Plastic	0.1 µF 50V

SYM-BOL NO.	PART NO.	DESCRIPTION	
C62-64	ECCF1H680JC	Ceramic	68 pF 50V
C65	ECCF1H100JC	Ceramic	10 pF 50V
C66	ECSF16E47	Electrolytic	47 µF 16V
C67	ECQV05223JZ	Plastic	0.022 µF 50V
C68	ECCF1H270J	Ceramic	27 pF 50V
C69	ECEA1CSS100	Electrolytic	10 µF 16V
C70	ECEA1ASS101	Electrolytic	100 µF 10V
C71	ECEA1ASS470	Electrolytic	47 µF 10V
C72	ECQV05103JZ	Plastic	0.01 µF 50V
C73,74	ECEA1CSS100	Electrolytic	10 µF 16V
C75	ECCF1H270J	Ceramic	27 pF 50V
C76	ECEA1CSS100	Electrolytic	10 µF 16V
C77	ECQV05223JZ	Plastic	0.022 µF 50V
C78	ECEA1CSS100	Electrolytic	10 µF 16V
C79	ECEA1ASS101	Electrolytic	100 µF 10V
C80,81	ECEA1ASS470	Electrolytic	47 µF 10V
C82	ECCF1H560JC	Ceramic	56 pF 50V
CT1,2	ECV1ZW25X53T	Trimmer Capacitor	25 pF
L3-9	ELEY470KA	Coil	47 µH
SW1,2	YWSSB02206	Slide Switch	
CF1	YFSLC871-197	Filter	
CN1-JM	YFB2B-XH-A	2 pin Jack Male	
CN2-JM	YFB2B-XH-A	2 pin Jack Male	
M36	YFV2SA0110A3	Mounting Angle A	
M37	YFV2PA0050A4	Insulator Plate	

PCB4 INPUT A BOARD
PCB5 INPUT B BOARD
PCB6 INPUT C BOARD

SYM-BOL NO.	PART NO.	DESCRIPTION	
IC1,2	HD14081BP	IC	
IC3	HD14073BP	IC	
IC4,5	YWHD14175BP	IC	
Q1-19	2SD636-RS	Transistor	
Q20-28	2SD639RS	Transistor	
D1-8	MA162	Diode	
D10-17	MA162	Diode	
R1-4	ERD25FJ563	Carbon	56K ohms 1/4W
R6	ERD25FJ103	Carbon	10K ohms 1/4W
R7	ERD25FJ563	Carbon	56K ohms 1/4W
R8	ERD25FJ221	Carbon	220 ohms 1/4W
R9	ERD25FJ103	Carbon	10K ohms 1/4W
R10	ERD25FJ221	Carbon	220 ohms 1/4W
R11	ERD25FJ103	Carbon	10K ohms 1/4W
R12	ERD25FJ221	Carbon	220 ohms 1/4W
R13	ERD25FJ103	Carbon	10K ohms 1/4W
R14	ERD25FJ221	Carbon	220 ohms 1/4W
R15	ERD25FJ103	Carbon	10K ohms 1/4W
R16	ERD25FJ221	Carbon	220 ohms 1/4W
R17	ERD25FJ103	Carbon	10K ohms 1/4W
R18	ERD25FJ221	Carbon	220 ohms 1/4W
R19	ERD25FJ103	Carbon	10K ohms 1/4W
R20	ERD25FJ221	Carbon	220 ohms 1/4W
R21	ERD25FJ103	Carbon	10K ohms 1/4W
R22	ERD25FJ221	Carbon	220 ohms 1/4W
R23	ERD25FJ103	Carbon	10K ohms 1/4W

SYM-BOL NO.	PART NO.	DESCRIPTION	
R24	ERD25FJ332	Carbon	3.3K ohms 1/4W
R25	ERD25FJ221	Carbon	220 ohms 1/4W
R26	ERD25FJ102	Carbon	1K ohms 1/4W
R27	ERD25FJ563	Carbon	56K ohms 1/4W
R28	ERD25FJ472	Carbon	4.7K ohms 1/4W
R29,30	ERD25FJ103	Carbon	10K ohms 1/4W
R31	ERD25FJ102	Carbon	1K ohms 1/4W
R32-47	ERD25FJ103	Carbon	10K ohms 1/4W
R48	ERG12ANJ181	Metal	180 ohms 1/2W
R49	ERD25FJ103	Carbon	10K ohms 1/4W
R50	ERG1ANJ150	Metal	15 ohms 1W
C1	ECEA1VSS4R7	Electrolytic	4.7 µF 35V
C2	ECEA1ASS101	Electrolytic	100 µF 10V
SW3	YW8FL1EC0421	8 Channel Switch	
E10	* WMT4X1R2X5	Insulator	
M38	YWJ5500FR02B	Mounting Guide	

PCB7 INPUT PV-PG BOARD

SYM-BOL NO.	PART NO.	DESCRIPTION	
IC1,2	HD14081BP	IC	
IC3	HD14073BP	IC	
IC4	HD14011BP	IC	
IC5	HD14174BP	IC	
IC6	YWHD14175BP	IC	
IC7	HD14013BP	IC	
Q1-20	2SD636-RS	Transistor	
Q21-31	2SD639RS	Transistor	
D1-18	MA162	Diode	
R1	ERD25FJ103	Carbon	10K ohms 1/4W
R2	ERD25FJ221	Carbon	220 ohms 1/4W
R3	ERD25FJ103	Carbon	10K ohms 1/4W
R4	ERD25FJ221	Carbon	220 ohms 1/4W
R5	ERD25FJ103	Carbon	10K ohms 1/4W
R6	ERD25FJ221	Carbon	220 ohms 1/4W
R7	ERD25FJ103	Carbon	10K ohms 1/4W
R8	ERD25FJ221	Carbon	220 ohms 1/4W
R9	ERD25FJ103	Carbon	10K ohms 1/4W
R10	ERD25FJ221	Carbon	220 ohms 1/4W
R11	ERD25FJ103	Carbon	10K ohms 1/4W
R12	ERD25FJ221	Carbon	220 ohms 1/4W
R13	ERD25FJ103	Carbon	10K ohms 1/4W
R14	ERD25FJ221	Carbon	220 ohms 1/4W
R15	ERD25FJ103	Carbon	10K ohms 1/4W
R16	ERD25FJ221	Carbon	220 ohms 1/4W
R17	ERD25FJ153	Carbon	15K ohms 1/4W
R18,19	ERD25FJ103	Carbon	10K ohms 1/4W
R20	ERD25FJ102	Carbon	1K ohms 1/4W
R21	ERD25FJ221	Carbon	220 ohms 1/4W
R22	ERD25FJ102	Carbon	1K ohms 1/4W
R23	ERD25FJ563	Carbon	56K ohms 1/4W
R24	ERD25FJ472	Carbon	4.7K ohms 1/4W
R25	ERD25FJ103	Carbon	10K ohms 1/4W
R26	ERD25FJ563	Carbon	56K ohms 1/4W
R27,28	ERD25FJ153	Carbon	15K ohms 1/4W
R29	ERD25FJ102	Carbon	1K ohms 1/4W

SYMBOL NO.	PART NO.	DESCRIPTION	
R30	ERG1ANJ150	Metal	15 ohms 1W
R31	ERD25FJ102	Carbon	1K ohms 1/4W
R32-52	ERD25FJ103	Carbon	10K ohms 1/4W
R53	ERG12ANJ181	Metal	180 ohms 1/2W
R54	ERD25FJ103	Carbon	10K ohms 1/4W
C1	ECEA1CSS221	Electrolytic	220 μF 16V
C2	ECEA1VSS4R7	Electrolytic	4.7 μF 35V
C3	ECEA1CSS100	Electrolytic	10 μF 16V
SW4	YW10FL1EC02	10 Channel Push Switch	
E10	* WMT4X1R2X5	Insulator	
M38	YWJ5500FR02B	Mounting Guide for Switch	

PCB8 WIPE PROCESS BOARD

SYMBOL NO.	PART NO.	DESCRIPTION	
IC1	HD14081BP	IC	
IC2,3	YWHD14175BP	IC	
IC4	HD14027BP	IC	
IC5	HD14053BP	IC	
Q1-7	2SD639RS	Transistor	
Q8,9	2SD636-RS	Transistor	
Q10	2SA1254-BC	Transistor	
Q11	2SC2377CD	Transistor	
Q12-15	2SD636-RS	Transistor	
Q16-18	2SC2377CD	Transistor	
Q19	2SA1254-BC	Transistor	
Q20	2SC2377CD	Transistor	
Q21,22	2SD636-RS	Transistor	
Q23,24	2SC2377CD	Transistor	
Q25,26	2SD636-RS	Transistor	
Q27	2SA1254-BC	Transistor	
Q28	2SC2377CD	Transistor	
Q29-31	2SD636-RS	Transistor	
Q32	2SC1216F	Transistor	
Q33-35	2SC2377CD	Transistor	
Q36	2SA1254-BC	Transistor	
Q37	2SC1216F	Transistor	
Q38-42	2SD636-RS	Transistor	
Q43	2SC2377CD	Transistor	
Q44	2SA1254-BC	Transistor	
Q45-47	2SD636-RS	Transistor	
D1-21	MA165	Diode	
D201-205	MA165	Diode	
R1	ERG1ANJ150	Metal	15 ohms 1W
R2	ERD10TJ472	Carbon	4.7K ohms 1/8W
R3	ERD10TJ103	Carbon	10K ohms 1/8W
R4	ERD10TJ472	Carbon	4.7K ohms 1/8W
R5	ERD10TJ102	Carbon	1K ohms 1/8W
R6-11	ERD10TJ103	Carbon	10K ohms 1/8W
R12	ERD10TJ472	Carbon	4.7K ohms 1/8W
R13	ERG1ANJ150	Metal	15 ohms 1W
R14	ERD10TJ102	Carbon	1K ohms 1/8W
R15-20	ERD10TJ103	Carbon	10K ohms 1/8W
R21	ERG1ANJ150	Metal	15 ohms 1W

SYMBOL NO.	PART NO.	DESCRIPTION	
R22	ERD10TJ563	Carbon	56K ohms 1/8W
R23	ERD10TJ562	Carbon	5.6K ohms 1/8W
R24	ERD10TJ223	Carbon	22K ohms 1/8W
R25	ERD10TJ272	Carbon	2.7K ohms 1/8W
R26	ERD10TJ103	Carbon	10K ohms 1/8W
R27	ERD10TJ223	Carbon	22K ohms 1/8W
R28	ERD10TJ153	Carbon	15K ohms 1/8W
R29,30	ERD10TJ561	Carbon	560 ohms 1/8W
R31	ERD10TJ223	Carbon	22K ohms 1/8W
R32	ERD10TJ153	Carbon	15K ohms 1/8W
R33	ERD10TJ102	Carbon	1K ohms 1/8W
R34,35	ERD10TJ103	Carbon	10K ohms 1/8W
R36	ERD10TJ821	Carbon	820 ohms 1/8W
R37	ERD10TJ471	Carbon	470 ohms 1/8W
R38	ERD10TJ122	Carbon	1.2K ohms 1/8W
R39	ERD10TJ332	Carbon	3.3K ohms 1/8W
R40	ERD10TJ471	Carbon	470 ohms 1/8W
R41	ERD10TJ122	Carbon	1.2K ohms 1/8W
R42	ERD10TJ222	Carbon	2.2K ohms 1/8W
R43	ERD10TJ103	Carbon	10K ohms 1/8W
R44	ERD10TJ221	Carbon	220 ohms 1/8W
R45	ERD10TJ681	Carbon	680 ohms 1/8W
R46	ERD10TJ103	Carbon	10K ohms 1/8W
R47	ERD10TJ821	Carbon	820 ohms 1/8W
R48	ERD10TJ103	Carbon	10K ohms 1/8W
R49	ERD10TJ332	Carbon	3.3K ohms 1/8W
R50,51	ERD10TJ103	Carbon	10K ohms 1/8W
R52	ERD10TJ562	Carbon	5.6K ohms 1/8W
R53	ERD10TJ152	Carbon	1.5K ohms 1/8W
R54	ERD10TJ103	Carbon	10K ohms 1/8W
R56	ERD10TJ152	Carbon	1.5K ohms 1/8W
R57	ERD10TJ103	Carbon	10K ohms 1/8W
R58,59	ERD10TJ153	Carbon	15K ohms 1/8W
R60,61	ERD10TJ103	Carbon	10K ohms 1/8W
R62,63	ERD10TJ152	Carbon	1.5K ohms 1/8W
R64,65	ERD10TJ103	Carbon	10K ohms 1/8W
R66,67	ERD10TJ153	Carbon	15K ohms 1/8W
R68	ERD10TJ104	Carbon	100K ohms 1/8W
R69	ERD10TJ223	Carbon	22K ohms 1/8W
R70	ERD10TJ153	Carbon	15K ohms 1/8W
R71,72	ERD10TJ561	Carbon	560 ohms 1/8W
R73	ERD10TJ223	Carbon	22K ohms 1/8W
R74	ERD10TJ153	Carbon	15K ohms 1/8W
R75	ERD10TJ102	Carbon	1K ohms 1/8W
R76,77	ERD10TJ103	Carbon	10K ohms 1/8W
R78	ERD10TJ821	Carbon	820 ohms 1/8W
R79	ERD10TJ471	Carbon	470 ohms 1/8W
R80	ERD10TJ122	Carbon	1.2K ohms 1/8W
R81	ERD10TJ102	Carbon	1K ohms 1/8W
R82	ERD10TJ103	Carbon	10K ohms 1/8W
R83	ERD10TJ102	Carbon	1K ohms 1/8W
R84	ERD10TJ222	Carbon	2.2K ohms 1/8W
R85,86	ERD10TJ103	Carbon	10K ohms 1/8W
R87	ERD10TJ562	Carbon	5.6K ohms 1/8W
R88	ERD10TJ221	Carbon	220 ohms 1/8W
R89	ERD10TJ681	Carbon	680 ohms 1/8W

MODEL WJ-5600

SYM-BOL NO.	PART NO.	DESCRIPTION	
R90	ERD10TJ332	Carbon	3.3K ohms 1/8W
R91	ERD10TJ681	Carbon	680 ohms 1/8W
R92-95	ERD10TJ103	Carbon	10K ohms 1/8W
R96	ERD10TJ222	Carbon	2.2K ohms 1/8W
R97	ERD10TJ562	Carbon	5.6K ohms 1/8W
R98	ERD10TJ152	Carbon	1.5K ohms 1/8W
R100	ERD10TJ103	Carbon	10K ohms 1/8W
R101	ERD10TJ102	Carbon	1K ohms 1/8W
R102,103	ERD10TJ103	Carbon	10K ohms 1/8W
R104	ERD10TJ562	Carbon	5.6K ohms 1/8W
R105	ERD10TJ152	Carbon	1.5K ohms 1/8W
R106	ERD10TJ103	Carbon	10K ohms 1/8W
R107,108	ERD10TJ222	Carbon	2.2K ohms 1/8W
R109	ERD10TJ103	Carbon	10K ohms 1/8W
R111,112	ERD10TJ103	Carbon	10K ohms 1/8W
R113	ERD10TJ222	Carbon	2.2K ohms 1/8W
R114	ERD10TJ103	Carbon	10K ohms 1/8W
R115	ERD10TJ562	Carbon	5.6K ohms 1/8W
R116	ERD10TJ103	Carbon	10K ohms 1/8W
R117	ERD10TJ332	Carbon	3.3K ohms 1/8W
R201	ERD10TJ333	Carbon	33K ohms 1/8W
R202	ERD10TJ752	Carbon	7.5K ohms 1/8W
R203	ERD10TJ683	Carbon	68K ohms 1/8W
R204	ERD10TJ392	Carbon	3.9K ohms 1/8W
R205	ERD10TJ752	Carbon	7.5K ohms 1/8W
VR1-4	YFP0T3321P13	Variable Resistor	1K ohms
C1	ECEA1VSS4R7	Electrolytic	4.7 μF 35V
C2	ECEA1CSS101	Electrolytic	100 μF 16V
C3	ECEA1ASS101	Electrolytic	100 μF 10V
C4,5	ECQV05393JZ	Plastic	0.039 μF 50V
C6	ECEA1CSS100	Electrolytic	10 μF 16V
C7	ECEA1ASS101	Electrolytic	100 μF 10V
C8	ECSF35ER47	Electrolytic	0.47 μF 35V
C9,10	ECEA1ASS470	Electrolytic	47 μF 10V
C11	ECEA1ASS220	Electrolytic	22 μF 10V
C12,13	ECQM1222KZ	Plastic	2200 pF 100V
C14-16	ECEA1ASS101	Electrolytic	100 μF 10V
C17 18	ECEA1CSS100	Electrolytic	10 μF 16V
C19	ECQP1102JZ	Plastic	1000 pF 100V
C20	ECEA1ASS220	Electrolytic	22 μF 10V
C21	ECCF1H121JR	Ceramic	120PF 50V
C22	ECCF1H101JC	Ceramic	100 pF 50V
C23	ECCF1H271K	Ceramic	270PF 50V
SW5,6	YF3F1C0472VB	3 Channel Switch	
SW7	YF1F5C0472VC	1 Channel Switch	
M38	YWJ5500FR02B	Mounting Guide for Switch	

PCB9 WAVEFORM GEN. BOARD

SYM-BOL NO.	PART NO.	DESCRIPTION	
IC1	ED14174BP	IC	
IC2	MC14077BP	IC	
IC3,4	DN850	IC	
Q1-5	2SD639RS	Transistor	
Q6,7	2SB641-RS	Transistor	
Q8,9	2SD636-RS	Transistor	
Q10-12	2SB641-RS	Transistor	
Q13-15	2SD636-RS	Transistor	
Q16	2SB641-RS	Transistor	
Q17-19	2SD636-RS	Transistor	
Q20	2SB641-RS	Transistor	
Q21-26	2SD636-RS	Transistor	
Q27	2SB641-RS	Transistor	
Q28	2SD636-RS	Transistor	
Q29	2SB641-RS	Transistor	
Q30-34	2SD636-RS	Transistor	
Q35	2SB641-RS	Transistor	
Q36	2SD636-RS	Transistor	
D1-21	MA165	Diode	
D22	YUD-XZ051	Diode	
R1	ERG1ANJ150	Metal	15 ohms 1W
R2	ERD10TJ102	Carbon	1K ohms 1/8W
R3-13	ERD10TJ103	Carbon	10K ohms 1/8W
R14-18	ERD10TJ472	Carbon	4.7K ohms 1/8W
R19	ERD10TJ563	Carbon	56K ohms 1/8W
R20	ERD10TJ222	Carbon	2.2K ohms 1/8W
R21	ERD10TJ153	Carbon	15K ohms 1/8W
R22,23	ERD10TJ822	Carbon	8.2K ohms 1/8W
R24	ERD10TJ152	Carbon	1.5K ohms 1/8W
R25	ERD10TJ103	Carbon	10K ohms 1/8W
R26	ERD10TJ562	Carbon	5.6K ohms 1/8W
R27	ERD10TJ222	Carbon	2.2K ohms 1/8W
R28	ERD10TJ103	Carbon	10K ohms 1/8W
R29	ERD10TJ473	Carbon	47K ohms 1/8W
R30	ERD10TJ332	Carbon	3.3K ohms 1/8W
R31	ERD10TJ103	Carbon	10K ohms 1/8W
R32	ERD10TJ562	Carbon	5.6K ohms 1/8W
R33	ERD10TJ680	Carbon	68 ohms 1/8W
R34	ERD10TJ152	Carbon	1.5K ohms 1/8W
R35	ERD10TJ562	Carbon	5.6K ohms 1/8W
R36	ERD10TJ153	Carbon	15K ohms 1/8W
R37,38	ERD10TJ682	Carbon	6.8K ohms 1/8W
R39	ERD10TJ152	Carbon	1.5K ohms 1/8W
R40	ERD10TJ103	Carbon	10K ohms 1/8W
R41	ERD10TJ562	Carbon	5.6K ohms 1/8W
R42	ERD10TJ222	Carbon	2.2K ohms 1/8W
R43	ERD10TJ103	Carbon	10K ohms 1/8W
R44	ERD10TJ333	Carbon	33K ohms 1/8W
R45	ERD10TJ332	Carbon	3.3K ohms 1/8W
R46,47	ERD10TJ103	Carbon	10K ohms 1/8W
R48	ERD10TJ821	Carbon	820 ohms 1/8W
R49	ERD10TJ332	Carbon	3.3K ohms 1/8W
R50	ERD10TJ562	Carbon	5.6K ohms 1/8W
R51	ERD10TJ102	Carbon	1K ohms 1/8W
R52	ERD10TJ101	Carbon	100 ohms 1/8W
R53	ERD10TJ681	Carbon	680 ohms 1/8W
R54,55	ERD10TJ562	Carbon	5.6K ohms 1/8W
R56	ERD10TJ471	Carbon	470 ohms 1/8W
R57	ERD10TJ472	Carbon	4.7K ohms 1/8W
R58	ERD10TJ242	Carbon	2.4K ohms 1/8W
R59	ERD10TJ221	Carbon	220 ohms 1/8W
R60	ERD10TJ332	Carbon	3.3K ohms 1/8W
R61	ERD10TJ221	Carbon	220 ohms 1/8W
R62	ERD10TJ123	Carbon	12K ohms 1/8W
R63	ERD10TJ152	Carbon	1.5K ohms 1/8W

SYMBOL NO.	PART NO.	DESCRIPTION	
R64	ERD10TJ272	Carbon	2.7K ohms 1/8W
R65	ERD10TJ562	Carbon	5.6K ohms 1/8W
R66	ERD10TJ103	Carbon	10K ohms 1/8W
R67	ERD10TJ821	Carbon	820 ohms 1/8W
R68,69	ERD10TJ332	Carbon	3.3K ohms 1/8W
R70	ERD10TJ103	Carbon	10K ohms 1/8W
R71	ERD10TJ332	Carbon	3.3K ohms 1/8W
R72,73	ERD10TJ103	Carbon	10K ohms 1/8W
R74	ERD10TJ332	Carbon	3.3K ohms 1/8W
R75	ERD10TJ391	Carbon	390 ohms 1/8W
R76	ERD10TJ562	Carbon	5.6K ohms 1/8W
R77,78	ERD10TJ560	Carbon	56 ohms 1/8W
R79	ERD10TJ681	Carbon	680 ohms 1/8W
R80	ERD10TJ472	Carbon	4.7K ohms 1/8W
R81	ERD10TJ562	Carbon	5.6K ohms 1/8W
R82	ERD10TJ471	Carbon	470 ohms 1/8W
R83	ERD10TJ100	Carbon	10 ohms 1/8W
R84	ERD10TJ471	Carbon	470 ohms 1/8W
R85-87	ERD10TJ562	Carbon	5.6K ohms 1/8W
R88,89	ERD10TJ221	Carbon	220 ohms 1/8W
R90	ERD10TJ273	Carbon	27K ohms 1/8W
R91	ERD10TJ153	Carbon	15K ohms 1/8W
R92	ERD10TJ222	Carbon	2.2K ohms 1/8W
R93	ERD10TJ562	Carbon	5.6K ohms 1/8W
R94	ERD10TJ102	Carbon	1K ohms 1/8W
R95	ERD10TJ221	Carbon	220 ohms 1/8W
R96	ERD10TJ123	Carbon	12K ohms 1/8W
R97	ERD10TJ122	Carbon	1.2K ohms 1/8W
R98	ERD10TJ123	Carbon	12K ohms 1/8W
R99	ERD10TJ152	Carbon	1.5K ohms 1/8W
R100	ERD10TJ272	Carbon	2.7K ohms 1/8W
R101	ERD10TJ222	Carbon	2.2K ohms 1/8W
R201	ERD10TJ562	Carbon	5.6K ohms 1/8W
VR1-3	YFP0T3321P54	Variable Resistor	50K ohms
VR4	YFP0T3321P13	Variable Resistor	1K ohms
VR5-7	YFP0T3321P54	Variable Resistor	50K ohms
VR8-13	YFP0T3321P13	Variable Resistor	1K ohms
C2	ECEA1ASS101	Electrolytic	100 μF 10V
C3	ECEA1VSS4R7	Electrolytic	4.7 μF 35V
C4	ECQV05333JZ	Plastic	0.033 μF 50V
C5	ECEA1ASS101	Electrolytic	100 μF 10V
C6	ECSF35ER47	Electrolytic	0.47 μF 35V
C7	ECEA1ASS101	Electrolytic	100 μF 10V
C8,9	ECSF35ER47	Electrolytic	0.47 μF 35V
C10	ECEA1ESS470	Electrolytic	47 μF 25V
C11	ECEA1CSS100	Electrolytic	10 μF 16V
C12	ECCF1H101JC	Ceramic	100 pF 50V
C13	ECEA1CSS100	Electrolytic	10 μF 16V
C14,15	ECQV05103JZ	Plastic	0.01 μF 50V
C16	ECQM1222KZ	Plastic	2200 pF 100V
C17	ECEA1ASS101	Electrolytic	100 μF 10V
C18,19	ECQM1222KZ	Plastic	2200 pF 100V
C20	ECEA1ESS100	Electrolytic	10 μF 25V
C21	ECCF1H101JC	Ceramic	100 pF 50V
C22,23	ECEA1CSS100	Electrolytic	10 μF 16V
C24,25	ECQV05103JZ	Plastic	0.01 μF 50V
C26	ECEA1CSS100	Electrolytic	10 μF 16V
C27	ECQV05103JZ	Plastic	0.01 μF 50V
C28	ECEA1CSS100	Electrolytic	10 μF 16V

SYMBOL NO.	PART NO.	DESCRIPTION	
C29	ECCW1H300JC	Ceramic	30PF 50V
C30	ECEA1ASS470	Electrolytic	47 μF 10V
C31,32	ECSF16E4R7	Electrolytic	4.7 μF 16V
C33	ECEA1ASS470	Electrolytic	47 μF 10V
C34,35	ECSF16E4R7	Electrolytic	4.7 μF 16V
C36-38	ECEA1ASS470	Electrolytic	47 μF 10V
C39	ECSF35ER47	Electrolytic	0.47 μF 35V
C40	ECEA1CSS100	Electrolytic	10 μF 16V
C41	ECQV05103JZ	Plastic	0.01 μF 50V
C42	ECQV05333JZ	Plastic	0.033 μF 50V
L1,2	ELEY470KA	Coil	47 μH
SW5	YF5F2C0472VC	5 Channel Push Switch	
E10	*WMT4X1R2X5	Insulator	
M38	YWJ5500FR02B	Mounting Guide	

PCB10 MODULATION BOARD

IC1	HD14081BP	IC	
IC2	HD14174BP	IC	
IC3	HD14071BP	IC	
IC4	NJM4558D	IC	
IC5	TWHD14052BP	IC	
Q1-5	2SD639RS	Transistor	
Q6,7	2SD636-RS	Transistor	
Q8	2SB641-RS	Transistor	
Q9,10	2SD636-RS	Transistor	
Q11	2SC1216F	Transistor	
Q12	2SD636-RS	Transistor	
Q13	2SC1216F	Transistor	
Q14	2SB644-RS	Transistor	
Q15	2SD636-RS	Transistor	
Q16	2SB641-RS	Transistor	
Q17,18	2SD636-RS	Transistor	
Q19,20	2SB641-RS	Transistor	
Q21~24	2SD636-RS	Transistor	
Q25	2SK19-Y	Transistor	
Q26	2SK34-CD	Transistor	
D1-15	MA165	Diode	
D16,17	XZ031	Diode	
D18	MA4047L	Diode	
D19,20	MA165	Diode	
D21	MA27A	Diode	
D201	MA27A	Diode	
D202,203	XZ031	Diode	
R1	ERG1ANJ150	Metal	15 ohms 1W
R2	ERD10TJ472	Carbon	4.7K ohms 1/8W
R3-12	ERD10TJ103	Carbon	10K ohms 1/8W
R13	ERD10TJ472	Carbon	4.7K ohms 1/8W
R14	ERD10TJ103	Carbon	10K ohms 1/8W
R16	ERD10TJ101	Carbon	100 ohms 1/8W
R17	ERD10TJ821	Carbon	820 ohms 1/8W
R18,19	ERD10TJ561	Carbon	560 ohms 1/8W
R20	ERD10TJ101	Carbon	100 ohms 1/8W
R21	ERD10TJ561	Carbon	560 ohms 1/8W
R22	ERD10TJ821	Carbon	820 ohms 1/8W
R23	ERD10TJ101	Carbon	100 ohms 1/8W
R24	ERD10TJ682	Carbon	6.8K ohms 1/8W
R25	ERD10TJ222	Carbon	2.2K ohms 1/8W
R26	ERD10TJ102	Carbon	1K ohms 1/8W
R27	ERD10TJ391	Carbon	390 ohms 1/8W

MODEL WJ-5600

SYM-BOL NO.	PART NO.	DESCRIPTION	
R28	ERD10TJ242	Carbon	2.4K ohms 1/8W
R29	ERD10TJ102	Carbon	1K ohms 1/8W
R30	ERD10TJ472	Carbon	4.7K ohms 1/8W
R31	ERD10TJ103	Carbon	10K ohms 1/8W
R32	ERD10TJ101	Carbon	100 ohms 1/8W
R33	ERD10TJ102	Carbon	1K ohms 1/8W
R39	ERD10TJ472	Carbon	4.7K ohms 1/8W
R41	ERD10TJ221	Carbon	220 ohms 1/8W
R43	ERD10TJ330	Carbon	33 ohms 1/8W
R44,45	ERD10TJ102	Carbon	1K ohms 1/8W
R46	ERD10TJ103	Carbon	10K ohms 1/8W
R47	ERD10TJ221	Carbon	220 ohms 1/8W
R48	ERD10TJ152	Carbon	1.5K ohms 1/8W
R49	ERD10TJ103	Carbon	10K ohms 1/8W
R50	ERD10TJ102	Carbon	1K ohms 1/8W
R51	ERD10TJ332	Carbon	3.3K ohms 1/8W
R52	ERD10TJ222	Carbon	2.2K ohms 1/8W
R53	ERD10TJ221	Carbon	220 ohms 1/8W
R54	ERD10TJ222	Carbon	2.2K ohms 1/8W
R55	ERD10TJ272	Carbon	2.7K ohms 1/8W
R56	ERD10TJ122	Carbon	1.2K ohms 1/8W
R57	ERD10TJ101	Carbon	100 ohms 1/8W
R58	ERD10TJ392	Carbon	3.9K ohms 1/8W
R59	ERD10TJ222	Carbon	2.2K ohms 1/8W
R60	ERD10TJ331	Carbon	330 ohms 1/8W
R61	ERD10TJ561	Carbon	560 ohms 1/8W
R62	ERD10TJ152	Carbon	1.5K ohms 1/8W
R63	ERD10TJ223	Carbon	22K ohms 1/8W
R64	ERD10TJ332	Carbon	3.3K ohms 1/8W
R65	ERD10TJ104	Carbon	100K ohms 1/8W
R67	ERD10TJ153	Carbon	15K ohms 1/8W
R68	ERD10TJ223	Carbon	22K ohms 1/8W
R201	ERD10TJ222	Carbon	2.2K ohms 1/8W
R202	ERD10TJ223	Carbon	22K ohms 1/8W
R203	ERD10TJ103	Carbon	10K ohms 1/8W
R204	ERD10TJ224	Carbon	220K ohms 1/8W
R205	ERD10TJ334	Carbon	330K ohms 1/8W
R206	ERD10TJ821	Carbon	820 ohms 1/8W
R80	ERD10TJ681	Carbon	680 ohms 1/8W
VR1	YFK1214500B	Variable Resistor	500 ohms
VR2	YFK121420KB	Variable Resistor	20K ohms
VR3	YFK12145KB	Variable Resistor	5K ohms
VR4	YFP0T3321P23	Variable Resistor	2K ohms
VR5,6	YFP0T3321P13	Variable Resistor	1K ohms
VR7	YFP0T3321P23	Variable Resistor	2K ohms
VR8	YFP0T3321P13	Variable Resistor	1K ohms
VR9,10	YFP0T3321P53	Variavle Resistor	5K ohms
VR11	YFP0T3321P25	Variable Resistor	200K ohms
C1	ECEA1ESS101	Electrolytic	100 µF 25V
C2	ECEA1ASS101	Electrolytic	100 µF 10V
C3	ECEA1VSS4R7	Electrolytic	4.7 µF 35V
C4	ECEA1ASS470	Electrolytic	47 µF 10V
C5	ECEA1ASS101	Electrolytic	100 µF 10V
C6	ECQP1102JZ	Plastic	1000 pF 100V
C7,8	ECQS1563JZ	Plastic	0.056µF 100V
C9	ECEA1ASS101	Electrolytic	100 µF 10V
C10	ECEA1ASS220	Electrolytic	22 µF 10V
C11	ECEA1CSS100	Electrolytic	10 µF 16V
C12	ECCF1H270JC	Ceramic	27 pF 50V
C13	ECEA1CSS100	Electrolytic	10 µF 16V
C14	ECQV05223JZ	Plastic	0.022 µF 50V
C15	ECEA1HS010	Electrolytic	1µF 50V
C16	ECEA1CSS100	Electrolytic	10µF 16V

SYM-BOL NO.	PART NO.	DESCRIPTION	
C18	ECEA1CSS100	Electrolytic	10 µF 16V
C201	ECCF1H332JC	Ceramic	3300pF 50V
L1	ELEY470KA	Coil	47 µH
SW10	YF5F2C0472VC	5 Channel Push Switch	
E10	*WMT4X1R2X5	Insulator	
M38	YWJ5500FR02B	Mounting Guide	
M43	*YFV2SA0111A4	Mounting Angle	

PCB11 SYNC, C/BAR BOARD

SYM-BOL NO.	PART NO.	DESCRIPTION	
IC1	HD14572UBP	IC	
IC2	YWHD14516BP	IC	
IC3	HA11720	IC	
IC4	AN78N05	IC	
IC5	TC40H002P	IC	
IC6	YWHD74LS221P	IC	
IC7	YWHD74LS107P	IC	
IC8	MP7260	IC	
IC9	TC40H002P	IC	
IC10	YWHD74LS04P	IC	
Q1	2SC641K-C	Transistor	
Q2	2SD636-RS	Transistor	
Q3	2SB641-RS	Transistor	
Q4-7	2SD636-RS	Transistor	
Q8	2SB641-RS	Transistor	
Q9	2SD636-RS	Transistor	
Q10	2SB641-RS	Transistor	
Q11-14	2SD636-RS	Transistor	
Q15	2SB641-RS	Transistor	
Q16-19	2SD636-RS	Transistor	
Q20	2SC641K-C	Transistor	
Q21	2SD636-RS	Transistor	
Q22	2SB641-RS	Transistor	
Q23	2SC641K-C	Transistor	
Q24,25	2SD636-RS	Transistor	
Q26	2SB641-RS	Transistor	
Q27-32	2SD636-RS	Transistor	
Q33	2SB641-RS	Transistor	
D1-5	MA165	Diode	
D6-8	YUD1S2688	Diode	
R1	ERD10TJ473	Carbon	47K ohms 1/8W
R2,3	ERD10TJ104	Carbon	100K ohms 1/8W
R4	ERD10TJ472	Carbon	4.7K ohms 1/8W
R5	ERD10TJ103	Carbon	10K ohms 1/8W
R6	ERD10TJ153	Carbon	15K ohms 1/8W
R7,8	ERD10TJ223	Carbon	22K ohms 1/8W
R9	ER0S2CKF4702	Metal	47K ohms 1/8W
R10	ER0S2CKF6801	Metal	6.8K ohms 1/8W
R11	ER0S2CKF1502	Metal	15K ohms 1/8W
R12	ER0S2CKF4701	Metal	4.7K ohms 1/8W
R13	ER0S2CKF1002	Metal	10K ohms 1/8W
R14	ER0S2CKF5600	Metal	560 ohms 1/8W
R15	ER0S2CKF1002	Metal	10K ohms 1/8W
R16	ER0S2CKF8201	Metal	8.2K ohms 1/8W
R17	ERD10TJ102	Carbon	1K ohms 1/8W
R18	ERD10TJ682	Carbon	6.8K ohms 1/8W
R19	ERD10TJ392	Carbon	3.9K ohms 1/8W
R20	ERD10TJ333	Carbon	33K ohms 1/8W

SYMBOL NO.	PART NO.	DESCRIPTION	
R21	ERD10TJ332	Carbon	3.3K ohms 1/8W
R22	ERD10TJ561	Carbon	560 ohms 1/8W
R23	ERD10TJ562	Carbon	5.6K ohms 1/8W
R24	ERD10TJ333	Carbon	33K ohms 1/8W
R25	ERD10TJ332	Carbon	3.3K ohms 1/8W
R26	ERD10TJ102	Carbon	1K ohms 1/8W
R27	ERD10TJ562	Carbon	5.6K ohms 1/8W
R28	ERD10TJ682	Carbon	6.8K ohms 1/8W
R29	ERD10TJ332	Carbon	3.3K ohms 1/8W
R30	ERD10TJ392	Carbon	3.9K ohms 1/8W
R31	ERD10TJ102	Carbon	1K ohms 1/8W
R32	ERD10TJ182	Carbon	1.8K ohms 1/8W
R33	ERD10TJ222	Carbon	2.2K ohms 1/8W
R34	ERD10TJ182	Carbon	1.8K ohms 1/8W
R35	ERD10TJ392	Carbon	3.9K ohms 1/8W
R36	ERD10TJ332	Carbon	3.3K ohms 1/8W
R37	ERD10TJ392	Carbon	3.9K ohms 1/8W
R38	ERD10TJ102	Carbon	1K ohms 1/8W
R39	ERD10TJ182	Carbon	1.8K ohms 1/8W
R40	ERD10TJ222	Carbon	2.2K ohms 1/8W
R41	ERD10TJ182	Carbon	1.8K ohms 1/8W
R42,43	ERD10TJ102	Carbon	1K ohms 1/8W
R44	ERD10TJ563	Carbon	56K ohms 1/8W
R45	ERD10TJ472	Carbon	4.7K ohms 1/8W
R46	ERD10TJ563	Carbon	56K ohms 1/8W
R47	ERD10TJ472	Carbon	4.7K ohms 1/8W
R48	ERD10TJ333	Carbon	33K ohms 1/8W
R49	ERD10TJ153	Carbon	15K ohms 1/8W
R50	ERD10TJ471	Carbon	470 ohms 1/8W
R51	ERD10TJ102	Carbon	1K ohms 1/8W
R52	ERD10TJ562	Carbon	5.6K ohms 1/8W
R53	ERD10TJ102	Carbon	1K ohms 1/8W
R54	ERD10TJ471	Carbon	470 ohms 1/8W
R55	ERD10TJ821	Carbon	820 ohms 1/8W
R56	ERD10TJ103	Carbon	10K ohms 1/8W
R57	ERD10TJ102	Carbon	1K ohms 1/8W
R58	ERD10TJ331	Carbon	330 ohms 1/8W
R59	ERD10TJ272	Carbon	2.7K ohms 1/8W
R60	ERD10TJ222	Carbon	2.2K ohms 1/8W
R61	ERD10TJ123	Carbon	12K ohms 1/8W
R62	ERD10TJ152	Carbon	1.5K ohms 1/8W
R63	ERD10TJ102	Carbon	1K ohms 1/8W
R64	ERD10TJ222	Carbon	2.2K ohms 1/8W
R65	ERD10TJ332	Carbon	3.3K ohms 1/8W
R66	ERD10TJ102	Carbon	1K ohms 1/8W
R67	ERD10TJ152	Carbon	1.5K ohms 1/8W
R68	ERD10TJ123	Carbon	12K ohms 1/8W
R69	ERD10TJ102	Carbon	1K ohms 1/8W
R70	ERD10TJ391	Carbon	390 ohms 1/8W
R71	ERD10TJ104	Carbon	100K ohms 1/8W
R72	ERD10TJ682	Carbon	6.8K ohms 1/8W
R73	ERD10TJ472	Carbon	4.7K ohms 1/8W
R74	ERD10TJ103	Carbon	10K ohms 1/8W
R75,76	ERD10TJ222	Carbon	2.2K ohms 1/8W
R77	ERD10TJ822	Carbon	8.2K ohms 1/8W
R78	ERD10TJ182	Carbon	1.8K ohms 1/8W
R79,80	ERD10TJ222	Carbon	2.2K ohms 1/8W

SYMBOL NO.	PART NO.	DESCRIPTION	
R82	ERD10TJ102	Carbon	1K ohms 1/8W
R84	ERD10TJ333	Carbon	33K ohms 1/8W
R85	ERD10TJ103	Carbon	10K ohms 1/8W
R86	ERD10TJ333	Carbon	33K ohms 1/8W
R87	ERD10TJ101	Carbon	100 ohms 1/8W
R88	ERD10TJ103	Carbon	10K ohms 1/8W
R89	ERD10TJ101	Carbon	100 ohms 1/8W
R90	ERD10TJ221	Carbon	220 ohms 1/8W
R91	ERD10TJ333	Carbon	33K ohms 1/8W
R92	ERD10TJ104	Carbon	100K ohms 1/8W
R93	ERD10TJ101	Carbon	100 ohms 1/8W
R94	ERD10TJ105	Carbon	1M ohms 1/8W
R95	ERD10TJ101	Carbon	100 ohms 1/8W
R96	ERD10TJ102	Carbon	1K ohms 1/8W
R97	ERD10TJ104	Carbon	100K ohms 1/8W
R99	ERD10TJ124	Carbon	120K ohms 1/8W
R100	ERD10TJ152	Carbon	1.5K ohms 1/8W
R101	ERD10TJ102	Carbon	1K ohms 1/8W
R102	ERD10TJ473	Carbon	47K ohms 1/8W
R103	ERD10TJ683	Carbon	68K ohms 1/8W
R104,105	ERD10TJ562	Carbon	5.6K ohms 1/8W
R106	ERD10TJ102	Carbon	1K ohms 1/8W
R107	ERD10TJ562	Carbon	5.6K ohms 1/8W
R108	ERD10TJ102	Carbon	1K ohms 1/8W
R109	ERD10TJ152	Carbon	1.5K ohms 1/8W
R110	ERD10TJ332	Carbon	3.3K ohms 1/8W
R111,112	ERD10TJ102	Carbon	1K ohms 1/8W
R114,115	ERD10TJ222	Carbon	2.2K ohms 1/8W
R116,117	ERD10TJ6R8	Carbon	6.8 ohms 1/8W
R118	ERD10TJ103	Carbon	10K ohms 1/8W
R119	ERD10TJ331	Carbon	330 ohms 1/8W
R120	ERD10TJ561	Carbon	560 ohms 1/8W
VR1	YFP0T3321P53	Variable Resistor	5K ohms
VR2	YFP0T3321P13	Variable Resistor	1K ohms
VR3,4	YFP0T3321P14	Variable Resistor	10K ohms
VR5	YFP0T3321P52	Variable Resistor	500 ohms
VR6	YFP0T3321P14	Variable Resistor	10K ohms
VR7	YFP0T3321P13	Variable Resistor	1K ohms
VR8	YFP0T3321P53	Variable Resistor	5K ohms
VR9,10	YFP0T3321P14	Variable Resistor	10K ohms
VR11	YFK12241KB2	Variable Resistor	1K ohms
VR12,13	YFK12242KB2	Variable Resistor	2K ohms
C1	ECSF1CE476	Electrolytic	47 µF 16V
C3,4	ECQP1151JZ	Plastic	150 pF 100V
C5	ECEA1ASS470	Electrolytic	47 µF 10V
C6	ECQP1331JZ	Plastic	330 pF 100V
C7-9	ECQM1H104MZ	Plastic	0.1 µF 50V
C10	ECSF1CE476	Electrolytic	47 µF 16V
C11	ECCF1H100JC	Ceramic	10 pF 50V
C12	ECQM1H103JZ	Plastic	0.01 µF 50V
C13	ECCF1H100JC	Ceramic	10 pF 50V
C14	ECQM1H103JZ	Plastic	0.01 µF 50V
C15	ECEA1ASS470	Electrolytic	47 µF 10V
C16	ECCF1H270J	Ceramic	27 pF 50V
C17	ECCF1H330J	Ceramic	33 pF 50V
C18	ECCF1H270J	Ceramic	27 pF 50V
C19	ECSF1CE476	Electrolytic	47 µF 16V

SYMBOL NO.	PART NO.	DESCRIPTION
C20-22	ECEA1ASS470	Electrolytic 47 µF 10V
C23	ECSF1CE476	Electrolytic 47 µF 16V
C24	ECEA0JS101	Electrolytic 100 µF 6.3V
C26,27	ECEA1ASS470	Electrolytic 47 µF 10V
C29	ECQP1151JZ	Plastic 150 pF 100V
C30	ECQM1H103JZ	Plastic 0.01 µF 50V
C31	ECQP1222JZ	Plastic 2200 pF 100V
C32	ECSF16E33	Electrolytic 33 µF 16V
C33	ECQM1H103JZ	Plastic 0.01 µF 50V
C34	ECSF1AE476	Electrolytic 47 µF 10V
C35	ECEA1HSS010	Electrolytic 1 µF 50V
C36	ECSF16E33	Electrolytic 33 µF 16V
C37	ECQP1101JZ	Plastic 100 pF 100V
C38	ECQP1221JZ	Plastic 220 pF 100V
C39	ECCF1H180JC	Ceramic 18 pF 50V
C40	ECCF1H330JC	Ceramic 33 pF 50V
C42	ECSF1AE476	Electrolytic 47 µF 10V
C43	ECQP1222JZ	Plastic 2200 pF 100V
C44	ECQM1H223JZ	Plastic 0.022 µF 50V
C45	ECQP1221JZ	Plastic 220 pF 100V
C48	ECCF1H330JC	Ceramic 33 pF 50V
C49	ECSF0JE476	Plastic 47 µF 6.3V
C50	ECQP1102JZ	Plastic 1000 pF 100V
C51	ECQP1221JZ	Plastic 220 pF 100V
C53	ECSF1AE476	Electrolytic 47 µF 10V
C54	ECCF1H220JC	Ceramic 22PF 50V
C55	ECQP1102JZ	Plastic 1000 pF 100V
C56	ECCF1H220JC	Ceramic 22PF 50V
C57	ECQM1H103JZ	Plastic 0.01 µF 50V
C58	ECCF1H470JC	Ceramic 47 pF 50V
C59	ECQP1101JZ	Plastic 100 pF 100V
C60	ECQV1H473JZ	Plastic 0.047 µF 50V
C62	ECSF1AE476	Electrolytic 47 µF 10V
C63	ECEA1ASS470	Electrolytic 47 µF 10V
C64,65	ECQP1101JZ	Plastic 100 pF 100V
C66	ECSF1AE476	Electrolytic 47 µF 10V
C67	ECSF1CE476	Electrolytic 47 µF 16V
C69	ECEA1HSS010	Electrolytic 1 µF 50V
C72	ECQP1101JZ	Plastic 100 pF 100V
C73	ECSF1CE476	Electrolytic 47 µF 16V
C74	ECCF1H220JC	Ceramic 22PF 50V
CT1-4	ECV1ZW25X53T	Trimmer Capacitor 25 pF
L1,2	YFL5470J	Coil 47 µH
L3	YWL5120J	Coil 12 µH
L4	YWL5270J	Coil 27 µH
L5	YWL5220J	Coil 22 µH
L6	YWL5100J	Coil 10 µH
L7-9	YFL5470J	Coil 47 µH
L10	YFL54R7J	Coil 4.7 µH
L11-14	YFL5470J	Coil 47 µH
SW1	YFSBU1024A	Rotary Switch
X1,2	YFKD2034KDB	Crystal Oscillator
X3	YFKD3246KAB	Crystal Oscillator
CF1-3	YFSLC871-197	Filter
J1,2	ERD25TC0	Jumper Resistor
J4	ERD25TC0	Jumper Resistor

SYMBOL NO.	PART NO.	DESCRIPTION
JK1	YWLJ145-1A	Jack
M44	YFV2SA0107A4	Mounting Angle for Intercom Jack
M45	YWA620AER01	Insulator Washer

PCB12 CHROMA KEY BOARD

SYMBOL NO.	PART NO.	DESCRIPTION
IC1	HD14081BP	IC
IC2	YWHD14175BP	IC
Q1-4	2SD639RS	Transistor
Q5,6	2SD636-RS	Transistor
Q7	2SK34-CD	Transistor
Q8	2SD636-RS	Transistor
Q9	2SC2377CD	Transistor
Q10	2SD636-RS	Transistor
Q11	2SC2377CD	Transistor
Q12	2SD636-RS	Transistor
Q13	2SK34-CD	Transistor

SYMBOL NO.	PART NO.	DESCRIPTION	
Q14-17	2SD636-RS	Transistor	
Q18	2SK34-CD	Transistor	
Q19	2SK19-Y	Transistor	
Q20,21	2SC2377CD	Transistor	
Q22-24	2SD636-RS	Transistor	
Q25	2SB641-RS	Transistor	
Q26	2SD636-RS	Transistor	
Q27	2SB641-RS	Transistor	
D1-5	MA165	Diode	
D6	YUDYZ040B	Diode	
R1	ERD10TJ472	Carbon	4.7K ohms 1/8W
R2	ERG1ANJ150	Metal	15 ohms 1W
R3	ERD10TJ102	Carbon	1K ohms 1/8W
R4-12	ERD10TJ103	Carbon	10K ohms 1/8W
R13	ERD10TJ472	Carbon	4.7K ohms 1/8W
R16	ERD10TJ472	Carbon	4.7K ohms 1/8W
R17	ERD10TJ102	Carbon	1K ohms 1/8W
R18	ERD10TJ222	Carbon	2.2K ohms 1/8W
R19	ERD10TJ332	Carbon	3.3K ohms 1/8W
R20	ERD10TJ101	Carbon	100 ohms 1/8W
R21	ERD10TJ104	Carbon	100K ohms 1/8W
R22	ERD10TJ102	Carbon	1K ohms 1/8W
R23	ERD10TJ271	Carbon	270 ohms 1/8W
R24	ERD10TJ332	Carbon	3.3K ohms 1/8W
R25	ERD10TJ272	Carbon	2.7K ohms 1/8W
R26	ERD10TJ271	Carbon	270 ohms 1/8W
R27	ERD10TJ221	Carbon	220 ohms 1/8W
R28	ERD10TJ271	Carbon	270 ohms 1/8W
R29	ERD10TJ272	Carbon	2.7K ohms 1/8W
R30	ERD10TJ332	Carbon	3.3K ohms 1/8W
R31	ERD10TJ152	Carbon	1.5K ohms 1/8W
R32	ERD10TJ222	Carbon	2.2K ohms 1/8W
R33	ERD10TJ104	Carbon	100K ohms 1/8W
R34-37	ERD10TJ102	Carbon	1K ohms 1/8W
R38	ERD10TJ392	Carbon	3.9K ohms 1/8W
R39,40	ERD10TJ223	Carbon	22K ohms 1/8W
R41	ERD10TJ392	Carbon	3.9K ohms 1/8W
R42,43	ERD10TJ223	Carbon	22K ohms 1/8W
R44	ERD10TJ392	Carbon	3.9K ohms 1/8W
R45,46	ERD10TJ223	Carbon	22K ohms 1/8W
R47	ERD10TJ104	Carbon	100K ohms 1/8W
R48	ERD10TJ102	Carbon	1K ohms 1/8W
R49	ERD10TJ222	Carbon	2.2K ohms 1/8W
R50	ERD10TJ182	Carbon	1.8K ohms 1/8W
R51	ERD10TJ201	Carbon	200 ohms 1/8W
R52	ERD10TJ152	Carbon	1.5K ohms 1/8W
R53	ERD10TJ102	Carbon	1K ohms 1/8W
R54	ERD10TJ101	Carbon	100 ohms 1/8W
R55	ERD10TJ222	Carbon	2.2K ohms 1/8W
R56,57	ERD10TJ102	Carbon	1K ohms 1/8W
R58,59	ERD10TJ271	Carbon	270 ohms 1/8W
R60	ERD10TJ330	Carbon	33 ohms 1/8W
R61,62	ERD10TJ271	Carbon	270 ohms 1/8W
R63	ERD10TJ330	Carbon	33 ohms 1/8W
R64	ERD10TJ102	Carbon	1K ohms 1/8W
R65	ERD10TJ471	Carbon	470 ohms 1/8W
R66	ERD10TJ152	Carbon	1.5K ohms 1/8W

SYMBOL NO.	PART NO.	DESCRIPTION	
R67	ERD10TJ221	Carbon	220 ohms 1/8W
R68	ERD10TJ152	Carbon	1.5K ohms 1/8W
VR3	YFK16116KB	Variable Resistor	6K ohms
C1	ECEA1ESS101	Electrolytic	100 μF 25V
C2	ECEA1ASS101	Electrolytic	100 μF 10V
C3	ECEA1EK4R7	Electrolytic	4.7 μF 25V
C4	ECEA1HK010	Electrolytic	1 μF 50V
C5	ECQV05104JZ	Plastic	0.1 μF 50V
C6	ECEA1CK100E	Electrolytic	10 μF 16V
C7	ECEA1HK010	Electrolytic	1 μF 50V
C8-10	ECEA1AK470	Electrolytic	47 μF 10V
C11	ECEA1ASS101	Electrolytic	100 μF 10V
C12	ECEA1CK100E	Electrolytic	10 μF 16V
C13	ECQV05223JZ	Plastic	0.022 μF 50V
C14	ECEA1CK100E	Electrolytic	10 μF 16V
C15	ECCF1H151JR	Ceramic	150 pF 50V
C16	ECCF1H181JC	Ceramic	180 pF 50V
DL1	YFDL4725	Delay Line	250ns
SW1	YF4F2C0472VC	4 Channel Push Switch	
CN1-JM	YFB6B-XH-A	6 pin Jack Male	
CN2-JM	YFB5B-XH-A	5 pin Jack Male	
CN3-JM	YFB3B-XH-A	3 pin Jack Male	
E10	* WMT4X1R2X5	Insulator	
M42	* YFV7SA0109A5	Mounting Angle A	

PCB13 DELAY BOARD

VR1	YFK1214500B2	Variable Resistor	500 ohms

PCB14 LEVEL BOARD

VR2	YFK12142KB2	Variable Resistor	2K ohms

PCB15 LEVER BOARD

IC1	HD14027BP	IC	
IC2	YWHD14001BP	IC	
IC3	HD14027BP	IC	
Q1-3	2SD639RS	Transistor	
Q4-7	2SB641-RS	Transistor	
R1	ERD25FJ563	Carbon	56K ohms 1/4W
R2	ERD25FJ562	Carbon	5.6K ohms 1/4W
R3	ERD25FJ272	Carbon	2.7K ohms 1/4W
R4	ERD25FJ223	Carbon	22K ohms 1/4W
R5	ERD25FJ103	Carbon	10K ohms 1/8W
R6	ERD25FJ563	Carbon	56K ohms 1/4W
R7	ERD25FJ562	Carbon	5.6K ohms 1/4W
R8	ERD25FJ103	Carbon	10K ohms 1/4W
R9	ERD25FJ563	Carbon	56K ohms 1/4W
R10	ERD25FJ562	Carbon	5.6K ohms 1/4W
R11	ERD25FJ103	Carbon	10K ohms 1/4W

SYMBOL NO.	PART NO.	DESCRIPTION	
R13	ERD25FJ472	Carbon	4.7K ohms 1/4W
R14	ERD25FJ183	Carbon	18K ohms 1/4W
R16	ERD25FJ332	Carbon	3.3K ohms 1/4W
R17	ERD25FJ153	Carbon	15K ohms 1/4W
R18,19	ERD25FJ222	Carbon	2.2K ohms 1/4W
R20-22	ERG1ANJ150	Metal	15 ohms 1W
C1,2	ECQV05393JZ	Plastic	0.039 μF 50V
C3	ECEA1CSS100	Electrolytic	10 μF 16V
C4-7	ECQV05393JZ	Plastic	0.039 μF 50V
C8,9	ECEA1CSS100	Electrolytic	10 μF 16V
C10	ECEA1ESS101	Electrolytic	100 μF 25V
C11	ECEA1CSS101	Electrolytic	100 μF 16V
SW1	YF2F3C0472VC	2 Channel Push Switch	
SW2	YF1F5C0472VC	1 Channel Push Switch	
CN4-JM	YFB4B-XH-A	4 pin Jack Male	
CN5-JM	YFB6B-XH-A	6 pin Jack Male	
CN6-JM	YFB2B-XH-A	2 pin Jack Male	
CN7-JM	YFB8B-XH-A	8 pin Jack Male	
CN8-JM	YFB7B-XH-A	7 pin Jack Male	
M38	YWJ5500FR02B	Mounting Guide	

PCB16 POSITION –1 BOARD

SYMBOL NO.	PART NO.	DESCRIPTION	
IC1	YFHD14027BP	IC	
Q1,2	2SB644-RS	Transistor	
Q3	2SD639RS	Transistor	
Q4,5	2SB644-RS	Transistor	
Q6	2SD636-RS	Transistor	
R1	ERD25FJ563	Carbon	56K ohms 1/4W
R2	ERD25FJ562	Carbon	5.6K ohms 1/4W
R3	ERD25FJ223	Carbon	22K ohms 1/4W
R4	ERD25FJ272	Carbon	2.7K ohms 1/4W
R5-7	ERD25FJ103	Carbon	10K ohms 1/4W
R8	ERD25FJ223	Carbon	22K ohms 1/4W
R9	ERD25FJ103	Carbon	10K ohms 1/4W
R10	ERD25FJ102	Carbon	10K ohms 1/4W
R11	ERD25FJ822	Carbon	8.2K ohms 1/4W
R12	ERD25FJ202	Carbon	2K ohms 1/4W
VR1	YFRJ6S502B	Variable Resistor	5K ohms
VR2	YFRJ6S202B	Variable Resistor	2K ohms
C1,2	ECQV05393JZ	Plastic	0.039 μF 50V
C3	ECEA1CSS100	Electrolytic	10 μF 16V
C4	ECEA1ASS101	Electrolytic	100 μF 10V
SW1	YF1F1A2272VB	Push Switch	
CN11-JM	YFB2B-XH-A	2 pin Jack Male	
CN12-JM	YFB2B-XH-A	2 pin Jack Male	
M38	YWJ5500FR02B	Mounting Guide	

PCB17 POSITION –2 BOARD

SYMBOL NO.	PART NO.	DESCRIPTION	
Q1	2SD636-RS	Transistor	1K ohms 1/4W
R1	ERD25FJ102	Carbon	1K ohms 1/8W
R2	ERD25FJ822	Carbon	8.2K ohms 1/4W
R3	ERD25FJ202	Carbon	2K ohms 1/4W
R4	ERG1ANJ150	Metal	15 ohms 1/4W
VR3	YFRJ6S502B	Variable Resistor	5K ohms
VR4	YFRJ6S202B	Variable Resistor	2K ohms
CN14-JM	YFB2B-XH-A	2 pin Jack Male	

PCB18 MOTHER BOARD

SYMBOL NO.	PART NO.	DESCRIPTION	
IC	HA17723G	IC	
Q1	2SD636-RS	Transistor	
Q2	2SC1226-QR	Transistor	
Q3-5	2SD636-RS	Transistor	
Q6	2SA1254-BC	Transistor	
Q7	2SC2377CD	Transistor	
D1,2	MA150	Diode	
D201,202	MA162	Diode	
R1	ERG2ANJR33	Metal	0.33 ohms 2W
R2	ERD25FJ822	Carbon	8.2K ohms 1/4W
R3	ERD25FJ821	Carbon	820 ohms 1/4W
R4	ERG1ANJ221	Metal	220 ohms 1W
R5	ERD25FJ333	Carbon	33K ohms 1/4W
R6	ERD25FJ393	Carbon	39K ohms 1/4W
R7	ERD25FJ332	Carbon	3.3K ohms 1/4W
R8,9	ERD25FJ102	Carbon	1K ohms 1/4W
R10	ERD25FJ332	Carbon	3.3K ohms 1/4W
R11	ERD25FJ333	Carbon	33K ohms 1/4W
R12,13	ERD25FJ472	Carbon	4.7K ohms 1/4W
R14	ERD25FJ103	Carbon	10K ohms 1/4W
R15	ERD25FJ391	Carbon	390 ohms 1/4W
R16	ERD25FJ331	Carbon	330 ohms 1/4W
R17	ERD25FJ392	Carbon	3.9K ohms 1/4W
R19,20	ERD25FJ103	Carbon	10K ohms 1/4W
R21	ERD25FJ392	Carbon	3.9K ohms 1/4W
R201	ERD25FJ392	Carbon	3.9K ohms 1/4W
R202	ERD25FJ103	Carbon	10K ohms 1/4W
R203	ERD25FJ680	Carbon	68 ohms 1/4W
VR1	YFP0T3321P14	Variable Resistor	10K ohms
C1	ECET35R103SW	Electrolytic	10000 μF 35V
C2	ECQP1101JZ	Plastic	100 pF 100V
C3,4	ECEA1CSS102E	Electrolytic	1000 μF 16V
C5,6	ECEA1CN100S	Electrolytic	10 μF 16V
C7	ECEA1CS102E	Electrolytic	1000 μF 16V
C8	ECEA1CN100S	Electrolytic	10 μF 16V
C9	ECKF1H472KB	Ceramic	4700 pF 50V
C10	ECEA1CN100S	Electrolytic	10 μF 16V
C11	ECEA1CS100	Electrolytic	10 μF 16V
T1	YWDP42-6015	Choke Coil for Intercom	
CN1-JM	YF527103A	3 pin Jack Male	
CN2-JM	YF527203A	3 pin Jack Male	
CN3-JM	YF527103A	3 pin Jack Male	
CN4-JM	YF527204A	4 pin Jack Male	
CN5-JM	YFB3B-XH-A	3 pin Jack Male	
CN6-JM	YF527110A	10 pin Jack Male	
CN7-JM	YF527110A	10 pin Jack Male	
CN8-JM	YF527106A	6 pin Jack Male	
CN9-JM	YFB3B-XH-A	3 pin Jack Male	
CN10-JM	YFB3B-XH-A	3 pin Jack Male	
CN11-JM	YF527106A	6 pin Jack Male	
CN12-JM	YF527106A	6 pin Jack Male	
CN13-JM	YF527110A	10 pin Jack Male	
CN14-JM	YF527106A	6 pin Jack Male	

SYM-BOL NO.	PART NO.	DESCRIPTION	
CN15-J 27-J	YWR412238U	Multi-pin Connector	
F1	XBA2C40ET0A	Current Fuse	250V 4A
E2	YWSN5053	Fuse Holder	
E10	* WMT4X1R2X5	Insulator	
E20	* WMT6X1R2X7	Insulator	
M46	YFV2SA0114A4	Mounting Angle D for Mother Board	
M47	* YWJ5500AM03	Mounting Angle E for Mother Board	
M48	* YFV7MA0075A4	Fuse Label	

PCB19 CONNECTOR BOARD

SYM-BOL NO.	PART NO.	DESCRIPTION	
Q1-18	2SD636-RS	Transistor	
Q19-27	2SD639RS	Transistor	
Q28	2SC1216F	Transistor	
Q29	2SB644-RS	Transistor	
Q30	2SC1216F	Transistor	
Q31	2SB644-RS	Transistor	
Q32	2SC1216F	Transistor	
Q33	2SB644-RS	Transistor	
Q34	2SC1216F	Transistor	
Q35	2SB644-RS	Transistor	
Q36	2SC1216-F	Transistor	
Q37	2SB644-RS	Transistor	
Q38	2SC1216F	Transistor	
Q39	2SB644-RS	Transistor	
R1-11	ERD10TJ750	Carbon	75 ohms 1/8W
R12	ERD10TJ560	Carbon	56 ohms 1/8W
R13	ERD10TJ470	Carbon	47 ohms 1/8W
R14	ERD10TJ270	Carbon	27 ohms 1/8W
R15	ERD10TJ680	Carbon	68 ohms 1/8W
R16	ERD10TJ120	Carbon	12 ohms 1/8W
R17	ERD10TJ620	Carbon	62 ohms 1/8W
R18	ERD10TJ333	Carbon	33K ohms 1/8W
R19	ERD10TJ153	Carbon	15K ohms 1/8W
R20	ERD10TJ221	Carbon	220 ohms 1/8W
R21	ERD10TJ222	Carbon	2.2K ohms 1/8W
R22	ERD10TJ333	Carbon	33K ohms 1/8W
R23	ERD10TJ153	Carbon	15K ohms 1/8W
R24	ERD10TJ221	Carbon	220 ohms 1/8W
R25	ERD10TJ222	Carbon	2.2K ohms 1/8W
R26	ERD10TJ333	Carbon	33K ohms 1/8W
R27	ERD10TJ153	Carbon	15K ohms 1/8W
R28	ERD10TJ221	Carbon	220 ohms 1/8W
R29	ERD10TJ222	Carbon	2.2K ohms 1/8W
R30	ERD10TJ333	Carbon	33K ohms 1/8W
R31	ERD10TJ153	Carbon	15K ohms 1/8W
R32	ERD10TJ221	Carbon	220 ohms 1/8W
R33	ERD10TJ222	Carbon	2.2K ohms 1/8W
R34	ERD10TJ333	Carbon	33K ohms 1/8W
R35	ERD10TJ153	Carbon	15K ohms 1/8W
R36	ERD10TJ221	Carbon	220 ohms 1/8W
R37	ERD10TJ222	Carbon	2.2K ohms 1/8W
R38	ERD10TJ333	Carbon	33K ohms 1/8W
R39	ERD10TJ153	Carbon	15K ohms 1/8W
R40	ERD10TJ221	Carbon	220 ohms 1/8W
R41	ERD10TJ222	Carbon	2.2K ohms 1/8W
R42	ERD10TJ333	Carbon	33K ohms 1/8W
R43	ERD10TJ153	Carbon	15K ohms 1/8W
R44	ERD10TJ221	Carbon	220 ohms 1/8W
R45	ERD10TJ222	Carbon	2.2K ohms 1/8W
R46	ERD10TJ333	Carbon	33K ohms 1/8W
R47	ERD10TJ153	Carbon	15K ohms 1/8W
R48	ERD10TJ221	Carbon	220 ohms 1/8W
R49	ERD10TJ222	Carbon	2.2K ohms 1/8W
R50,51	ERD10TJ183	Carbon	18K ohms 1/8W
R52	ERD10TJ221	Carbon	220 ohms 1/8W
R53	ERD10TJ152	Carbon	1.5K ohms 1/8W
R54,55	ERD10TJ183	Carbon	18K ohms 1/8W
R56	ERD10TJ221	Carbon	220 ohms 1/8W
R57	ERD10TJ152	Carbon	1.5K ohms 1/8W
R58,59	ERD10TJ183	Carbon	18K ohms 1/8W
R60	ERD10TJ221	Carbon	220 ohms 1/8W
R61	ERD10TJ152	Carbon	1.5K ohms 1/8W
R62,63	ERD10TJ183	Carbon	18K ohms 1/8W
R64	ERD10TJ221	Carbon	220 ohms 1/8W
R65	ERD10TJ152	Carbon	1.5K ohms 1/8W
R66,67	ERD10TJ183	Carbon	18K ohms 1/8W
R68	ERD10TJ221	Carbon	220 ohms 1/8W
R69	ERD10TJ152	Carbon	1.5K ohms 1/8W
R70,71	ERD10TJ183	Carbon	18K ohms 1/8W
R72	ERD10TJ221	Carbon	220 ohms 1/8W
R73	ERD10TJ152	Carbon	1.5K ohms 1/8W
R74	ERD10TJ181	Carbon	180 ohms 1/8W
R75	ERD10TJ560	Carbon	56 ohms 1/8W
R76	ERD10TJ223	Carbon	22K ohms 1/8W
R77	ERD10TJ332	Carbon	3.3K ohms 1/8W
R78	ERD10TJ471	Carbon	470 ohms 1/8W
R79	ERD10TJ821	Carbon	820 ohms 1/8W
R80	ERD10TJ272	Carbon	2.7K ohms 1/8W
R81	ERD10TJ561	Carbon	560 ohms 1/8W
R82	ERD10TJ102	Carbon	1K ohms 1/8W
R83	ERD10TJ471	Carbon	470 ohms 1/8W
R84	ERD10TJ561	Carbon	560 ohms 1/8W
R85	ERD10TJ103	Carbon	10K ohms 1/8W
R86	ERD10TJ273	Carbon	27K ohms 1/8W
R89	ERD10TJ680	Carbon	68 ohms 1/8W
R90	ERD10TJ223	Carbon	22K ohms 1/8W
R91	ERD10TJ561	Carbon	560 ohms 1/8W
R92	ERD10TJ153	Carbon	15K ohms 1/8W
R93	ERD10TJ223	Carbon	22K ohms 1/8W
R94	ERD10TJ102	Carbon	1K ohms 1/8W
R95	ERD10TJ103	Carbon	10K ohms 1/8W
R96	ERD10TJ104	Carbon	100K ohms 1/8W
R97	ERD10TJ103	Carbon	10K ohms 1/8W
R98	ERD10TJ104	Carbon	100K ohms 1/8W
R99	ERD10TJ103	Carbon	10K ohms 1/8W
R100	ERD10TJ104	Carbon	100K ohms 1/8W
R101	ERD10TJ103	Carbon	10K ohms 1/8W
R102	ERD10TJ104	Carbon	100K ohms 1/8W
R103	ERD10TJ103	Carbon	10K ohms 1/8W
R104	ERD10TJ104	Carbon	100K ohms 1/8W

SYMBOL NO.	PART NO.	DESCRIPTION
R105	ERD10TJ103	Carbon 10K ohms 1/8W
R106	ERD10TJ104	Carbon 100K ohms 1/8W
R107	ERD10TJ103	Carbon 10K ohms 1/8W
R108	ERD10TJ104	Carbon 100K ohms 1/8W
R109	ERD10TJ103	Carbon 10K ohms 1/8W
R110	ERD10TJ104	Carbon 100K ohms 1/8W
R111	ERD10TJ103	Carbon 10K ohms 1/8W
R112	ERD10TJ751	Carbon 750 ohms 1/8W
R113	ERD10TJ101	Carbon 100 ohms 1/8W
R114	ERD10TJ471	Carbon 470 ohms 1/8W
R115	ERD10TJ223	Carbon 22K ohms 1/8W
R116	ERD10TJ103	Carbon 10K ohms 1/8W
R117	ERD10TJ751	Carbon 750 ohms 1/8W
R118	ERD10TJ101	Carbon 100 ohms 1/8W
R119	ERD10TJ471	Carbon 470 ohms 1/8W
R120	ERD10TJ223	Carbon 22K ohms 1/8W
R121	ERD10TJ103	Carbon 10K ohms 1/8W
R122	ERD10TJ751	Carbon 750 ohms 1/8W
R123	ERD10TJ101	Carbon 100 ohms 1/8W
R124	ERD10TJ271	Carbon 270 ohms 1/8W
R125	ERD10TJ223	Carbon 22K ohms 1/8W
R126	ERD10TJ103	Carbon 10K ohms 1/8W
R127	ERD10TJ751	Carbon 750 ohms 1/8W
R128	ERD10TJ101	Carbon 100 ohms 1/8W
R129	ERD10TJ271	Carbon 270 ohms 1/8W
R130	ERD10TJ223	Carbon 22K ohms 1/8W
R131	ERD10TJ103	Carbon 10K ohms 1/8W
R132	ERD10TJ751	Carbon 750 ohms 1/8W
R133	ERD10TJ101	Carbon 100 ohms 1/8W
R134	ERD25FJ471	Carbon 470 ohms 1/8W
R135	ERD10TJ680	Carbon 68 ohms 1/8W
R136	ERD10TJ223	Carbon 22K ohms 1/8W
R137	ERD10TJ103	Carbon 10K ohms 1/8W
R138	ERD10TJ751	Carbon 750 ohms 1/8W
R139	ERD10TJ101	Carbon 100 ohms 1/8W
R140	ERD10TJ471	Carbon 470 ohms 1/8W
R141	ERD10TJ223	Carbon 22K ohms 1/8W
R201	ERD10TJ822	Carbon 8.2K ohms 1/8W
R202	ERD10TJ112	Carbon 1.1K ohms 1/8W
R207	ERD10TJ112	Carbon 1.1K ohms 1/8W
C1-6	ECEA0JSS471	Electrolytic 470μF 6.3V
C7	ECEA1ASS101	Electrolytic 100μF 10V
C8-22	ECEA1AK470	Electrolytic 47μF 10V
C23	ECEA0JK101	Electrolytic 100μF 6.3V
C24	ECEA1ASS101	Electrolytic 100μF 10V
C25	ECEA1AK470	Electrolytic 47μF 10V
C26	ECEA0JSS102	Electrolytic 1000μF 6.3V
C28	ECEA0JSS102	Electrolytic 1000μF 6.3V
C30	ECEA0JSS102	Electrolytic 1000μF 6.3V
C32	ECEA0JSS102	Electrolytic 1000μF 6.3V
C34	ECEA1ASS102	Electrolytic 1000μF 10V
C36	ECEA0JSS102	Electrolytic 1000μF 6.3V
E9	YVL437TM027	Terminal
CN6-JF	YW5145-10CH	10 pin Jack Female
CN7-JF	YW5145-10CH	10 pin Jack Female
CN8-JF	YW5145-6CH	6 pin Jack Female
CN11-JF	YW5145-6CH	6 pin Jack Female
CN12-JF	YW5145-6CH	6 pin Jack Female
CN13-JF	YW5145-10CH	10 pin Jack Female
CN14-JF	YW5145-6CH	6 pin Jack Female
M49	YWJ5500AM04	Mounting Angle

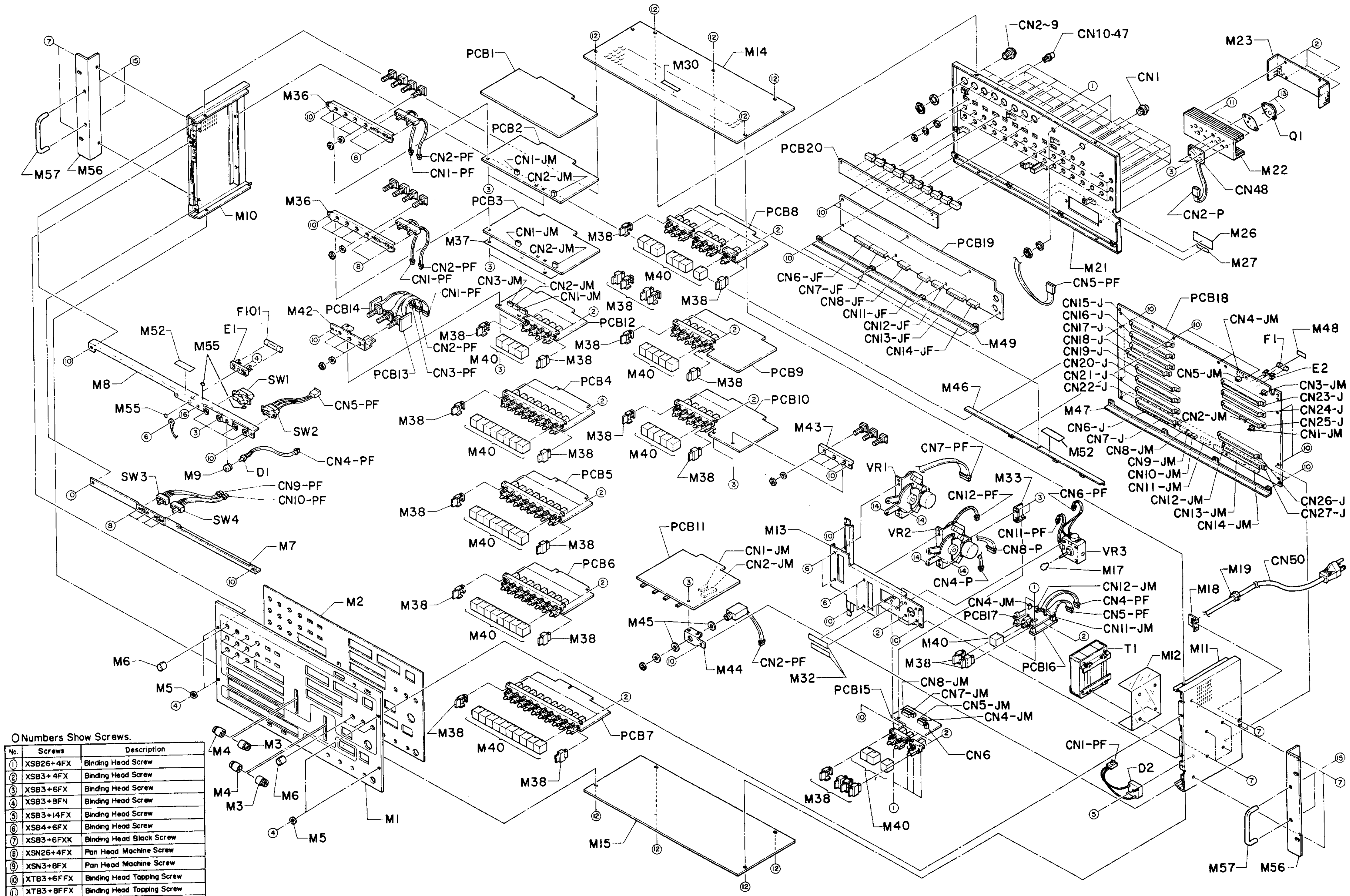
PCB20 TERMINATION BOARD

SYMBOL NO.	PART NO.	DESCRIPTION
R1-10	ERD25FJ750	Carbon 75 ohms 1/4W
SW1-10	YWSSC-322A	Slide Switch

ACCESSORY PARTS/PACKAGING PARTS

SYMBOL NO.	PART NO.	DESCRIPTION
PCB25	YWJ5500ZK13	Extension Board Assy
CN1	YQAAA-33	4 pin Connector (x8)
CN2	YWRM12BPG-4S	4 pin DC Connector
PL1	YW6200120500	Lamp (x2)
M56	YWJ5500AM10	Rack Mounting Angle
M57	YWB350-HM01	Rack Mounting Handle
M58	YWJ5500UR02	Expression Card B for Switch
M60	* YFV8QA0443AN	Operating Instruction for WJ-5600/C
	* YFV8QA0569AN	Operating Instruction for WJ-5600/B
M61	19998700331	Warranty Card for WJ-5600/B
M64	XZB55X71C1	Polyethylene Bag for SEG
M65	YWT20X35C03	Polyethylene Bag for Power Cord
M66	YWT15X20C03	Polyethylene Bag for Extension Board
M67	YWT050803	Polyethylene Bag for Lamp
M68	XZB26X40C05	Polyethylene Bag for Printed Matters
M70	YFV9CA0340AN	Packaging
M71	YFV8FA0004A3	Packing Label

EXPLODED VIEW OF SPECIAL EFFECTS GENERATOR



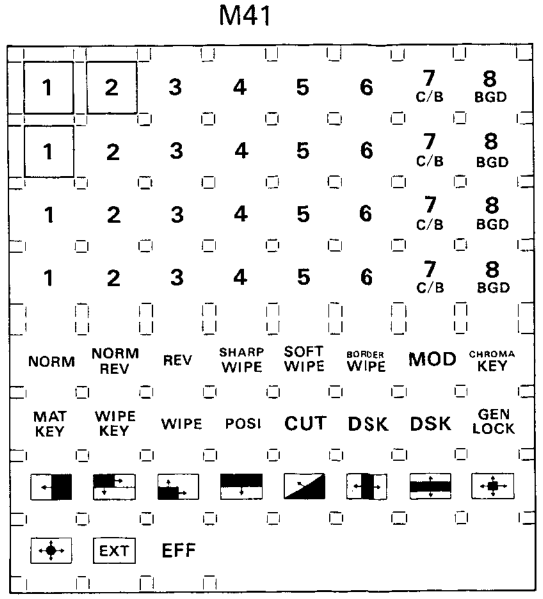
PCB1
M14
M30
M36
M57
M56
M10
PCB2
CN1-JM
CN2-JM
CN2-PF
CN1-PF
PCB3
M37
CN3-JM
PCB8
PCB20
CN2~9
CN10-47
CN1
M23
Q1
M22
CN48
CN2-P
M26
M27
M21
CN5-PF
PCB19
CN6-JF
CN7-JF
CN8-JF
CN11-JF
CN12-JF
CN13-JF
CN14-JF
M49
PCB18
CN4-JM
M48
F1
E2
CN15-J
CN16-J
CN17-J
CN18-J
CN19-J
CN20-J
CN21-J
CN22-J
CN5-JM
CN3-JM
CN23-J
CN24-J
CN25-J
M46
M47
M52
CN6-J
CN7-J
CN8-JM
CN9-JM
CN10-JM
CN11-JM
CN12-JM
CN13-JM
CN14-JM
CN26-J
CN27-J
F101
M42
PCB14
E1
M52
M55
M8
SW1
SW2
PCB12
PCB13
CN3-PF
M38
M40
PCB4
PCB9
PCB10
CN4-PF
M9
D1
SW3
SW4
CN9-PF
CN10-PF
M7
PCB5
PCB6
PCB7
PCB11
M43
VR1
VR2
VR3
CN7-PF
CN12-PF
M33
CN6-PF
CN11-PF
CN8-P
M17
CN4-P
M13
M45
M44
M32
CN12-JM
CN4-PF
CN5-PF
CN11-JM
PCB17
PCB16
T1
M12
M11
M18
M19
CN50
PCB15
CN8-JM
CN7-JM
CN5-JM
CN4-JM
CN6
CN1-PF
D2
M2
M6
M5
M4
M3
M1
M15

○Numbers Show Screws.

No.	Screws	Description
①	XSB26+4FX	Binding Head Screw
②	XSB3+4FX	Binding Head Screw
③	XSB3+6FX	Binding Head Screw
④	XSB3+8FN	Binding Head Screw
⑤	XSB3+14FX	Binding Head Screw
⑥	XSB4+6FX	Binding Head Screw
⑦	XSB3+6FXK	Binding Head Black Screw
⑧	XSN26+4FX	Pan Head Machine Screw
⑨	XSN3+8FX	Pan Head Machine Screw
⑩	XTB3+6FFX	Binding Head Tapping Screw
⑪	XTB3+8FFX	Binding Head Tapping Screw
⑫	XTB3+6FFXK	Binding Head Tapping Black Screw
⑬	XSB3+12BN	Binding Head Screw
⑭	XSS3+6FXN	Flush Head Machine Screw
⑮	XSS4+6FX	Flush Head Machine Screw
⑯	XWC4BFN	External Toothed Lock Washer

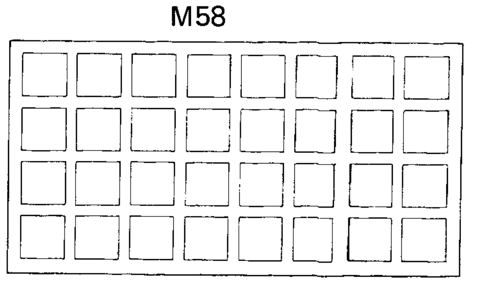
M1	YFV5WA0134A2
M2	YFV2CA0043A2
M3	YWMSF1004-5
M4	YWMSF1003-5
M5	YXL3X6BER01
M6	YWUM50-HM01A
M7	YFV2SA0105A3
M8	YFV2SA0104A3
M9	YFJ800PWB01
M10	YFV5EA0166A2
M11	YFV5EA0165A2
M12	YFV2PA0051A4
M13	YFV2SA0113A2
M14	YFV5EA0163A3
M15	YFV5EA0164A3
M17	YWJ5500HR01
M18	YFV2SA0108A4 YFV2SB0108A4
M19	YFSR6W-1
M21	YFV2KB0071A2
M22	YFV7DA0007A4
M23	YFV5EA0084A4
M26	YFV7QA0441B4
M27	YVZC700R850
M30	YFV7MA0053A4
M32	YFV7SA0106A4
M33	YFV2SA0112A4
M36	YFV2SA0110A3
M37	YFV2PA0050A4
M38	YWJ5500FR02B
M40	YWFL-BUTTON
M41	YFV7SA0105A3
M42	YF7SA0109A5
M43	YF2SA0111A4
M44	YF2SA0107A4
M45	YWA620AER01
M46	TF2SA0114A4
M47	YWJ5500AM03
M48	YFV7MA0075A4
M52	YWS-F00RB05A
M55	YW-BCG-UR01B

M41

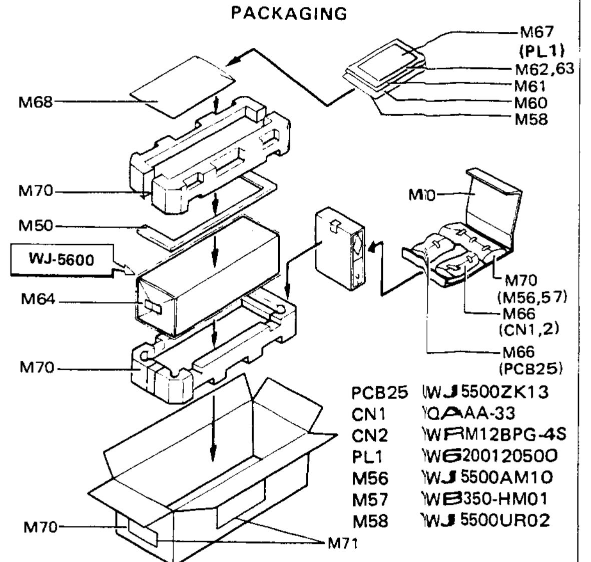


1
2
3
4
5
6
7 C/B
8 BGD
1
2
3
4
5
6
7 C/B
8 BGD
1
2
3
4
5
6
7 C/B
8 BGD
1
2
3
4
5
6
7 C/B
8 BGD
NORM
NORM REV
REV
SHARP WIPE
SOFT WIPE
BORDER WIPE
MOD
CHROMA KEY
MAT KEY
WIPE KEY
WIPE
POSI
CUT
DSK
DSK
GEN LOCK
EXT
EFF

M58



PACKAGING



M67 (PL1)
M62,63
M61
M60
M58
M68
M70
M10
M50
WJ-5600
M64
M70 (M56,57)
M66 (CN1,2)
M66 (PCB25)
M70
M70
M71

PCB25	YWJ5500ZK13
CN1	YQAAA-33
CN2	YWRM12BPG-4S
PL1	YW[illegible]200120500
M56	YWJ5500AM10
M57	YWB350-HM01
M58	YWJ5500UR02

M66	YWT15X20C03	M60	YFV8[illegible]QA0433AN YFV8[illegible]QA0567AN
M67	YWT050803		
M68	XZB26X40C05	M61	19[illegible]700331
M70	YFV9CA0340AN	M64	X[illegible]X71C1
M71	YFV8FA0004A3	M65	YWT2[illegible]X35C03

PCB1	OUTPUT BOARD
PCB2	DSK/BACK GROUND BOARD
PCB3	EFFECT/MIX BOARD
PCB4	CH.A CROSSPOINT BOARD
PCB5	CH.B CROSSPOINT BOARD
PCB6	CH.C CROSSPOINT BOARD
PCB7	CH.PV-PG CROSSPOINT BOARD
PCB8	WIPE WAVE PROCESS BOARD
PCB9	WAVEFORM GENERATOR BOARD
PCB10	MODULATION BOARD
PCB11	SYNC/COLOR BAR BOARD
PCB12	CHROMA KEY BOARD
PCB13	DELAY VR BOARD

PCB14	LEVEL VR BOARD
PCB15	LEVER CONNECTION BOARD
PCB16	POSITION SW BOTTOM BOARD
PCB17	POSITIPN SW UPPER BOARD
PCB18	MOTHER BOARD
PCB19	CONNECTOR BOARD
PCB20	IMPEADANCA SELECT SW BOARD
Q1	2SC647-PQ
D1	LN21RPH
D2	S15VB20
VR1,2	YWMSF1000-A4
VR3	EVXP2A001B15
T1	YFPHE86V002

SW1	EST1554
SW2	ESD391T
SW3,4	YWSSB02206
F101	XBA2C05ET0A
E1	YWXN1153-07
CN1	YWRM12BRD-4P
CN2-9	YWAA-34
CN10-47	YWBNC-R
CN48	YWS2-104W1S0
CN50	YFKPGTSA25 YFHBS308A YFCE009908FA YFVM009908A

CN1-JM	YF527103A
CN2-JM	YF527203A
CN3-JM	YF527103A
CN4-JM	YF527204A
CN5-JM	YFB3B-XH-A
CN6-JM	YF527110A
CN7-JM	YF527110A
CN8-JM	YF527106A
CN9-JM	YFB3B-XH-A
CN10-JM	YFB3B-XH-A
CN11-JM	YF527106A
CN12-JM	YF527106A
CN13-JM	YF527110A
CN14-JM	YF527106A
CN15-JM 27-JM	YWR412238U

ORDER NO. VKD87031053T8

VM047

Technical Information

Subject : APPEARANCE of IC / Part No. MP7260A

Applicable model No.: WJ-5600, WV-555series, WV-888, WV-P3, WV-N3

Symptom : The appearance between MP7260 and MP7260A is different.

Cause : This IC is sync generator LSI for cameras and special effects generators.

As of the first generation of this IC, MP7260 was developed and total 16 pins which are not used had already cut at IC factory.

Later on, most of ICs, chip transistors, etc.,on the P.C.B Assy are assembled by PANASERT machine as well as this MP7260.

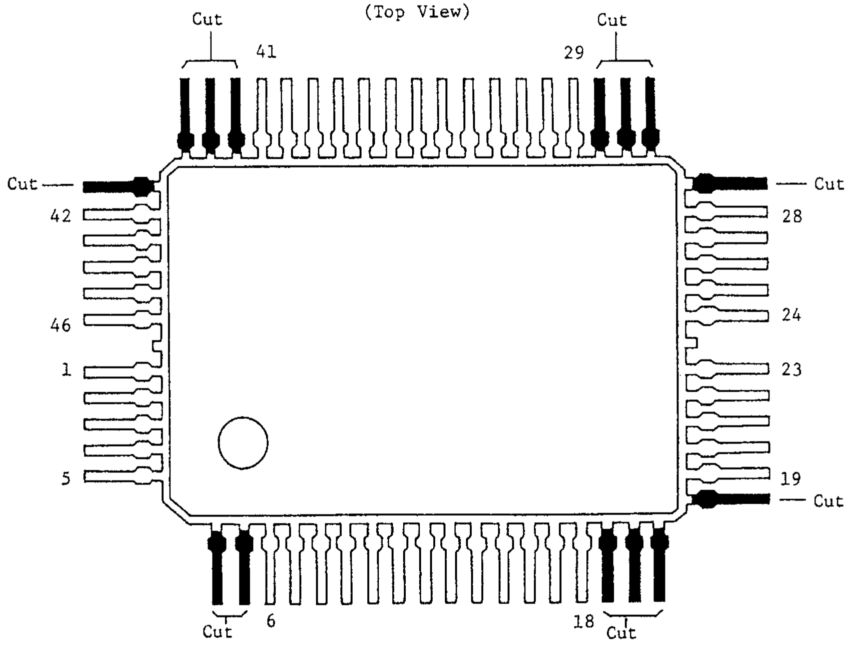
Since the all pins of IC should be positioned onto the copper patterns of P.C.B less than 1 millimeter tolerance, all pins located in the corner of IC must be there to measure the location of them by camera and computer.

As a result, the second generation of this IC MP7260A has been developed. At the same time and after, (MAY/86 and later) all copper pattern of PCB for new models have 60 pins and only MP7260A is supplied for both masproduction and replacement parts.

Remedy :

1. The function of both MP7260 and MP7260A is exactly same.
2. When the pins of original IC are cut , would you please cut the 14 pins indicated on the attached figure at your side and if not, please use it as it is.

Appearance of MP7260 / MP7260A
(Top View)



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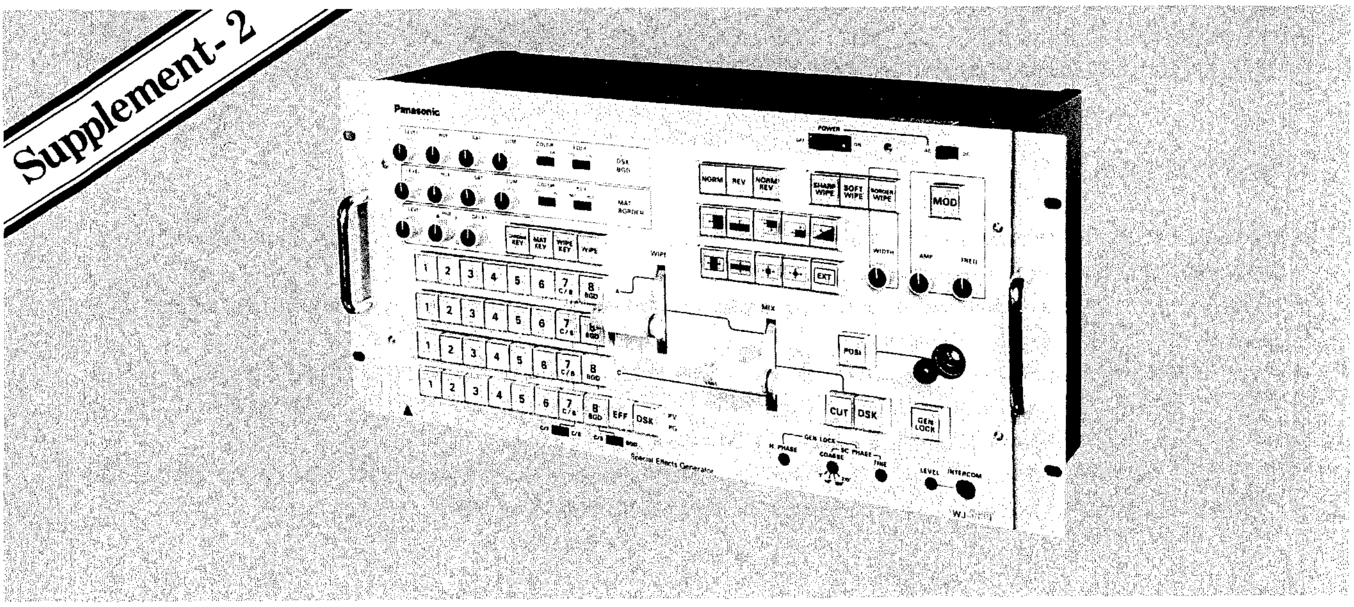
Service Manual

Special Effects Generator
WJ-5600



- Please file this supplement-2 with original service manual (Order No. VKD84040819C8)

CONTENTS

1. Vol. 2 **Adjustment Procedure** 3
2. Vol. 3 **Schematic Diagrams, Conductor Views** 4
    - Output Board .... 4 ~ 7
    - DSK, BGD Board 8, 9
    - Effect, Mix Board 10, 11
    - Chroma Key Board 12
    - Wipe Process Board 13
    - Waveform Gen. Board 14
    - Modulation Board 15
    - Lever/Position-1/Position-2 Board 16, 17
    - Sync, C/Bar Board 18, 19
    - Mother Board 20, 21
3. Vol. 4 **Replacement Parts List** .... 22 ~ 24

Panasonic

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P.O. Box 288, Central Osaka Japan

o Output Board

- o The white clip circuit has been changed to improve the white clip circuit from serial No. 42A00001 and higher. At same time the white clip level adjustment has been changed from 0.9V p-p to 0.8V p-p.
- o A jumper wire and a shield jumper wire have been added to prevent crosstalk for program output signal from serial No. 54A0001 and higher.
- o The resistors R26, R30, R145 and R149 have been changed to prevent the drift of pedestal level program output and preview output signals, when the warmed up.
- o The resistors R2, R15, R52, R60, R61, R124, R134, R169, R176, R200 and capacitors C35, C40 have been changed to improve signal output circuit from serial No. 55A00001 and higher.

o DSK, BGD Board

- o Capacitors C100, C101 have been added and C30 has been deleted to improve colour signal stability for DSK, BGD from serial No. 4ZA00001 and higher.
- o Capacitor C80 has been changed to prevent the distortion of sync signal for program output and preview output from serial No. 4YA00001 and higher.
- o Resistor R49 has been changed to improve the DSK signal noise from serial No. 51A00001 and higher.
- o Variable resistor VR7 has been deleted, resistor R43 and capacitor C29 have been changed to improve the DSK, BGD colour signal generator circuit from serial No. 51A00001 and higher.
- o Transistor Q72 and resistors R166, R167 have been deleted to prevent the black line noise on the picture, while DSK EDGE ON/OFF switch is ON position from serial No. 48A00001 and higher.

o Effect, Mix Board

- o Capacitors C100 and C101 have been added and C14 has been deleted to improve colour signal stability for border and mat from serial No. 4ZA00001 and higher.
- o Resistors R102 and R103 have been changed to improve border wipe signal gain from serial No. 55A00001 and higher.
- o Resistors R154, R159 and R162 have been changed to improve the wipe amplifier circuit from serial No. 4YA00001 and higher.
- o Variable resistor VR7 has been deleted and resistors R43, R49 have been changed to improve the border and mat colour generator circuit from serial No. 51A00001 and higher.

o Chroma Key Board

- o Resistors R17, R58, R59, R61 and R62 have been changed to prevent oscillation of chroma key signal from serial No. 47A00001 and higher.

o Wipe Process Board

- o Variable resistor VR1 has been changed to improve the border wipe width control from serial No. 4ZA00001 and higher.

o **Waveform Generator Board**

o Variable resistor VR8 has been deleted, resistor R102 has been added and capacitor C25 has been changed to improve horizontal linearity of wipe parabola signal from serial No. 51A00001 and higher.

o **Modulation Board**

o Capacitor C19 has been changed to improve horizontal linearity of modulation wipe signal from serial No. 4XA00001 and higher.
o Resistor R82 has been added to improve wiping picture stability, when modulation (MOD) ON/OFF switch to ON and OFF from serial No. 47A00001 and higher.

o **Position-1 Board and Lever Board**

o Capacitor C2 has been changed and diode D1 has been added to prevent abnormal function of lamp inside of GEN-LOCK ON/OFF switch.

o **Wipe Lever Unit**

o Capacitors C101 and C102 have been added to prevent the switching noise, when wipe lever moves to upper limit and lower limit from serial No. 49A00001 and higher.

o **Sync, C/Bar Board**

o Resistors R57, R72, R75 and coil L10 have been changed and capacitor C37 has been deleted to prevent the drift of H.sync lock from serial No. 48A00001 and higher.
o Resistor R35 has been changed to improve color bar signal from 47A00001 and higher.
o Capacitor C59 has been changed to improve gen-lock stability from serial No. 4YA00001 and higher.
o Resistor R104, R105, R106 and transistor Q25 have been deleted to prevent the drift of burst subcarrier signal from serial No. 47A00001 and higher.

o **Mother Board**

o A shield jumper wire has been added to prevent crosstalk for program output signal from serial No. 54A00001 and higher. At same time, the pattern layout of this board has been changed.

1. Vol. 2 *Adjustment Procedure*

■ The Adjustment Procedure of step (71) white clip adjustment has been changed from Serial No. 42A00001 and higher.

(71) White clip adjustment

Test points :	Program Output	Rear Panel
	Preview Output	Rear Panel
Adjusts :	VR8 (WHITE CLIP-1)	Output Board
	VR27 (WHITE CLIP-2)	Output Board
Observe :	Waveform monitor	

- Connect the oscilloscope with 75 ohms termination to the Program Output connector or observe waveform monitor.
  Set C/7, Color Bar Selector switch to color bar (C/B) position.
- Select No. 7 (C/B) switches on the Video Input A selector, Video Input B selector and Video Input C selector.
- Select EFF switch on the Video Input Preview/Program selector.
- Set the Mix lever separate and left side lever (EFF Mix lever) to top position, right side lever (INPUT C Mix lever) to bottom position.
- Adjust VR8 (WHITE CLIP-1) so that blanking level to luminance video clip level becomes 0.8V. (Fig. 3-2-58)
- Connect the oscilloscope with 75 ohms termination to the Preview Output connector or observe waveform monitor.
- Adjust VR27 (WHITE CLIP-2) so that blanking level to luminance video clip level becomes 0.8V. (Fig. 3-2-58)

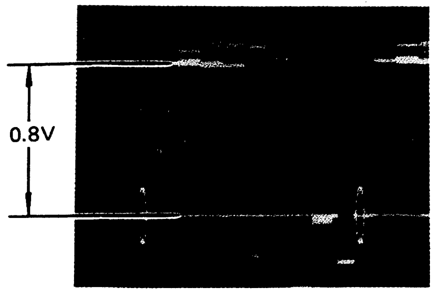
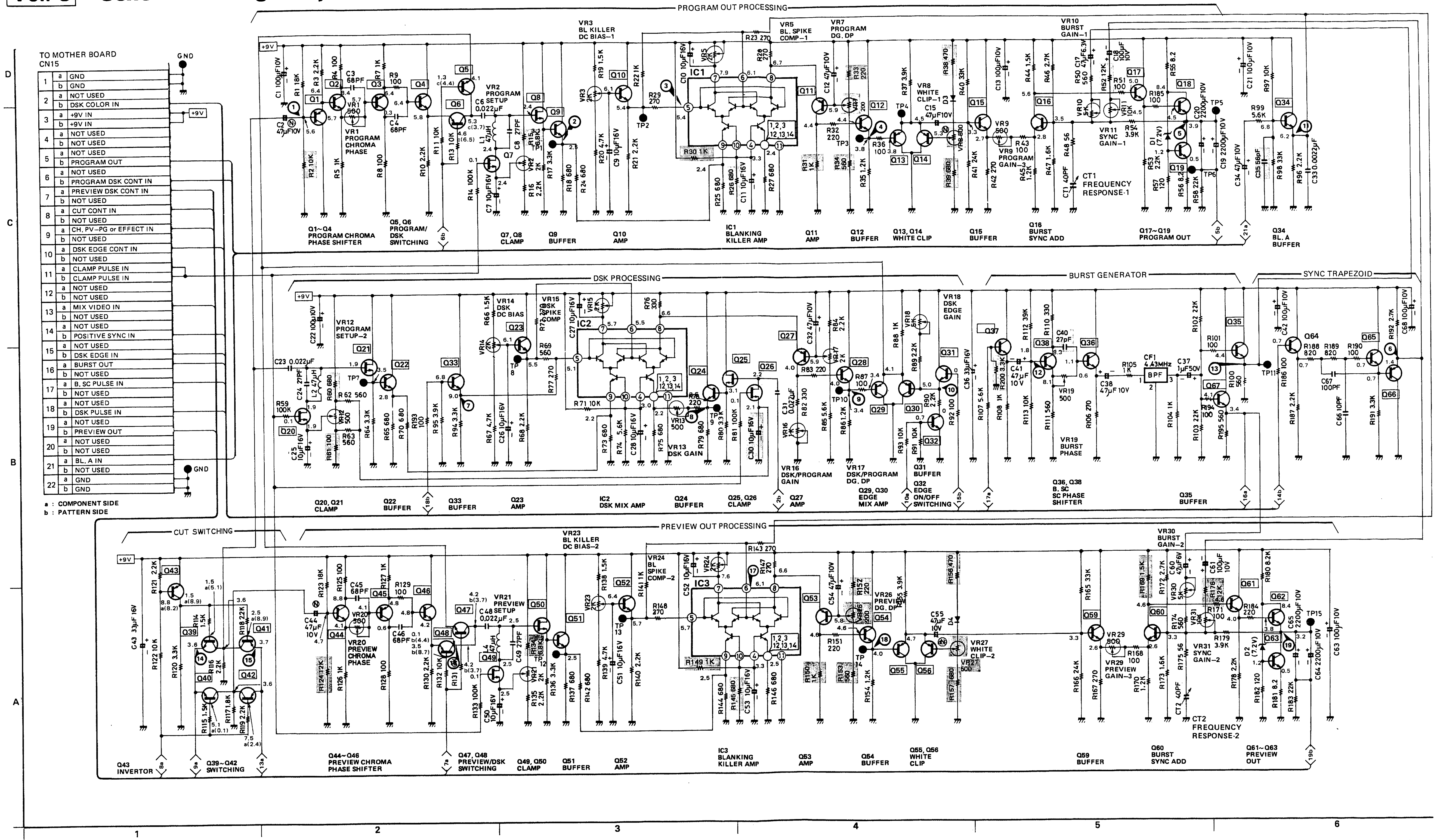


Fig. 3-2-58

SCHEMATIC DIAGRAM OF OUTPUT BOARD


PROGRAM OUT PROCESSING
TO MOTHER BOARD CN15
GND
1 a GND
1 b GND
2 a NOT USED
2 b DSK COLOR IN
3 a +9V IN
3 b +9V IN
4 a NOT USED
4 b NOT USED
5 a NOT USED
5 b PROGRAM OUT
6 a NOT USED
6 b PROGRAM DSK CONT IN
7 a PREVIEW DSK CONT IN
7 b NOT USED
8 a CUT CONT IN
8 b NOT USED
9 a CH. PV-PG or EFFECT IN
9 b NOT USED
10 a DSK EDGE CONT IN
10 b NOT USED
11 a CLAMP PULSE IN
11 b CLAMP PULSE IN
12 a NOT USED
12 b NOT USED
13 a MIX VIDEO IN
13 b NOT USED
14 a NOT USED
14 b POSITIVE SYNC IN
15 a NOT USED
15 b DSK EDGE IN
16 a BURST OUT
16 b NOT USED
17 a B, SC PULSE IN
17 b NOT USED
18 a NOT USED
18 b DSK PULSE IN
19 a NOT USED
19 b PREVIEW OUT
20 a NOT USED
20 b NOT USED
21 a BL, A IN
21 b NOT USED
22 a GND
22 b GND
a : COMPONENT SIDE
b : PATTERN SIDE
VR3 BL KILLER DC BIAS-1
VR5 BL SPIKE COMP-1
VR7 PROGRAM DG, DP
VR10 BURST GAIN-1
VR1 PROGRAM CHROMA PHASE
VR2 PROGRAM SETUP
VR8 WHITE CLIP-1
VR9 PROGRAM GAIN-1
VR11 SYNC GAIN-1
CT1 FREQUENCY RESPONSE-1
Q1~Q4 PROGRAM CHROMA PHASE SHIFTER
Q5, Q6 PROGRAM/DSK SWITCHING
Q7, Q8 CLAMP
Q9 BUFFER
Q10 AMP
IC1 BLANKING KILLER AMP
Q11 AMP
Q12 BUFFER
Q13, Q14 WHITE CLIP
Q15 BUFFER
Q16 BURST SYNC ADD
Q17~Q19 PROGRAM OUT
Q34 BL. A BUFFER
DSK PROCESSING
BURST GENERATOR
SYNC TRAPEZOID
VR12 PROGRAM SETUP-2
VR14 DSK DC BIAS
VR15 DSK SPIKE COMP
VR13 DSK GAIN
VR16 DSK/PROGRAM GAIN
VR17 DSK/PROGRAM DG, DP
VR18 DSK EDGE GAIN
VR19 BURST PHASE
CF1 4.43MHz BPF
Q20, Q21 CLAMP
Q22 BUFFER
Q33 BUFFER
Q23 AMP
IC2 DSK MIX AMP
Q24 BUFFER
Q25, Q26 CLAMP
Q27 AMP
Q29, Q30 EDGE MIX AMP
Q31 BUFFER
Q32 EDGE ON/OFF SWITCHING
Q36, Q38 B, SC PHASE SHIFTER
Q35 BUFFER
CUT SWITCHING
PREVIEW OUT PROCESSING
VR23 BL KILLER DC BIAS-2
VR24 BL SPIKE COMP-2
VR26 PREVIEW DG, DP
VR30 BURST GAIN-2
VR20 PREVIEW CHROMA PHASE
VR21 PREVIEW SETUP
VR27 WHITE CLIP-2
VR29 PREVIEW GAIN-3
VR31 SYNC GAIN-2
CT2 FREQUENCY RESPONSE-2
Q43 INVERTOR
Q39~Q42 SWITCHING
Q44~Q46 PREVIEW CHROMA PHASE SHIFTER
Q47, Q48 PREVIEW/DSK SWITCHING
Q49, Q50 CLAMP
Q51 BUFFER
Q52 AMP
IC3 BLANKING KILLER AMP
Q53 AMP
Q54 BUFFER
Q55, Q56 WHITE CLIP
Q59 BUFFER
Q60 BURST SYNC ADD
Q61~Q63 PREVIEW OUT
1
2
3
4
5
6
A
B
C
D

Voltages are measured by following conditions

a( ) : CUT → ON

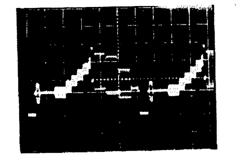
b( ) : DSK PV PG → ON

c( ) : DSK → ON

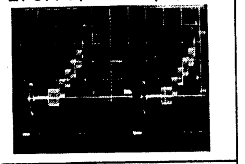
Changed components are shown by shading (▨).

IC1	AN610P	C3, C4
IC2	AN610P	B3
IC3	AN610P	A3, A4
Q1	2SA1254-BC	C2
Q2	2SD636-RS	D2
Q3	2SA1254-BC	D2
Q4	2SD636-RS	D2
Q5	2SC2377CD	D2
Q6	2SA1254-BC	C2
Q7	2SK34-CD	C2, C3
Q8	2SK19-Y	C3
Q9	2SD636-RS	C3
Q10	2SD636-RS	D3
Q11	2SA1254-BC	C4
Q12	2SD636-RS	C4
Q13	2SA1254-BC	C4
Q14	2SA1254-BC	C4
Q15	2SD636-RS	C5
Q16	2SC2377CD	C5
Q17	2SD636-RS	D5
Q18	2SD639RS	C5
Q19	2SD639RS	C5
Q20	2SK34-CD	B2
Q21	2SK19-Y	B2
Q22	2SD636-RS	B2
Q23	2SD636-RS	B3
Q24	2SD636-RS	B3
Q25	2SK19-Y	B3
Q26	2SK34-CD	B4
Q27	2SA1254-BC	B4
Q28	2SD636-RS	B4
Q29	2SA1254-BC	B4
Q30	2SA1254-BC	B4
Q31	2SD636-RS	B4
Q32	2SD636-RS	B4
Q33	2SD636-RS	B2
Q34	2SD636-RS	C6
Q35	2SD636-RS	B6
Q36	2SD636-RS	B5
Q38	2SD636-RS	B5
Q39	2SC2377CD	A1
Q40	2SC2377CD	A1
Q41	2SA1254-BC	A1
Q42	2SA1254-BC	A1
Q43	2SA1254-BC	A1
Q44	2SD636-RS	A2
Q45	2SA1254-BC	A2
Q46	2SD636-RS	A2
Q47	2SC2377CD	A2
Q48	2SA1254-BC	A2
Q49	2SK34-CD	A2
Q50	2SK19-Y	A3
Q51	2SD636-RS	A3
Q52	2SD636-RS	A3
Q53	2SA1254-BC	A4
Q54	2SD636-RS	A4
Q55	2SA1254-BC	A4
Q56	2SA1254-BC	A4
Q57	2SD636-RS	A5
Q58	2SA1254-BC	A5
Q59	2SD636-RS	A5
Q60	2SC2377CD	A5
Q61	2SD636-RS	A6
Q62	2SD639RS	A6
Q63	2SD639RS	A6
Q64	2SD636-RS	B6
Q65	2SD636-RS	B6
Q66	2SA1254-BC	B6
Q67	2SC828-QR	B5
Q201	2SC828-QR	B6
D1	MA4075L	C5
D2	MA4075L	A6
D3	MA27WA	D4
D4	MA27WA	A4

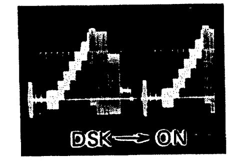
1. 0.2V/DIV 10μs/DIV



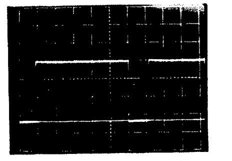
2. 0.1V/DIV 10μs/DIV



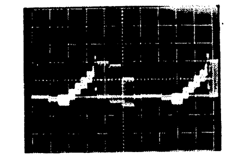
2. 0.1V/DIV 10μs/DIV



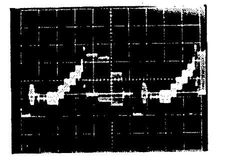
3. 0.5V/DIV 10μs/DIV



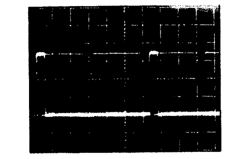
4. 0.2V/DIV 10μs/DIV



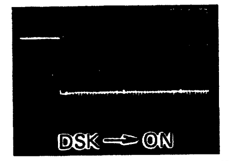
5. 0.5V/DIV 10μs/DIV



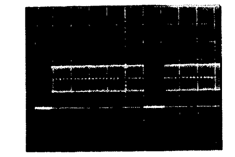
6. 2.0V/DIV 10μs/DIV



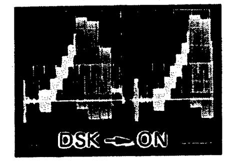
7. 0.5V/DIV 20μs/DIV



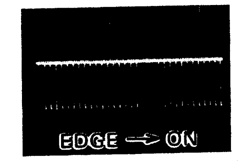
8. 0.2V/DIV 10μs/DIV



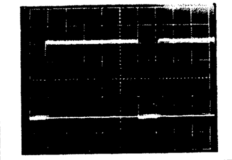
9. 0.1V/DIV 10μs/DIV



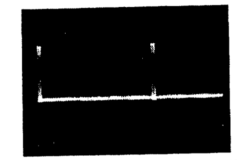
10. 0.2V/DIV 10μs/DIV



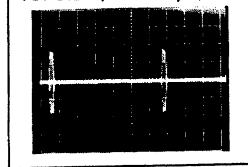
11. 0.5V/DIV 10μs/DIV



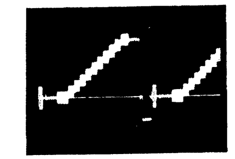
12. 0.5V/DIV 10μs/DIV



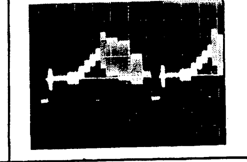
13. 0.2V/DIV 10μs/DIV



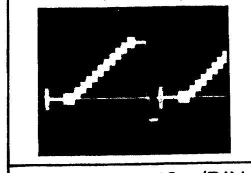
14. 0.2V/DIV 10μs/DIV



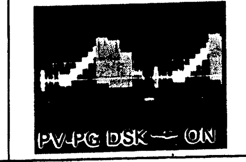
15. 0.2V/DIV 10μs/DIV



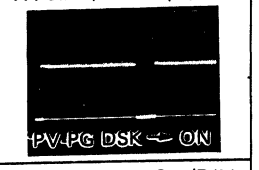
16. 0.2V/DIV 10μs/DIV



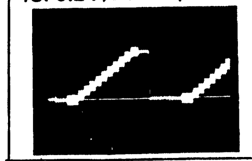
16. 0.5V/DIV 10μs/DIV



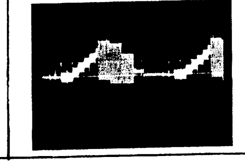
17. 0.2V/DIV 10μs/DIV



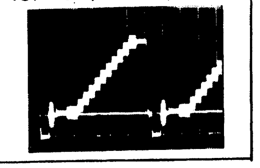
18. 0.2V/DIV 10μs/DIV



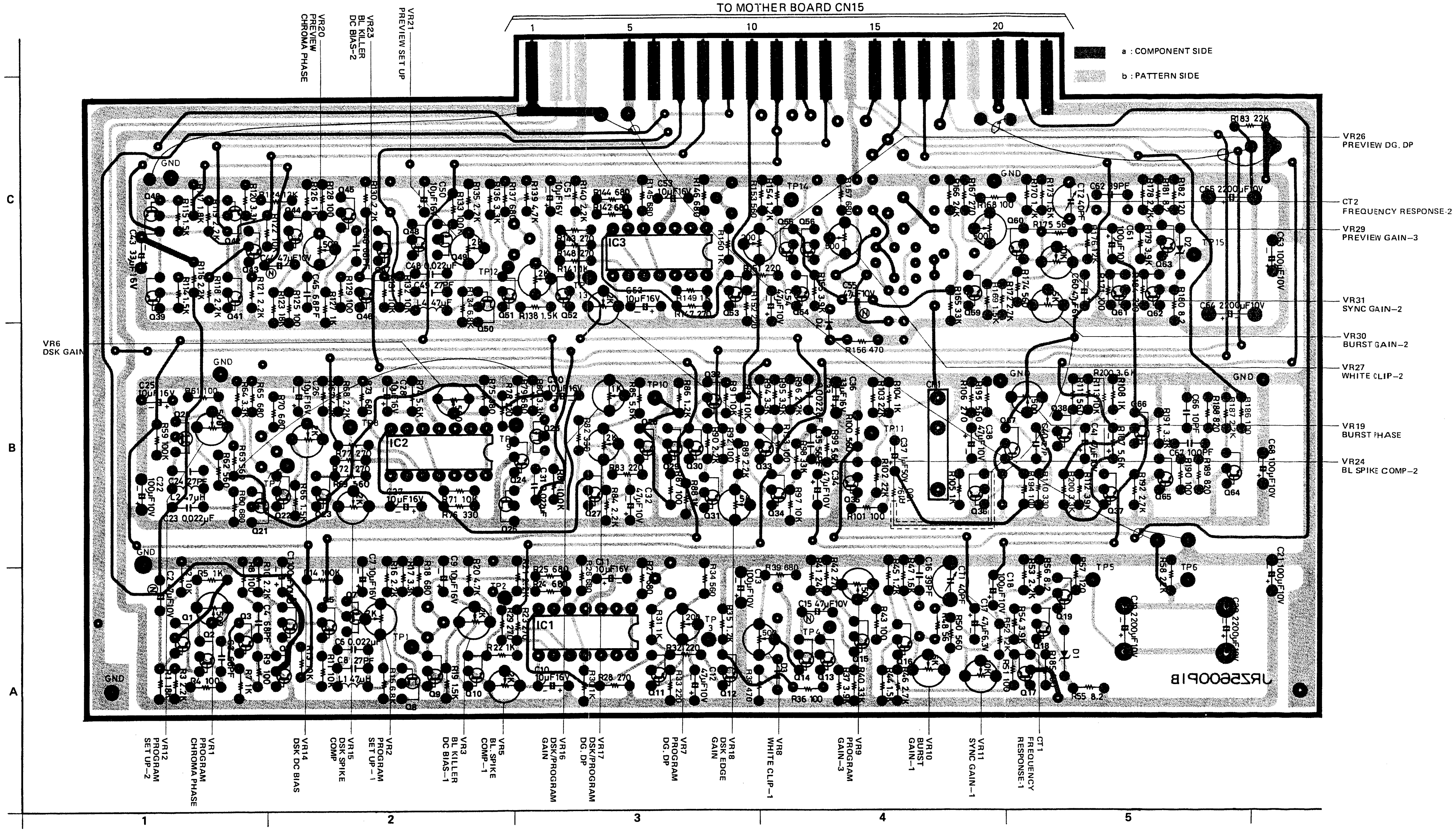
18. 0.2V/DIV 10μs/DIV



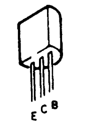
19. 0.5V/DIV 10μs/DIV



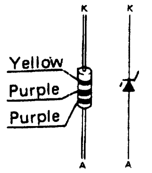
CONDUCTOR VIEW OF OUTPUT BOARD


TO MOTHER BOARD CN15
1
5
10
15
20
a : COMPONENT SIDE
b : PATTERN SIDE
VR20 PREVIEW CHROMA PHASE
VR23 BL KILLER DC BIAS-2
VR21 PREVIEW SET UP
VR26 PREVIEW DG. DP
CT2 FREQUENCY RESPONSE-2
VR29 PREVIEW GAIN-3
VR31 SYNC GAIN-2
VR30 BURST GAIN-2
VR27 WHITE CLIP-2
VR19 BURST PHASE
VR24 BL SPIKE COMP-2
VR6 DSK GAIN
VR12 PROGRAM SET UP-2
VR1 PROGRAM CHROMA PHASE
VR14 DSK DC BIAS
VR15 DSK SPIKE COMP
VR2 PROGRAM SET UP-1
VR3 BL KILLER DC BIAS-1
VR5 BL. SPIKE COMP-1
VR16 DSK/PROGRAM GAIN
VR17 DSK/PROGRAM DG. DP
VR7 PROGRAM DG. DP
VR18 DSK EDGE GAIN
VR8 WHITE CLIP-1
VR9 PROGRAM GAIN-3
VR10 BURST GAIN-1
VR11 SYNC GAIN-1
CT1 FREQUENCY RESPONSE-1
IC1
IC2
IC3
GND
A
B
C
1
2
3
4
5

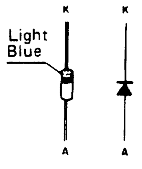
2SC828-QR



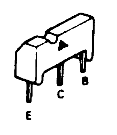
MA4075L


K
K
Yellow
Purple
Purple
A
A

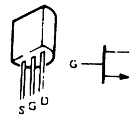
MA27WA


K
K
Light Blue
A
A

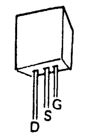
2SA1254-BC
2SB641-RS
2SC2377CD
2SD636-RS
2SD639RS



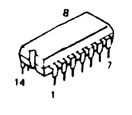
2SK34-CD



2SK19-Y

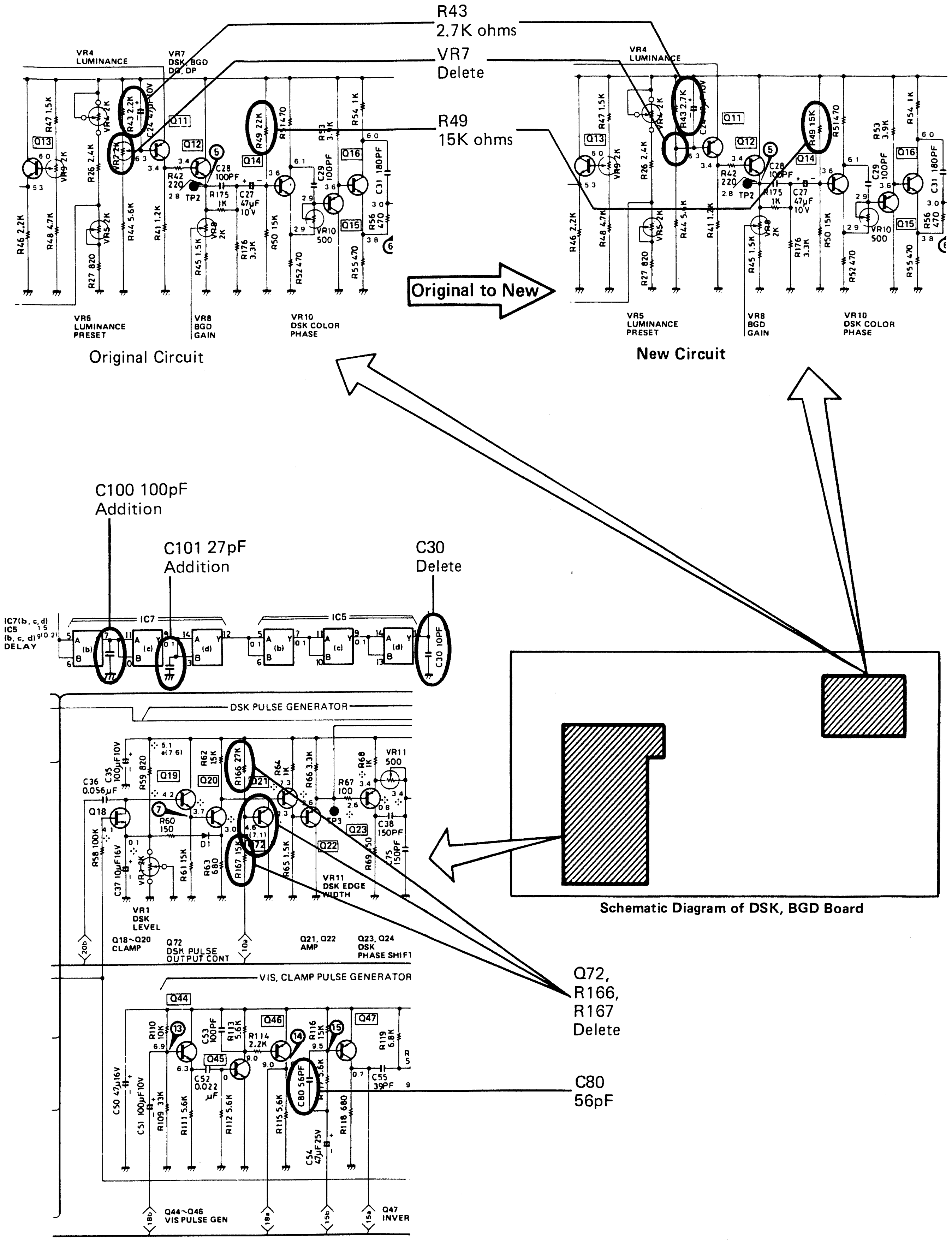


AN610P



IC1	AN610P	A3
IC2	AN610P	B2
IC3	AN610P	C3
Q1	2SA1254-BC	A1
Q2	2SD636-RS	A1
Q3	2SA1254-BC	A1
Q4	2SD636-RS	A2
Q5	2SC2377CD	A2
Q6	2SA1254-BC	A2
Q7	2SK34-CD	A2
Q8	2SK19-Y	A2
Q9	2SD636-RS	A2
Q10	2SD636-RS	A2
Q11	2SA1254-BC	A3
Q12	2SD636-RS	A3
Q13	2SA1254-BC	A4
Q14	2SA1254-BC	A4
Q15	2SD636-RS	A4
Q16	2SC2377CD	A4
Q17	2SD636-RS	A5
Q18	2SD639RS	A5
Q19	2SD639RS	A5
Q20	2SK34-CD	B1
Q21	2SK19-Y	B1
Q22	2SD636-RS	B2
Q23	2SD636-RS	B2
Q24	2SD636-RS	B3
Q25	2SK19-Y	B2
Q26	2SK34-CD	B3
Q27	2SA1254-BC	B3
Q28	2SD636-RS	B3
Q29	2SA1254-BC	B3
Q30	2SA1254-BC	B3
Q31	2SD636-RS	B3
Q32	2SD636-RS	B3
Q33	2SD636-RS	B4
Q34	2SD636-RS	B4
Q35	2SD636-RS	B4
Q36	2SD636-RS	B4
Q38	2SD636-RS	B5
Q39	2SC2377CD	C1
Q40	2SC2377CD	C1
Q41	2SA1254-BC	C1
Q42	2SA1254-BC	C1
Q43	2SA1254-BC	C1
Q44	2SD636-RS	C2
Q45	2SA1254-BC	C2
Q46	2SD636-RS	C2
Q47	2SC2377CD	C2
Q48	2SA1254-BC	C2
Q49	2SK34-CD	C2
Q50	2SK19-Y	C2
Q51	2SD636-RS	C2
Q52	2SD636-RS	C3
Q53	2SA1254-BC	C3
Q54	2SD636-RS	C4
Q55	2SA1254-BC	C4
Q56	2SA1254-BC	C4
Q57	2SD636-RS	C4
Q58	2SA1254-BC	C4
Q59	2SD636-RS	C4
Q60	2SC2377CD	C5
Q61	2SD636-RS	C5
Q62	2SD639RS	C5
Q63	2SD639RS	C5
Q64	2SD636-RS	B5
Q65	2SD636-RS	B5
Q66	2SA1254-BC	B5
Q67	2SC828-QR	B5
Q201	2SC828-QR	B4
D1	MA4075L	A5
D2	MA4075L	C5
D3	MA27WA	A3
D4	MA27WA	C4

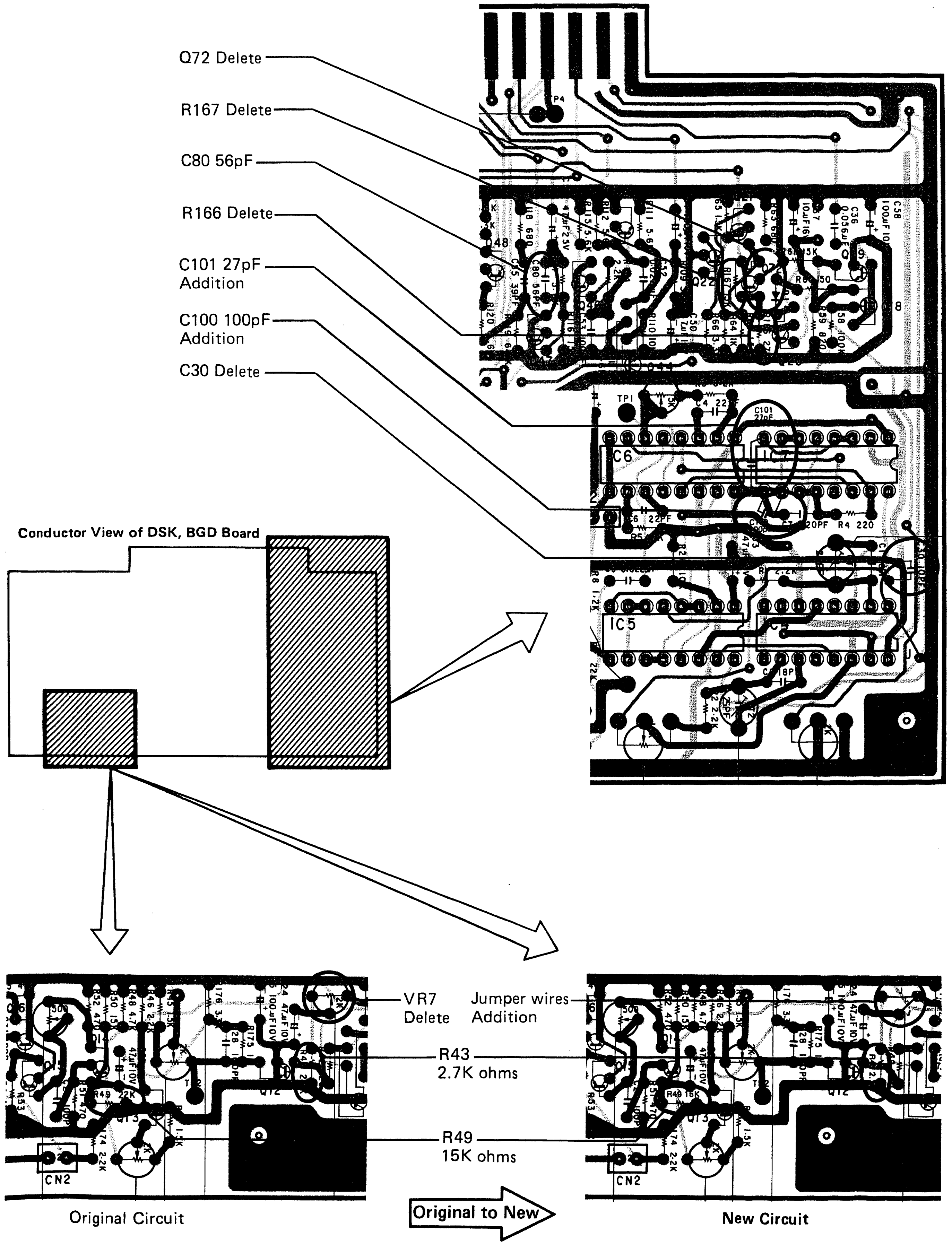
■ DSK. BGD Board


R43
2.7K ohms
VR7
Delete
R49
15K ohms
Original to New
VR4 LUMINANCE
VR7 DSK BGD DC. DP
VR5 LUMINANCE PRESET
VR8 BGD GAIN
VR10 DSK COLOR PHASE
C100 100pF
Addition
C101 27pF
Addition
C30
Delete
IC7
IC5
IC7(b, c, d) IC5 (b, c, d) DELAY
DSK PULSE GENERATOR
VR11 DSK EDGE WIDTH
VR1 DSK LEVEL
Q18~Q20 CLAMP
Q72 DSK PULSE OUTPUT CONT
Q21, Q22 AMP
Q23, Q24 DSK PHASE SHIFT
VIS. CLAMP PULSE GENERATOR
Q44~Q46 VIS PULSE GEN
Q47 INVER
Q72,
R166,
R167
Delete
C80
56pF

Original Circuit

New Circuit

Schematic Diagram of DSK, BGD Board

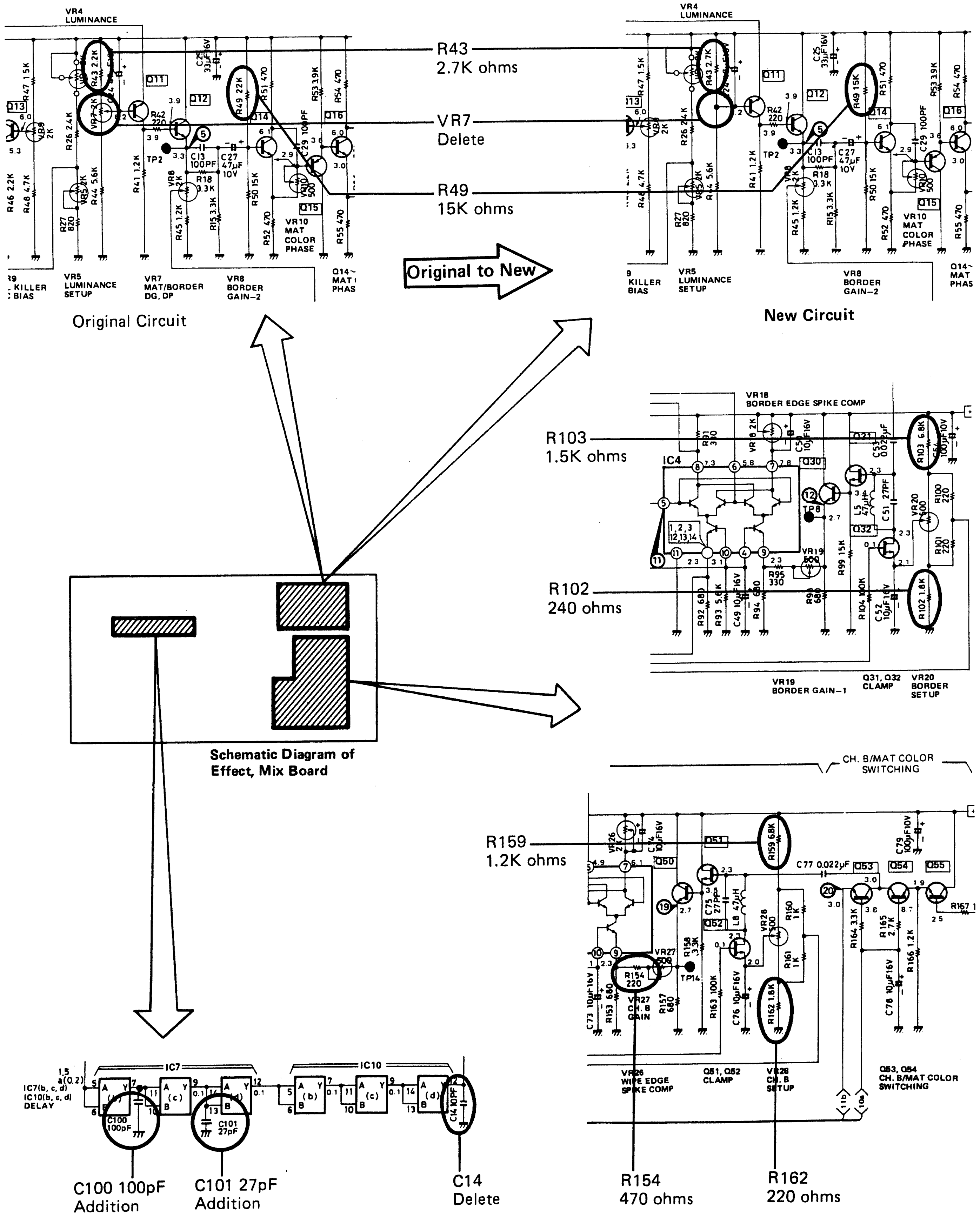

Q72 Delete
R167 Delete
C80 56pF
R166 Delete
C101 27pF
Addition
C100 100pF
Addition
C30 Delete
IC6
IC7
IC5
CN2
VR7
Delete
Jumper wires
Addition
R43
2.7K ohms
R49
15K ohms
Original to New

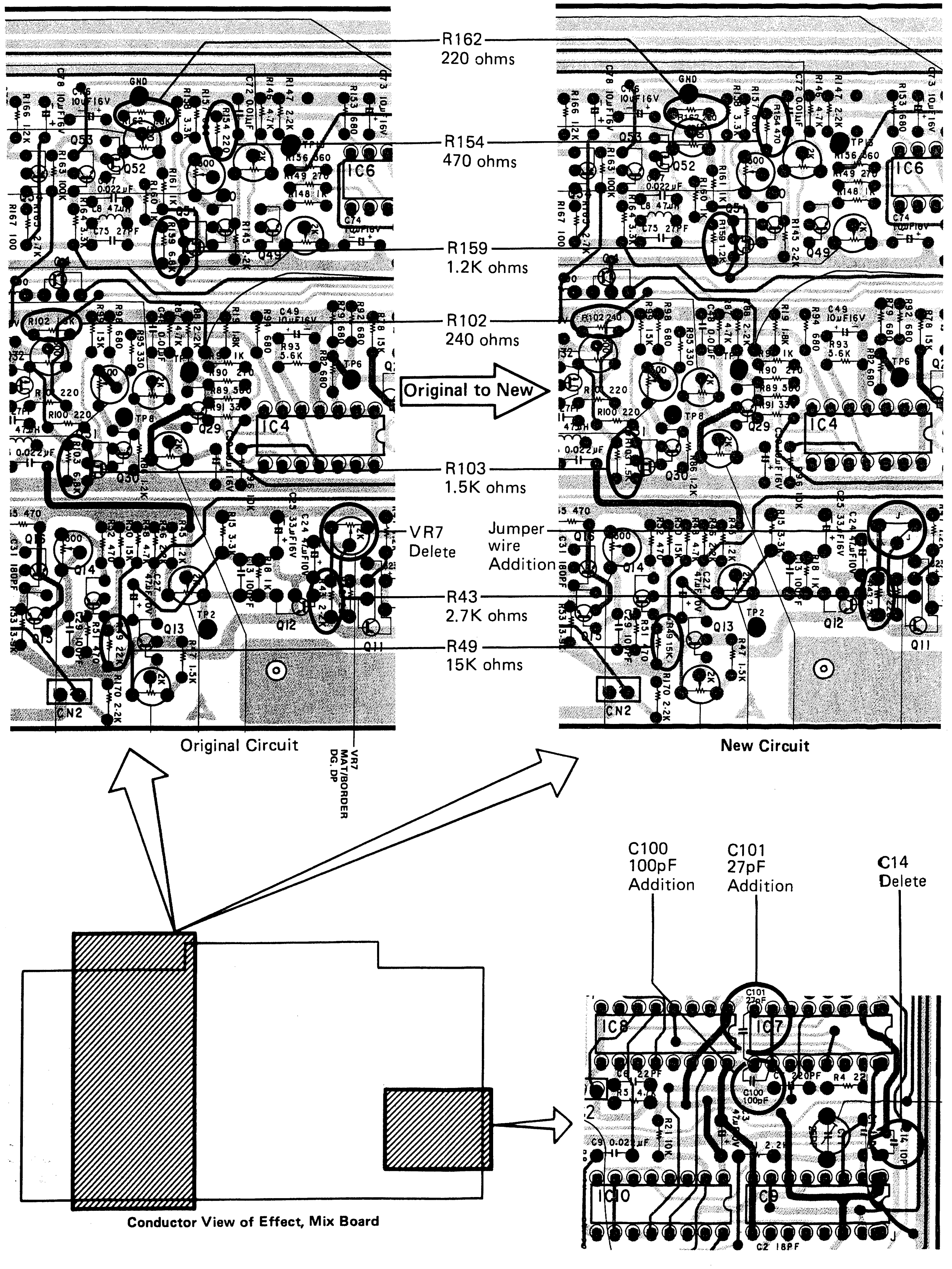
Conductor View of DSK, BGD Board

Original Circuit

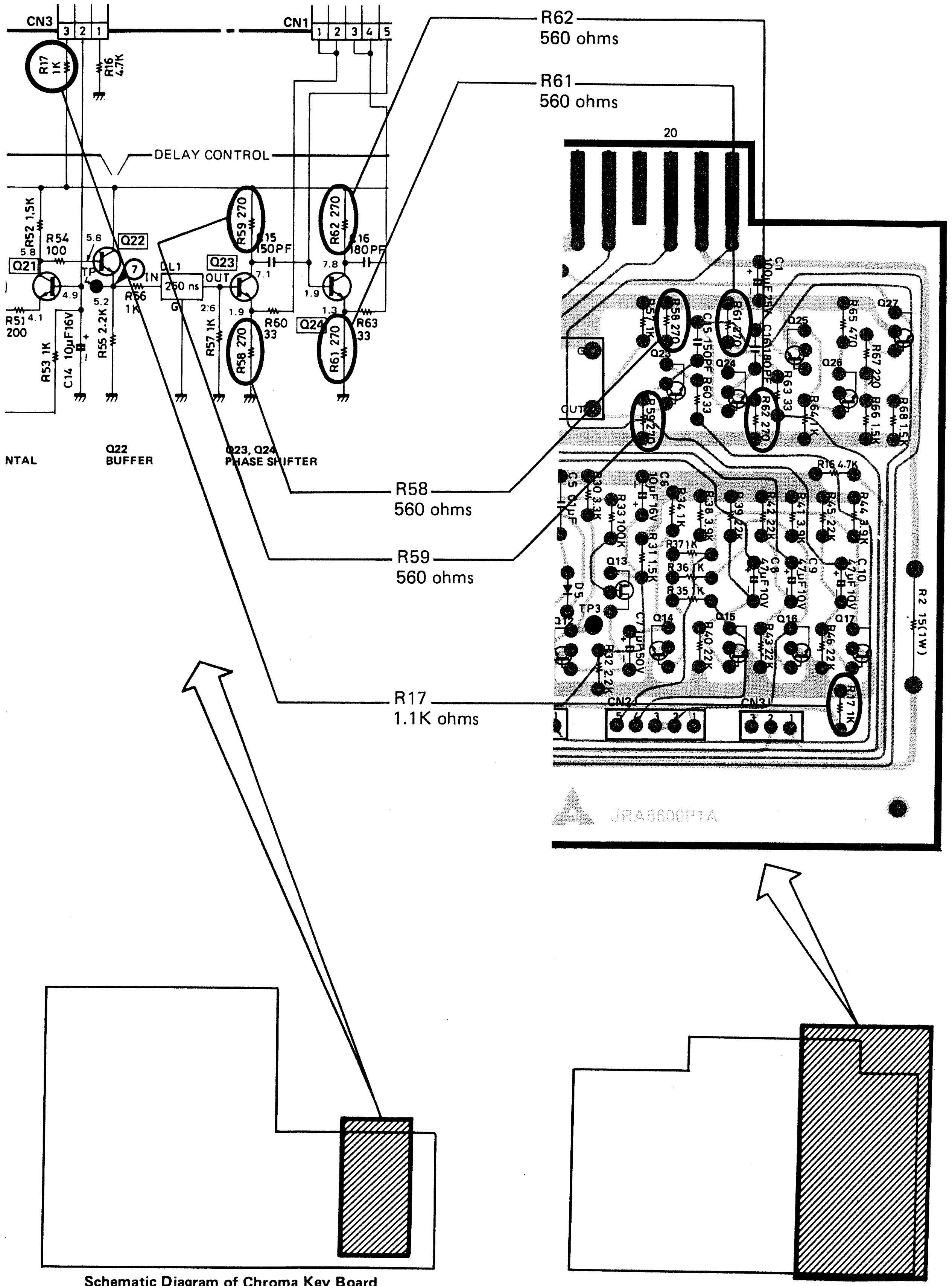
New Circuit

■ EFFECT, MIX Board


VR4 LUMINANCE
R43
2.7K ohms
VR7
Delete
R49
15K ohms
Original to New
VR5 LUMINANCE SETUP
VR7 MAT/BORDER DG, DP
VR8 BORDER GAIN-2
VR10 MAT COLOR PHASE
KILLER BIAS
Original Circuit
New Circuit
VR18 BORDER EDGE SPIKE COMP
R103
1.5K ohms
R102
240 ohms
IC4
VR19 BORDER GAIN-1
Q31, Q32 CLAMP
VR20 BORDER SETUP
Schematic Diagram of Effect, Mix Board
CH. B/MAT COLOR SWITCHING
R159
1.2K ohms
VR26 WIPE EDGE SPIKE COMP
Q51, Q52 CLAMP
VR28 CH. B SETUP
Q53, Q54 CH. B/MAT COLOR SWITCHING
VR27 CH. B GAIN
IC7(b, c, d) IC10(b, c, d) DELAY
IC7
IC10
C100 100pF
Addition
C101 27pF
Addition
C14
Delete
R154
470 ohms
R162
220 ohms


R162
220 ohms
R154
470 ohms
R159
1.2K ohms
R102
240 ohms
Original to New
R103
1.5K ohms
VR7
Delete
Jumper wire Addition
R43
2.7K ohms
R49
15K ohms
IC6
IC4
CN2
Original Circuit
New Circuit
VR7 MAT/BORDER DG, DP
C100
100pF
Addition
C101
27pF
Addition
C14
Delete
IC7
IC8
IC10
IC9
Conductor View of Effect, Mix Board

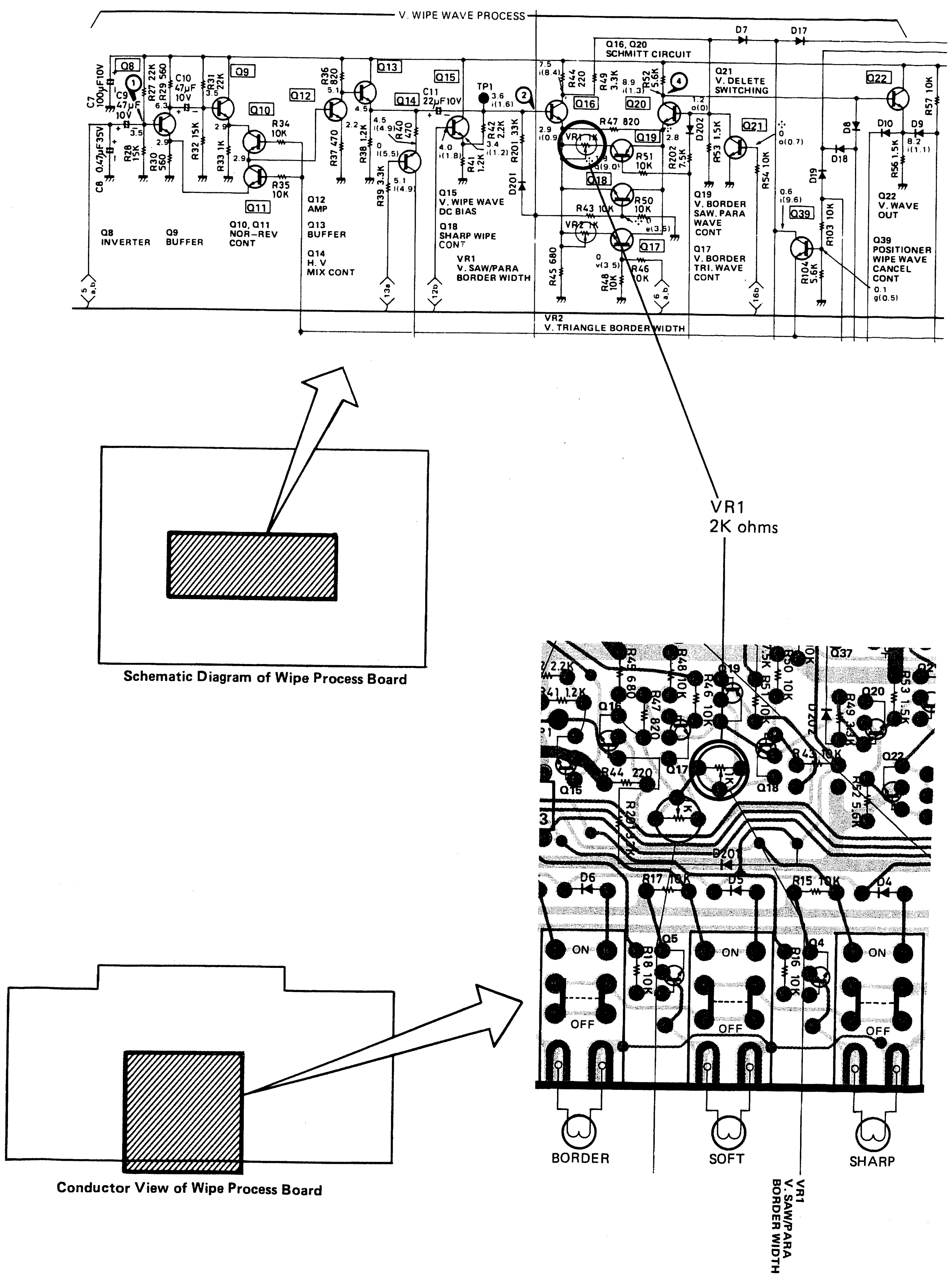
■ CHROMA KEY Board


CN3
CN1
DELAY CONTROL
R62
560 ohms
R61
560 ohms
R58
560 ohms
R59
560 ohms
R17
1.1K ohms
Q22
BUFFER
Q23, Q24
PHASE SHIFTER
NTAL
JRA5600P1A

Schematic Diagram of Chroma Key Board

Conductor View of Chroma Key Board

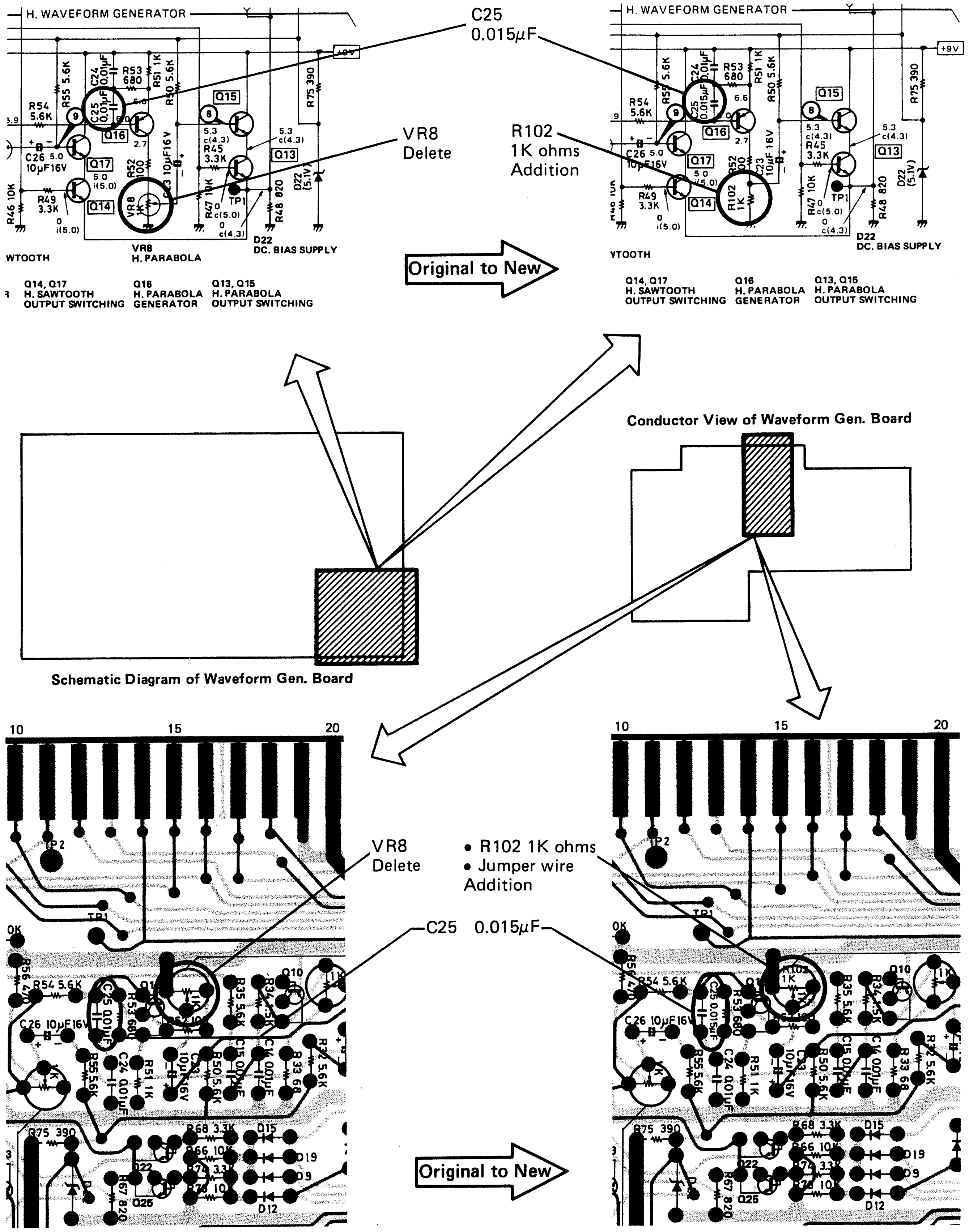
■ WIPE PROCESS Board


V. WIPE WAVE PROCESS
Q8
INVERTER
Q9
BUFFER
Q10, Q11
NOR–REV
CONT
Q12
AMP
Q13
BUFFER
Q14
H. V
MIX CONT
Q15
V. WIPE WAVE
DC BIAS
Q18
SHARP WIPE
CONT
VR1
V. SAW/PARA
BORDER WIDTH
Q16, Q20
SCHMITT CIRCUIT
Q21
V. DELETE
SWITCHING
Q19
V. BORDER
SAW. PARA
WAVE
CONT
Q17
V. BORDER
TRI. WAVE
CONT
Q22
V. WAVE
OUT
Q39
POSITIONER
WIPE WAVE
CANCEL
CONT
VR2
V. TRIANGLE BORDER WIDTH
VR1
2K ohms
ON
OFF
BORDER
SOFT
SHARP
VR1
V. SAW/PARA
BORDER WIDTH

Schematic Diagram of Wipe Process Board

Conductor View of Wipe Process Board

■ **WAVEFORM GEN. Board**


H. WAVEFORM GENERATOR
C25
0.015µF
VR8
Delete
R102
1K ohms
Addition
Original to New
Q14, Q17
H. SAWTOOTH
OUTPUT SWITCHING
Q16
H. PARABOLA
GENERATOR
Q13, Q15
H. PARABOLA
OUTPUT SWITCHING
VR8
H. PARABOLA
D22
DC. BIAS SUPPLY
+9V
10
15
20
VR8
Delete
• R102 1K ohms
• Jumper wire
Addition
C25 0.015µF
Original to New

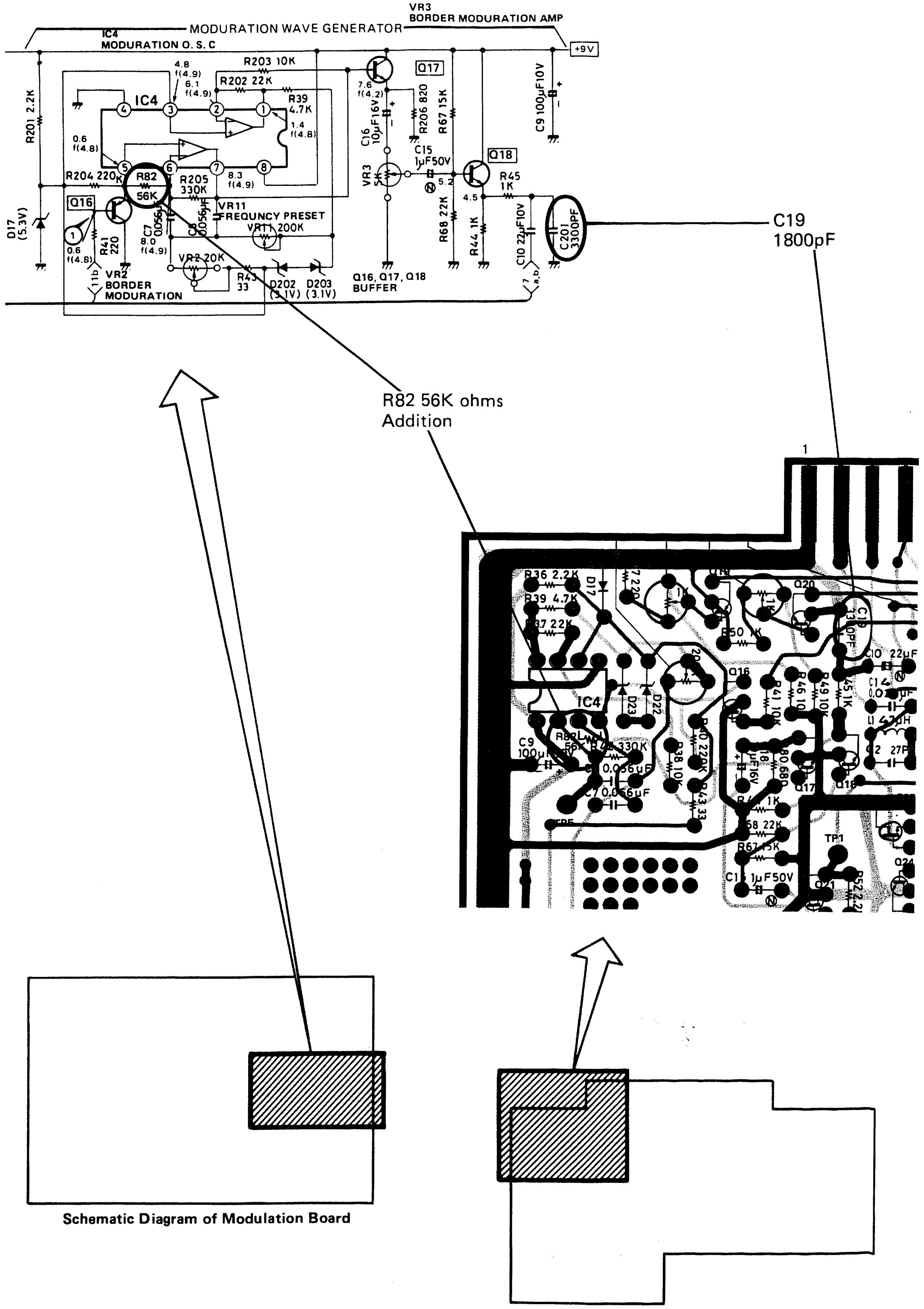
Conductor View of Waveform Gen. Board

Schematic Diagram of Waveform Gen. Board

Original Circuit

New Circuit

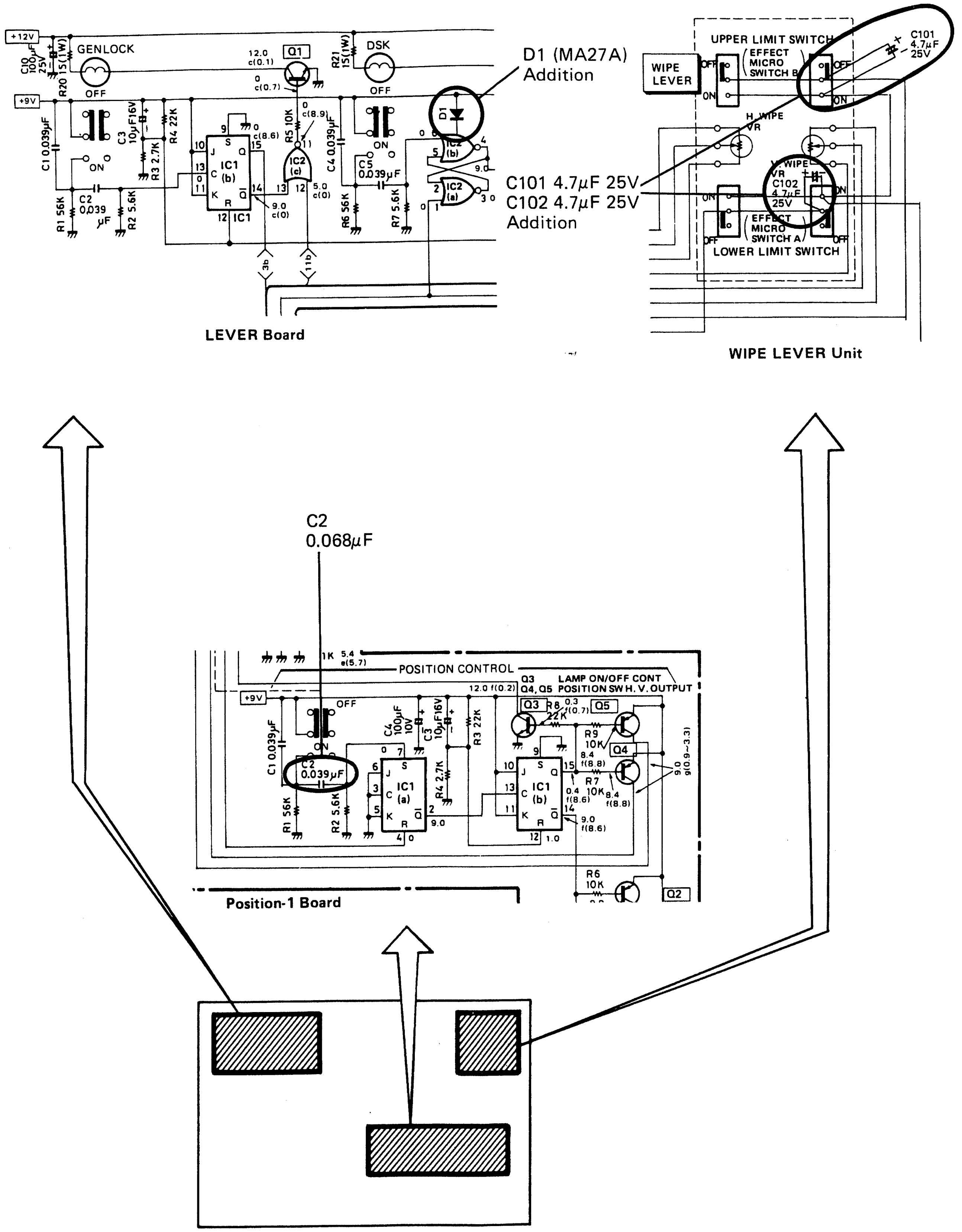
■ **MODULATION Board**


VR3
BORDER MODURATION AMP
MODURATION WAVE GENERATOR
IC4
MODURATION O. S. C
+9V
IC4
R82
56K
VR11
FREQUNCY PRESET
VR2
BORDER
MODURATION
Q16, Q17, Q18
BUFFER
C201
330PF
C19
1800pF
R82 56K ohms
Addition
1

Schematic Diagram of Modulation Board

Conductor View of Modulation Board

■ LEVER Board/POSITION-1 Board/WIPE LEVER Unit


GENLOCK
DSK
OFF
ON
Q1
IC1 (b)
IC2 (c)
IC2 (b)
IC2 (a)
D1
LEVER Board
WIPE LEVER
UPPER LIMIT SWITCH
EFFECT MICRO SWITCH B
H. WIPE VR
V. WIPE VR
EFFECT MICRO SWITCH A
LOWER LIMIT SWITCH
C101 4.7μF 25V
C102 4.7μF 25V
WIPE LEVER Unit
POSITION CONTROL
LAMP ON/OFF CONT
Q4, Q5 POSITION SW H. V. OUTPUT
Q3
Q4
Q5
Q2
C2 0.039μF
Position-1 Board

D1 (MA27A)
Addition

C101 4.7μF 25V
C102 4.7μF 25V
Addition

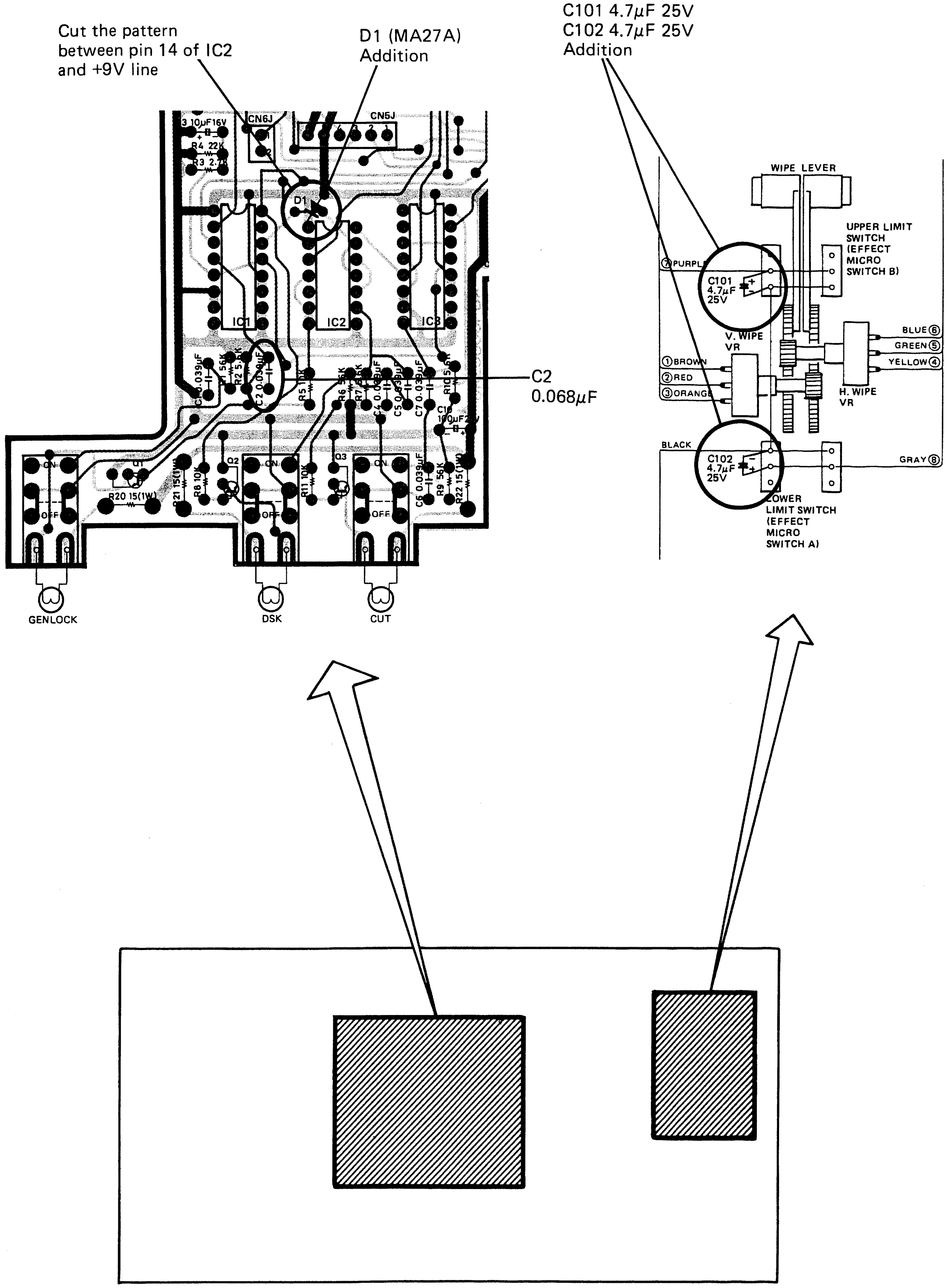
C2
0.068μF

Schematic Diagram of
Lever Board/Position-1 Board/Position-2 Board

Cut the pattern
between pin 14 of IC2
and +9V line

D1 (MA27A)
Addition

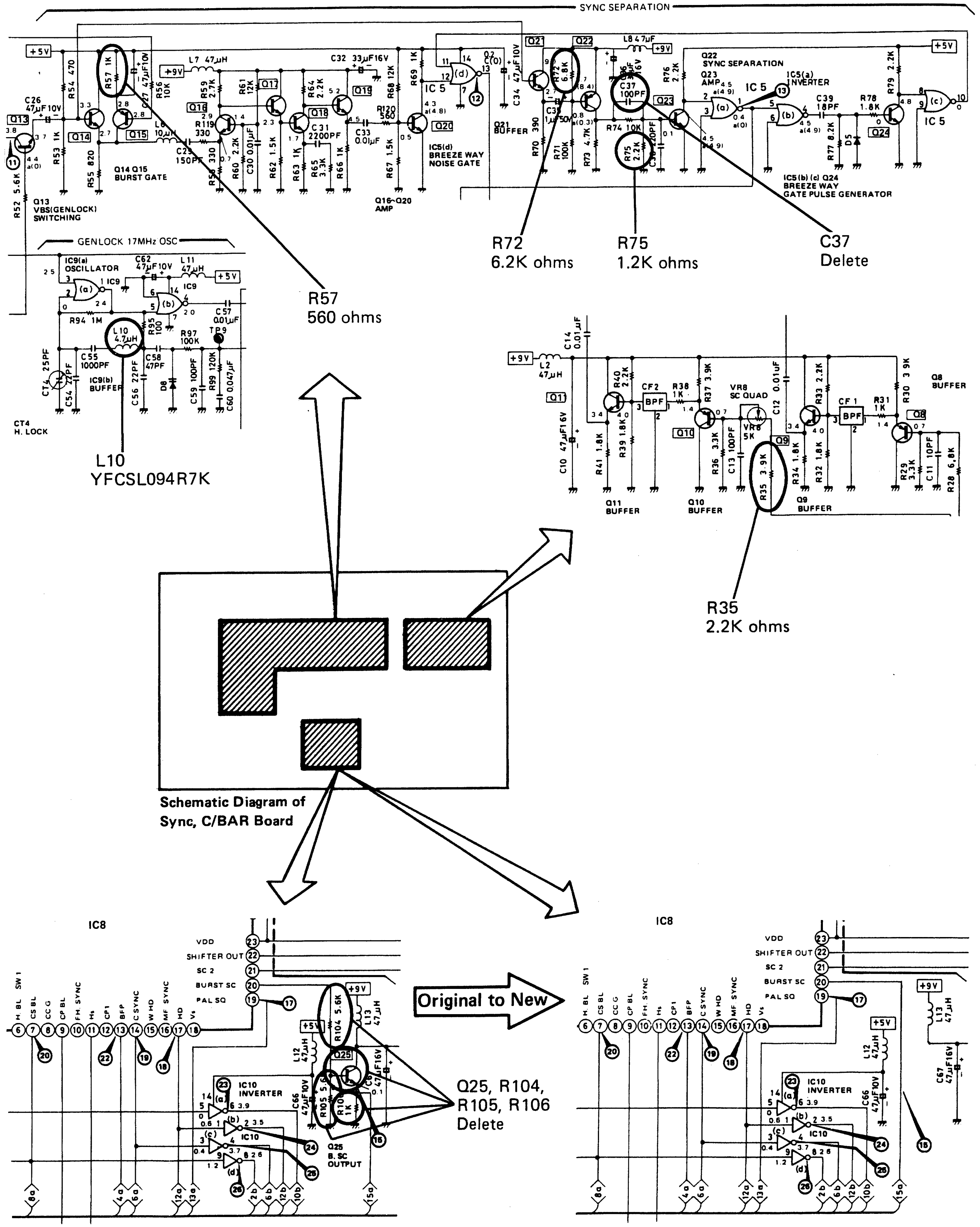
C101 4.7μF 25V
C102 4.7μF 25V
Addition


CN6J
CN5J
D1
IC1
IC2
IC3
Q1
Q2
Q3
GENLOCK
DSK
CUT
WIPE LEVER
UPPER LIMIT SWITCH (EFFECT MICRO SWITCH B)
C101 4.7μF 25V
⑦PURPLE
V. WIPE VR
①BROWN
②RED
③ORANGE
BLUE⑥
GREEN⑤
YELLOW④
H. WIPE VR
BLACK
C102 4.7μF 25V
GRAY⑧
LOWER LIMIT SWITCH (EFFECT MICRO SWITCH A)

C2
0.068μF

Conductor View of Lever Board/Position-1 Board/Position-2 Board

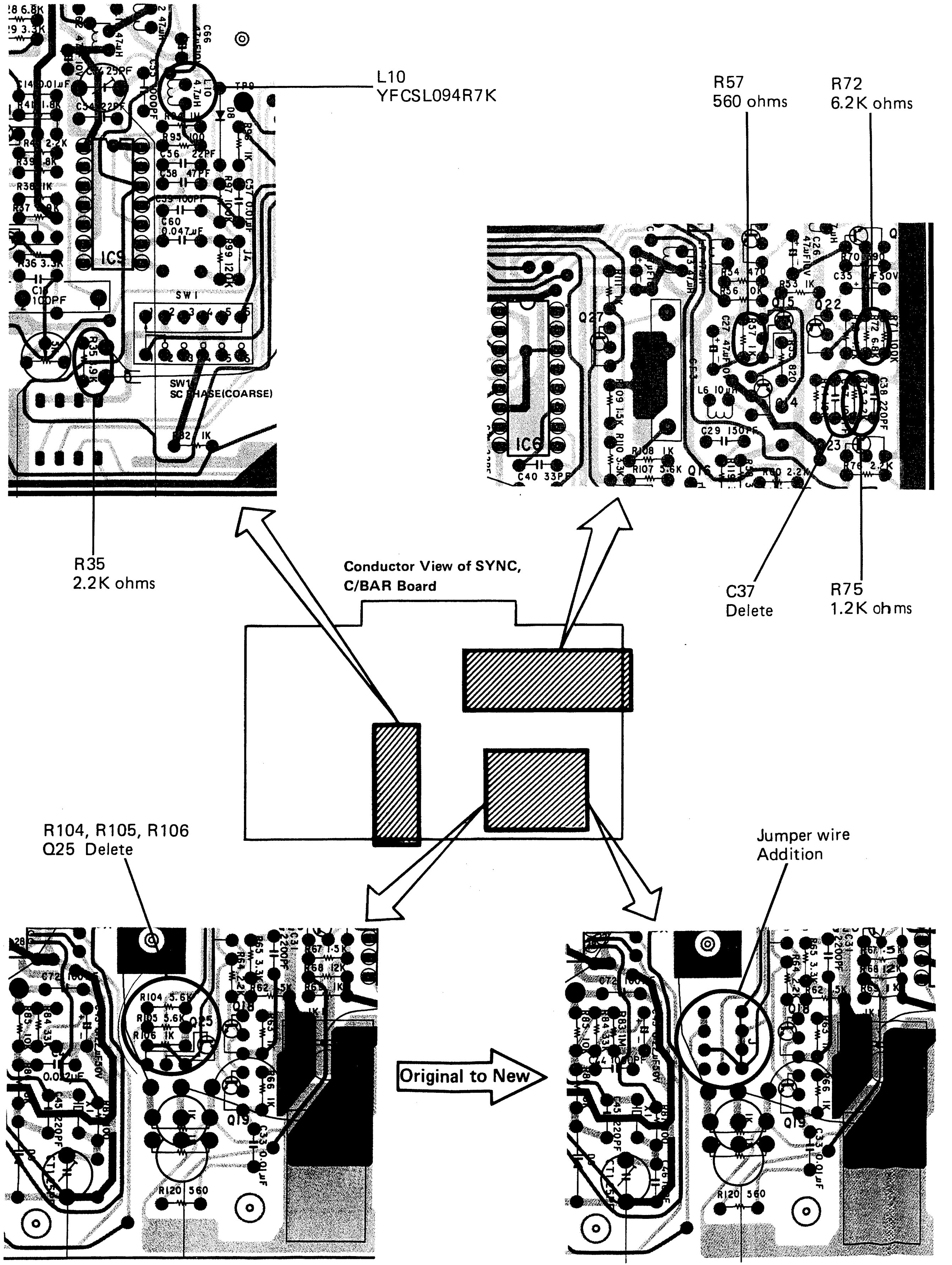
■ SYNC, C/BAR Board


SYNC SEPARATION
Q13 VBS(GENLOCK) SWITCHING
Q14 Q15 BURST GATE
IC5(d) BREEZE WAY NOISE GATE
Q16-Q20 AMP
Q21 BUFFER
Q22 SYNC SEPARATION
Q23 AMP
IC5(a) INVERTER
IC5(b) (c) Q24 BREEZE WAY GATE PULSE GENERATOR
GENLOCK 17MHz OSC
IC9(a) OSCILLATOR
IC9(b) BUFFER
CT4 H. LOCK
R72
6.2K ohms
R75
1.2K ohms
C37
Delete
R57
560 ohms
L10
YFCSL094R7K
Q11 BUFFER
Q10 BUFFER
Q9 BUFFER
Q8 BUFFER
VR8 SC QUAD
R35
2.2K ohms
IC8
IC10 INVERTER
Q25 B. SC OUTPUT
Original to New
Q25, R104,
R105, R106
Delete

Schematic Diagram of Sync, C/BAR Board

Original Circuit

New Circuit

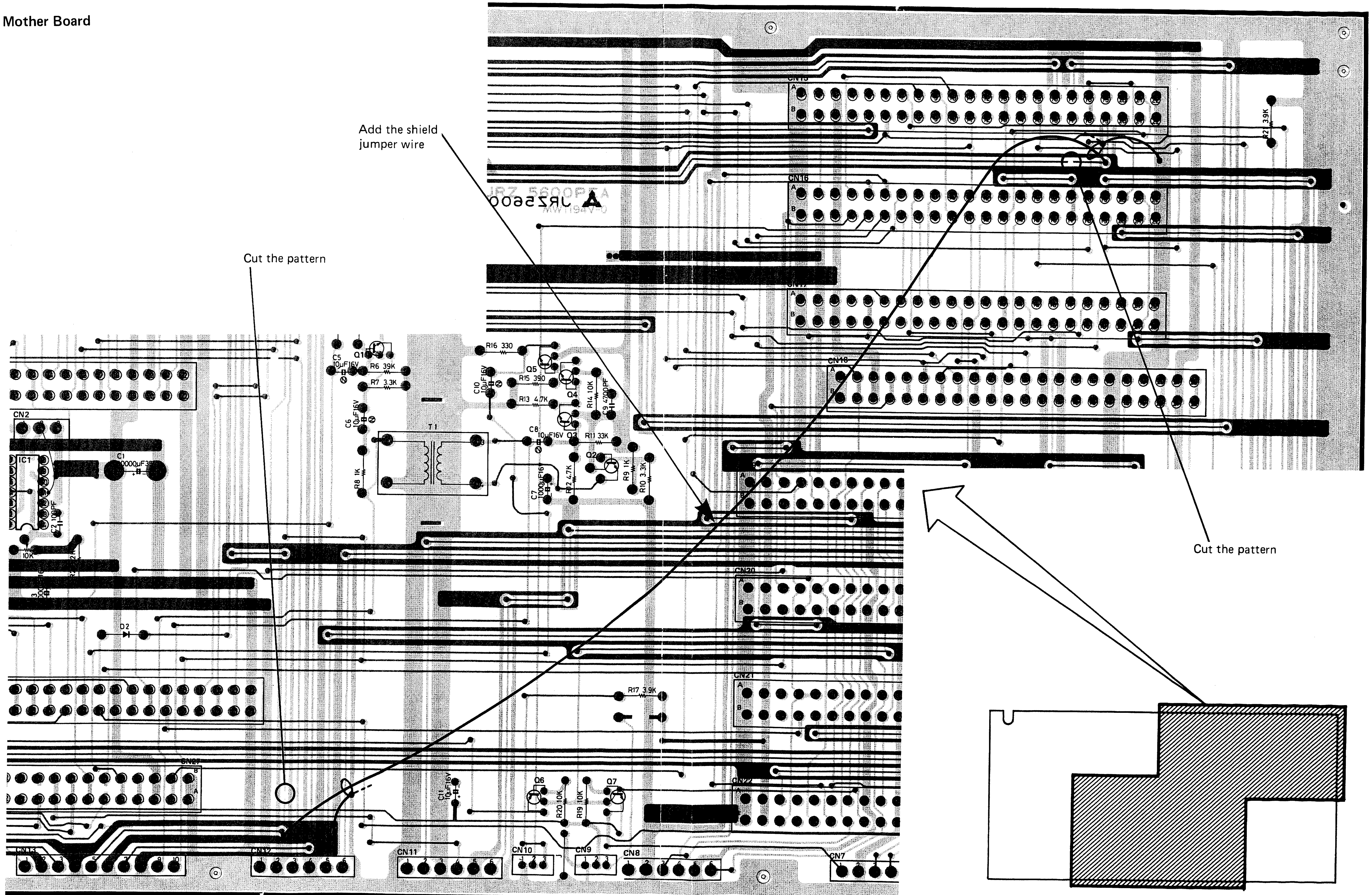

L10
YFCSL094R7K
R57
560 ohms
R72
6.2K ohms
R35
2.2K ohms
C37
Delete
R75
1.2K ohms
SW1 SC PHASE(COARSE)
R104, R105, R106
Q25 Delete
Jumper wire
Addition
Original to New

Conductor View of SYNC, C/BAR Board

Original Circuit

New Circuit

■ Mother Board


CN15
CN16
CN17
CN18
CN20
CN21
CN22
CN27
CN2
CN13
CN12
CN11
CN10
CN9
CN8
CN7
IC1
C1
D2
T1
Q1
Q2
Q3
Q4
Q5
Q6
Q7
R16 330
R15 390
R13 4.7K
R14 10K
R6 39K
R7 3.3K
R8 1K
R9 1K
R10 3.3K
R11 33K
R12 4.7K
R17 3.9K
R19 10K
R20 10K
R21 3.9K
C5 10μF16V
C6 10μF16V
C7 100μF16V
C8 10μF16V
C9 4700PF
C10 10μF16V
C11 10μF16V
JRZ5600PA
A
B

Add the shield jumper wire

Cut the pattern

Cut the pattern

Conductor View of Mother Board

3. Vol. 4 ***Replacement Parts List***

- Following replacement parts has been changed.

SYMBOL NO.	ORIGINAL PART NO.	NEW PART NO.	DESCRIPTION		
		MISCELLANEOUS			
C101	–	**ECEA1ES4R7**	Electrolytic	4.7μF	25V
C102	–	**ECEA1ES4R7**	Electrolytic	4.7μF	25V
		OUTPUT BOARD			
R2	ERD10TJ153	**ERD10TJ103**	Carbon	10K ohms	1/8W
R15	ERD10TJ103	**ERD10TJ682**	Carbon	6.8K ohms	1/8W
R26	ERD10TJ682	**ERD10TJ681**	Carbon	680 ohms	1/8W
R30	ERD10TJ103	**ERD10TJ102**	Carbon	1K ohms	1/8W
R31	ERD10TJ821	**ERD10TJ102**	Carbon	1K ohms	1/8W
R33	ERD10TJ222	**ERD10TJ221**	Carbon	220 ohms	1/8W
R34	ERD10TJ562	**ERD10TJ561**	Carbon	560 ohms	1/8W
R38	ERD10TJ472	**ERD10TJ471**	Carbon	470 ohms	1/8W
R39	ERD10TJ682	**ERD10TJ681**	Carbon	680 ohms	1/8W
R52	ERD10TJ183	**ERD10TJ123**	Carbon	12K ohms	1/8W
R60	ERD10TJ562	**ERD10TJ681**	Carbon	680 ohms	1/8W
R61	ERD10TJ152	**ERD10TJ101**	Carbon	100 ohms	1/8W
R124	ERD10TJ183	**ERD10TJ123**	Carbon	12K ohms	1/8W
R134	ERD10TJ103	**ERD10TJ682**	Carbon	6.8K ohms	1/8W
R145	ERD10TJ682	**ERD10TJ681**	Carbon	680 ohms	1/8W
R149	ERD10TJ103	**ERD10TJ102**	Carbon	1K ohms	1/8W
R150	ERD10TJ821	**ERD10TJ102**	Carbon	1K ohms	1/8W
R152	ERD10TJ222	**ERD10TJ221**	Carbon	220 ohms	1/8W
R153	ERD10TJ562	**ERD10TJ561**	Carbon	560 ohms	1/8W
R156	ERD10TJ472	**ERD10TJ471**	Carbon	470 ohms	1/8W
R157	ERD10TJ682	**ERD10TJ681**	Carbon	680 ohms	1/8W
R169	ERD10TJ222	**ERD10TJ152**	Carbon	1.5K ohms	1/8W
R176	ERD10TJ183	**ERD10TJ123**	Carbon	12K ohms	1/8W
R200	ERD10TJ362	**ERD10TJ332**	Carbon	3.3K ohms	1/8W
VR7	YFPOT3321P23	**YFPOT3321P22**	Variable Resistor	200 ohms	
VR8	YFPOT3321P53	**YFPOT3321P52**	Variable Resistor	500 ohms	
VR26	YFPOT3321P23	**YFPOT3321P22**	Variable Resistor	200 ohms	
VR27	YFPOT3321P53	**YFPOT3321P52**	Variable Resistor	500 ohms	
C14	ECEA1CSS100	–	Delete		
C35	–	**ECCW1H560JC**	Ceramic	56pF	50V
C40	ECCW1H101JC	**ECCW1H270JC**	Ceramic	27pF	50V
C56	ECEA1CSS100	–	Delete		

SYMBOL NO.	ORIGINAL PART NO.	NEW PART NO.	DESCRIPTION
DSK, BGD BOARD			
Q72	2SA1254-BC	–	Delete
R43	ERD10TJ222	**ERD10TJ272**	Carbon 2.7K ohms 1/8W
R49	ERD10TJ223	**ERD10TJ153**	Carbon 15K ohms 1/8W
R166	ERD10TJ273	–	Delete
R167	ERD10TJ153	–	Delete
VR7	YFPOT3321P23	–	Delete
C30	ECCF1H100JC	–	Delete
C80	ECCF1H181JC	**ECCW1H560JC**	Ceramic 56pF 50V
C100	–	**ECCF1H101JC**	Ceramic 100pF 50V
C101	–	**ECCF1H270JC**	Ceramic 27pF 50V
EFFECT, MIX BOARD			
R43	ERD10TJ222	**ERD10TJ272**	Carbon 2.7K ohms 1/8W
R49	ERD10TJ223	**ERD10TJ153**	Carbon 15K ohms 1/8W
R102	ERD10TJ182	**ERD10TJ241**	Carbon 240 ohms 1/8W
R103	ERD10TJ682	**ERD10TJ152**	Carbon 1.5K ohms 1/8W
R154	ERD10TJ221	**ERD10TJ471**	Carbon 470 ohms 1/8W
R159	ERD10TJ682	**ERD10TJ122**	Carbon 1.2K ohms 1/8W
R162	ERD10TJ182	**ERD10TJ221**	Carbon 220 ohms 1/8W
VR7	YFPOT3321P23	–	Delete
C14	ECCF1H100JC	–	Delete
C100	–	**ECCF1H101JC**	Ceramic 100pF 50V
C101	–	**ECCF1H270JC**	Ceramic 27pF 50V
CHROMA KEY BOARD			
R17	ERD10TJ102	**ERD10TJ112**	Carbon 1.1K ohms 1/8W
R58	ERD10TJ271	**ERD10TJ561**	Carbon 560 ohms 1/8W
R59	ERD10TJ271	**ERD10TJ561**	Carbon 560 ohms 1/8W
R61	ERD10TJ271	**ERD10TJ561**	Carbon 560 ohms 1/8W
R62	ERD10TJ271	**ERD10TJ561**	Carbon 560 ohms 1/8W
WIPE PROCESS BOARD			
VR1	YFPOT3321P13	**YFPOT3321P23**	Variable Resistor 2K ohms
WAVEFORM GEN. BOARD			
R102	–	**ERD10TJ102**	Carbon 1K ohms 1/8W
VR8	YFPOT3321P13	–	Delete
C25	ECQV05103JZ	**ECQV1H153JZ**	Plastic 0.015μF 50V
MODULATION BOARD			
R82	–	**ERD10TJ563**	Carbon 56K ohms 1/8W
C19	ECCF1H332JC	**ECCF1H182JC**	Ceramic 1800pF 50V

SYMBOL NO.	ORIGINAL PART NO.	NEW PART NO.	DESCRIPTION		
LEVER BOARD					
D1	–	**MA27A**	Diode		
POSITION-1 BOARD					
C2	ECQV05393JZ	**ECQV05683JZ**	Plastic	$0.068\mu F$	50V
SYNC, C/BAR BOARD					
Q25	2SD636-RS	–	Delete		
R35	ERD10TJ392	**ERD10TJ222**	Carbon	2.2K ohms	1/8W
R57	ERD10TJ102	**ERD10TJ561**	Carbon	560 ohms	1/8W
R72	ERD10TJ682	**ERD10TJ622**	Carbon	6.2K ohms	1/8W
R75	ERD10TJ222	**ERD10TJ122**	Carbon	1.2K ohms	1/8W
R104	ERD10TJ562	–	Delete		
R105	ERD10TJ562	–	Delete		
R106	ERD10TJ102	–	Delete		
C37	ECCF1H101JC	–	Delete		
L10	YFL54R7J	**YFCSL094R7K**	Coil	$4.7\mu H$	